signetics

DUAL D-TYPE MASTER-SLAVE FLIP-FLOP 10131

10131F: –30 to +85°C

DIGITAL 10,000 SERIES ECL

DESCRIPTION

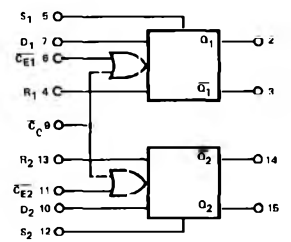
The 10131 is a dual master-slave type D flip-flop. Asynchronous set (S) and reset (R) override clock ($\overline{C}$) and clock enable ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the clock enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master-slave construction. Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

The 10131 is pin compatible with the 10130 dual D-type latch.

LOGIC DIAGRAM

10131



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = "1"

FEATURES

- f_{TOG} = 125 MHz MIN
  = 160 MHz TYP
- FAST PROPAGATION DELAY
  = 2.8 ns TYP (SET, RESET)
  = 3.0 ns TYP (CLOCK)
- LOW POWER DISSIPATION = 235 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY
  – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- OPEN EMITTER LOGIC AND BUSSING CAPABILITY
- PIN COMPATIBLE WITH 10130

APPLICATIONS

- CONTROL LOGIC
- STATUS LOGIC
- COUNTERS
- SHIFT REGISTER
- PRESCALERS

TRUTH TABLE

D	C*	S	R	Q_{n+1}
ϕ	L	L	L	Q_n
L	H	L	L	L
H	H	L	L	H
ϕ	*ϕ	H	L	H
ϕ	ϕ	L	H	L
ϕ	ϕ	H	H	N.D.

*An H represents a transition from L to H between t = n and t = n + 1

$C = C_C + \overline{CE}$

N.D. = Not defined

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

ELECTRICAL CHARACTERISTICS
(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES Vdc ± 1% $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.600	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10131 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	45	58	–	–	mAdc	9	–	–	–	8	1,16
Input Current	I_{inH}	4	–	–	–	–	330	–	–	μAdc	4	–	–	–	8	1,16
		5	–	–	–	–	330	–	–		5	–	–	–		
		6	–	–	–	–	220	–	–		6	–	–	–		
		7	–	–	–	–	245	–	–		7	–	–	–		
		9	–	–	–	–	265	–	–		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1,16
		6,7,9	–	–	0.5	–	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	5	–	–	–	8	1,16
		21	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	7	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	5	–	–	–	8	1,16
		31	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	7	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	5	–	8	1,16
		21	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	–	7	8	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	5	–	8	1,16
		31	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	–	–	7	8	1,16
Switching Times Clock Input**											+1.11 Vdc		Pulse In	Pulse Out	−3.2 Vdc	+2.0 Vdc
Propagation Delay	$t_{9+\ 2-}$	2	1.4	4.6	1.5	3.0	4.5	1.5	5.0	ns	–	–	9	2	8	1,16
	$t_{9+\ 2+}$	2									7	–	9	2		
	$t_{6+\ 2+}$	2									7	–	6	2		
	$t_{6+\ 2-}$	2									–	–	6	2		
Rise Time (20% to 80%)	t_{2+}	2	0.8		1.1	2.5		1.1	4.9		7	–	9	2		
Fall Time (20% to 80%)	t_{2-}	2	0.8		1.1	2.5		1.1	4.9		–	–	9	2		
Set Input																
Propagation Delay	$t_{5+\ 2+}$	2	1.1	4.4	1.2	2.8	4.3	1.2	4.8	ns	–	–	5	2	8	1,16
	$t_{12+\ 16+}$	15									–	–	12	15		
	$t_{5+\ 3-}$	3									–	–	5	3		
	$t_{12+\ 14-}$	14									–	–	12	14		
Reset Input																
Propagation Delay	$t_{4+\ 2-}$	2	1.1	4.4	1.2	2.8	4.3	1.2	4.8	ns	–	–	4	2	8	1,16
	$t_{13+\ 15-}$	15									–	–	13	15		
	$t_{4+\ 3+}$	3									–	–	4	3		
	$t_{13+\ 14+}$	14									–	–	13	14		
Setup Time	t_{setup}	7	–	–	–	1.5	2.5	–	–	ns	–	–	6,7	2	8	1,16
Hold Time	t_{hold}	7	–	–	1.5	−0.5	–	–	–	ns	–	–	6,7	2	8	1,16
Toggle Frequency (Max)	f_{Tog}	2	125	–	125	160	–	125	–	MHz	–	–	8	2	8	1,16

*Individually test each input; apply $V_{IL\ min}$ to pin under test.

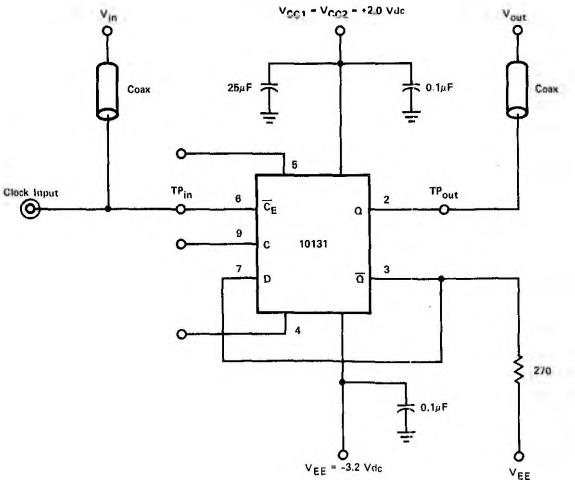
**Pin 3 is tied to pin 7 for these tests.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 6) ⎍⎍ $V_{IH\ max}$, $V_{OL\ min}$

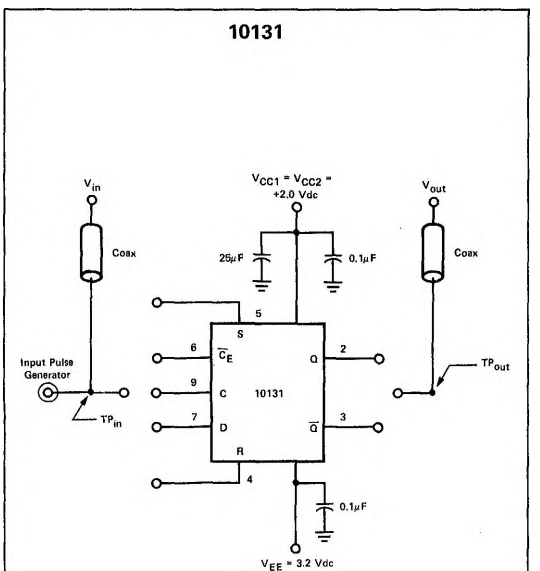
NOTES:

1. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to 2.0 volts.
2. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
3. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
4. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

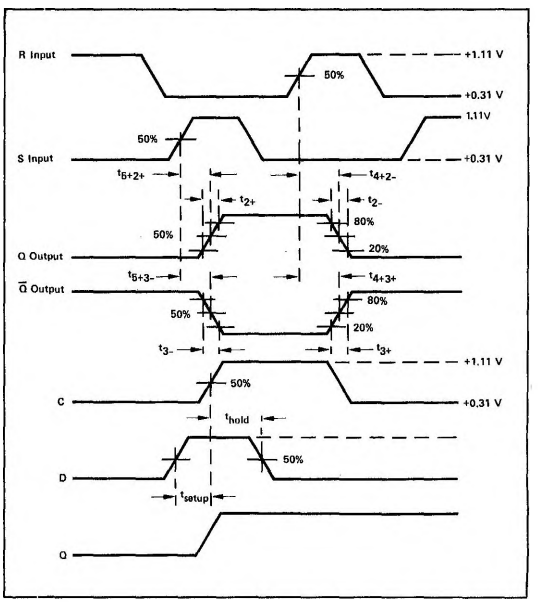
TOGGLE FREQUENCY TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C



NOTE

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

CIRCUIT SCHEMATIC

10131
(1/2 OF CIRCUIT SHOWN)