signetics

9-BIT PARITY CIRCUIT (WITH 2 CARRY INPUTS) 10170

ADVANCE INFORMATION

10170F: –30 TO +85°C, CERDIP

DIGITAL 10,000 SERIES ECL

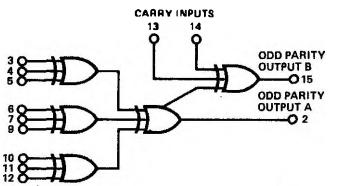
DESCRIPTION

The 10170 is a high performance parity circuit constructed with triple EXCLUSIVE-OR gates. The function is optimized for use in byte organized systems. The device can generate or check 9 bits of parity in 2 gate delays. Larger word lengths to 27 bits can be checked in 3 gate delays by connecting output A of other 10170's to the carry inputs. The carry inputs may also be used for ODD/EVEN parity control.

Output A goes high with ODD parity on input pins 3 through 12. (That is if there are 1,3,5,7, or 9 '1's on these inputs). Output B goes high for ODD parity on output A and carry input pins 13 and 14. (That is if there are 1,3,5,7,9 or 11 '1's on input pins 3 through 14).

LOGIC DIAGRAM

10170



V_{CC1} = 1, V_{CC2} = 16, V_{EE} = 8
POSITIVE LOGIC: HIGH LEVEL = '1'

FEATURES

- OPTIMIZED FOR BYTE-ORGANIZED SYSTEMS
- FAST PROPAGATION DELAY
  = 4.0 ns TYP (INPUT TO OUTPUT A)
  = 6.0 ns TYP (INPUT TO OUTPUT B)
  = 2.0 ns TYP (CARRY TO OUTPUT B)
- CARRY INPUTS FOR EASY EXPANSION OR ODD/EVEN CONTROL
- UP TO 9 BIT CHECK IN 4.0 ns
- UP TO 27 BIT CHECK IN 6.0 ns WITH NO ADDITIONAL GATES REQUIRED
- LOW POWER DISSIPATION = 280 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE 50 Ω LINES
- HIGH Z INPUTS – INTERNAL 50 kΩ PULLDOWNS
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- OPEN EMITTER OUTPUTS FOR LOGIC AND BUSSING CAPABILITY

ELECTRICAL CHARACTERISTICS

Conditions: T_A = 25°C, V_{EE} = –5.2 V ±1%

1. I_E = 54 mA dc, typ.
2. I_{inH} = 265 μA dc, max.

Conditions: T_A = 25°C, V_{CC} = +2.0 V±1%, V_{EE} = –3.2 V ±1%, 50 Ω loads

3. t_{pd} = 4.0 ns (inputs to output A)
   = 6.0 ns (inputs to output B)
   = 2.0 ns (carry to output B)
4. t_r, t_f = 2.0 ns typ. (20% to 80%)

TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP