

Intel 100 MHz Pentium(tm) II processor/440BX AGPset Uniprocessor Customer Reference Schematics Revision 1.0

**** Please note that these schematics are subject to change.**

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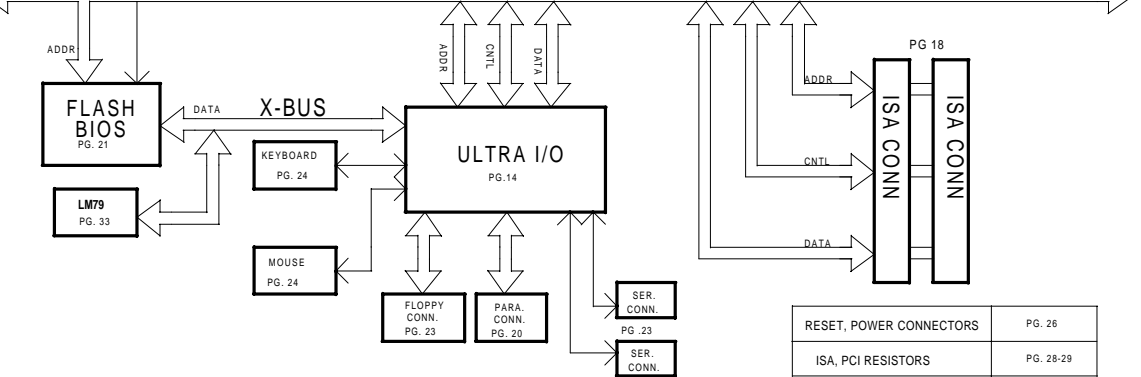
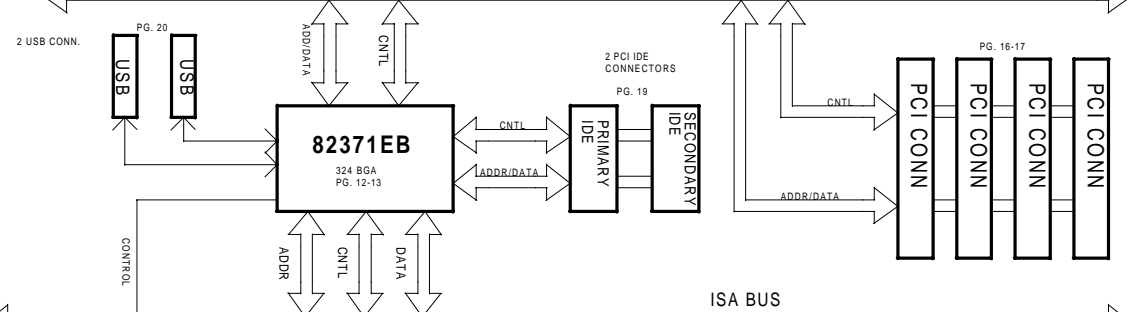
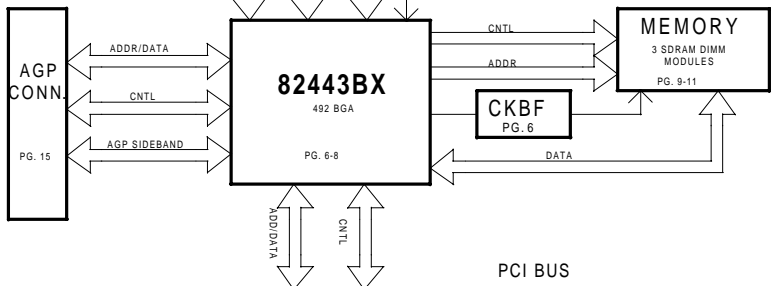
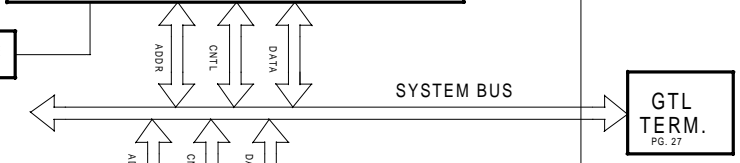
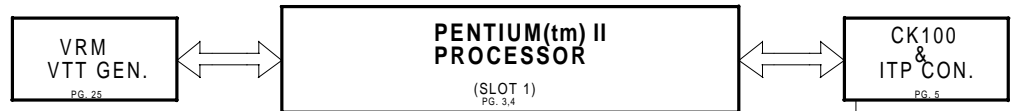
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Title Intel 100MHz Pentium(tm) II processor/440BX AGPset Uni-Processor Cover Sheet		
Size A	Document Number Intel(R) 440BX AGPset	Rev 1.0
Date: Thursday, April 09, 1998		Sheet 1 of 34



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DEVICE TABLE		
DEVICE TYPE	REFERENCE DESIGNATOR	PAGE #
FUSES	F1,F2,F3,F4	20,24
ITP Connector	J2	5
DIMM Sockets	J4,J5,J6	9,10,11
ISA Connectors	J12, J13	18
IDE Connectors	J14, J15	19
USB Connectors	J16, J17	20
VRM8.2	J24	25
Slot 1 Connector	J33 A,B	3,4
AGP Connector	J32	15
PCI Connectors	J34-37	16,17
BLM31A700S	L1-L6,L7-L13	20,24
CK100	U1	5
74LVC14 3VSB	U5 A,B,C,D,E,F	13,26
FDC37C932FR	U6	14
74AS07	U7 A,B,C,D,E,F	15,26,29
74HC14	U8 A,B,C,D,E,F	21,25,26
E28F002BC-T(FLASH)	U9	21
74F07	U12 A,B,C,D,E,F	25,26,29
74LVC3244	U13	25
74ALS08	U16 A,B,C,D	26,29
74HC10 5VSB	U17 A,B,C	13,26,29
82443BX	U19-1,2,3	6,7,8
CKBF	U20	6
LM79	U21	33
74F07 5VSB	U28 A,B,C,D,E,F	13,26,29
82371EB (PIIX4E)	U23 A,B	12,13
MAX1617 ME	U24	3
74HC112	U27 A,B	13
LT1585	VR1	25
LT1575	VR2	25
Crystal (14.318MHz)	Y1	5
Crystal(32.768KHz)	Y2	13

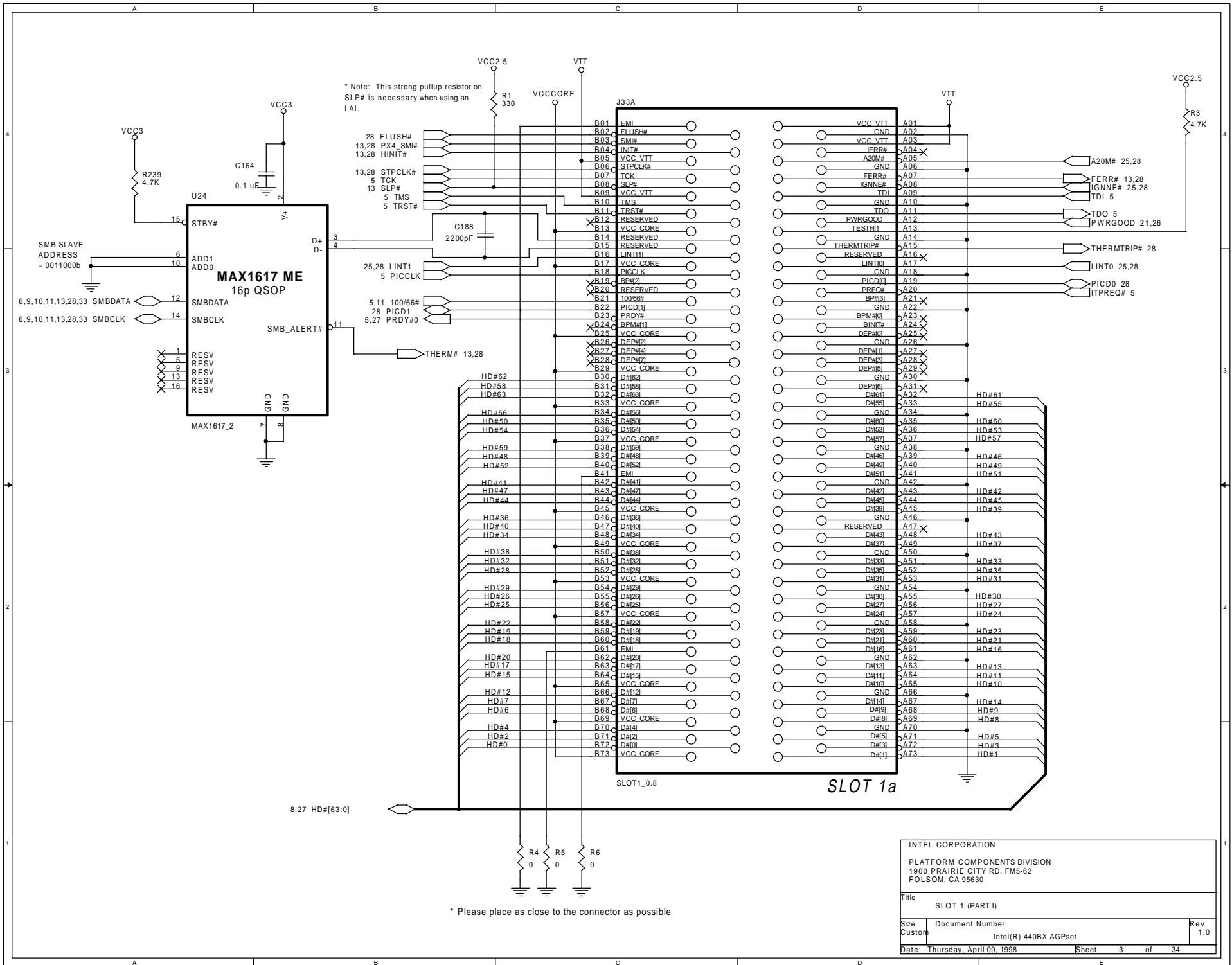
RESET, POWER CONNECTORS	PG. 26
ISA, PCI RESISTORS	PG. 28-29
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Title
 INTEL 100MHz Pentium(tm) II processor/440BX AGPset Block Diagram

Size Document Number
 Custom Intel(R) 440BX AGPset Rev 1.0

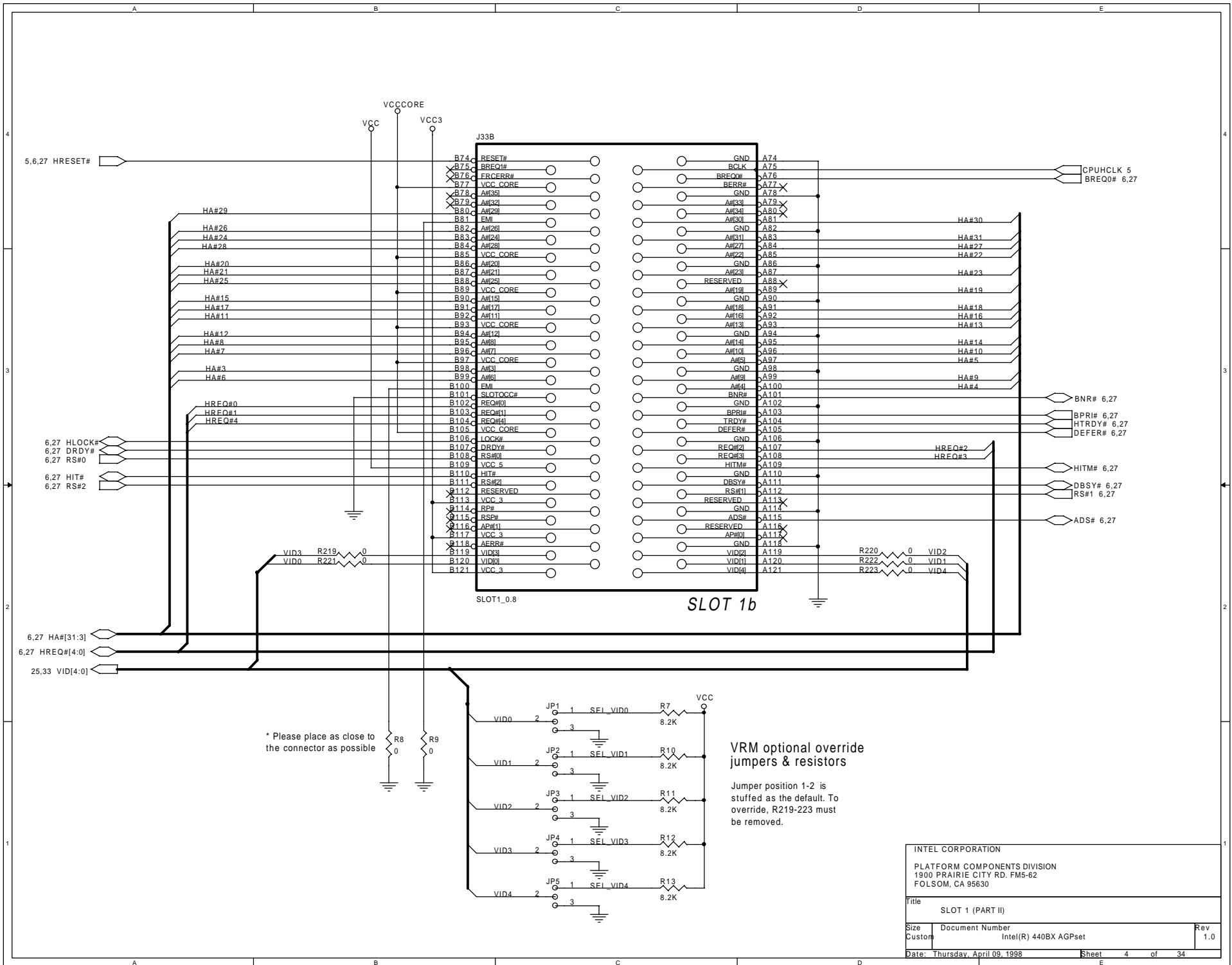
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Title			SLOT 1 (PART I)		
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* Please place as close to the connector as possible



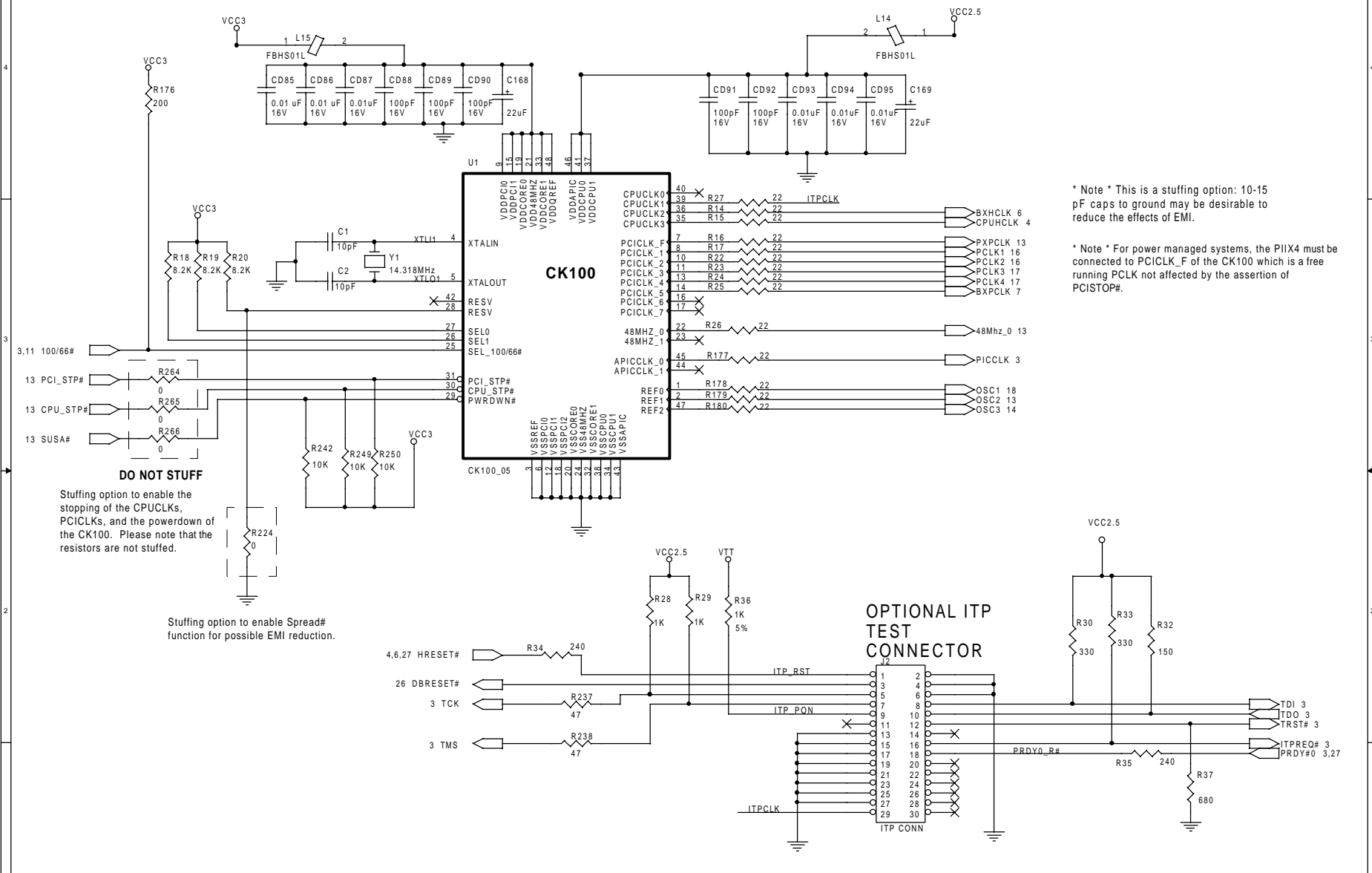
* Please place as close to the connector as possible

VRM optional override jumpers & resistors

Jumper position 1-2 is stuffed as the default. To override, R219-223 must be removed.

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Title		
SLOT 1 (PART II)		
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CLOCK SYNTHESIZER



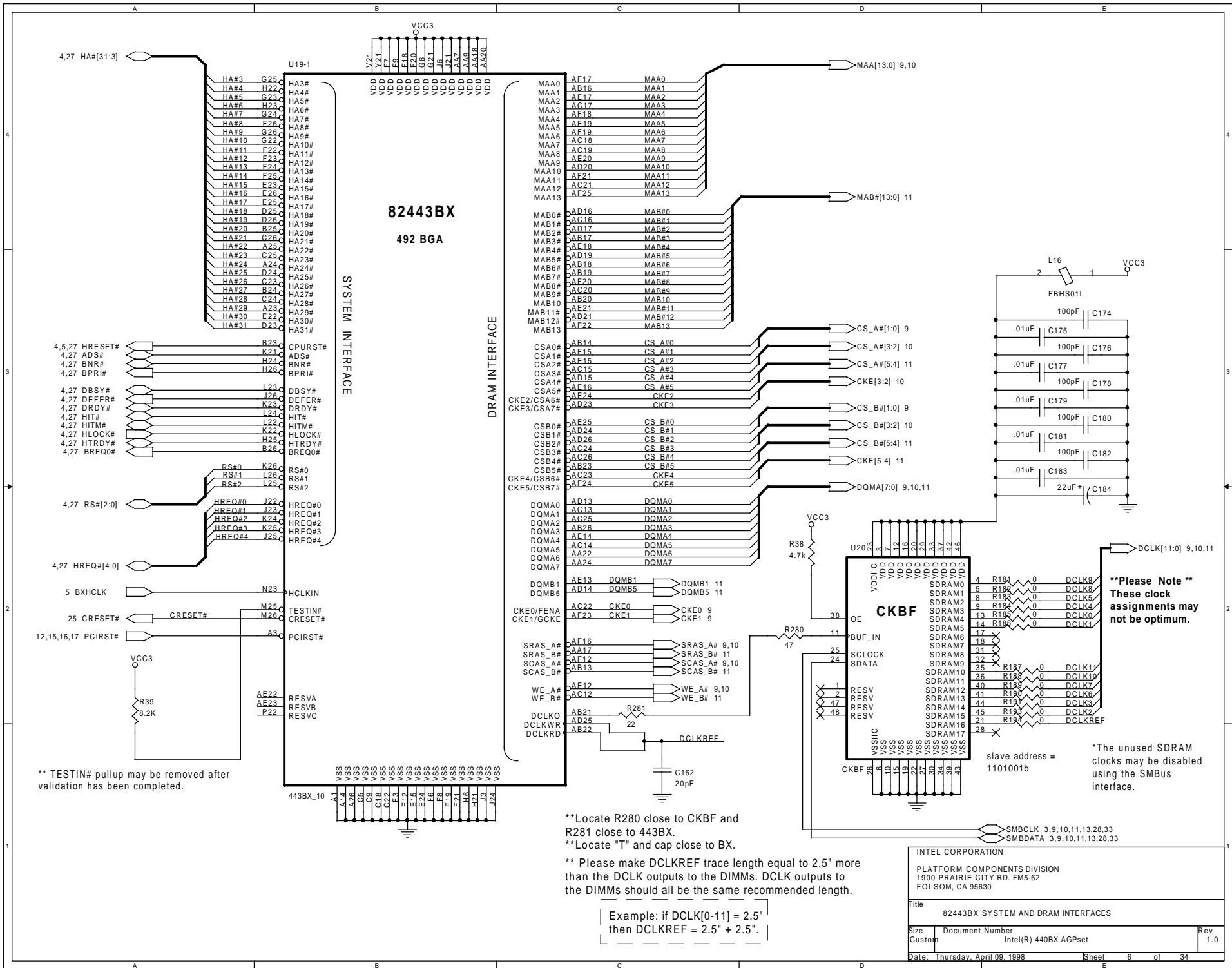
* Note * This is a stuffing option: 10-15 pF caps to ground may be desirable to reduce the effects of EMI.

* Note * For power managed systems, the PIIx4 must be connected to PCICLK_F of the CK100 which is a free running PCLK not affected by the assertion of PCISTOP#.

DO NOT STUFF
 Stuffing option to enable the stopping of the CPUCCLKs, PCICCLKs, and the powerdown of the CK100. Please note that the resistors are not stuffed.

Stuffing option to enable Spread# function for possible EMI reduction.

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82443BX
492 BGA

SYSTEM INTERFACE

DRAM INTERFACE

** TESTIN# pullup may be removed after validation has been completed.

**Locate R280 close to CKBF and R281 close to 443BX.
**Locate "T" and cap close to BX.

** Please make DCLKREF trace length equal to 2.5" more than the DCLK outputs to the DIMMs. DCLK outputs to the DIMMs should all be the same recommended length.

Example: if DCLK[0-11] = 2.5"
then DCLKREF = 2.5" + 2.5".

****Please Note****
These clock assignments may not be optimum.

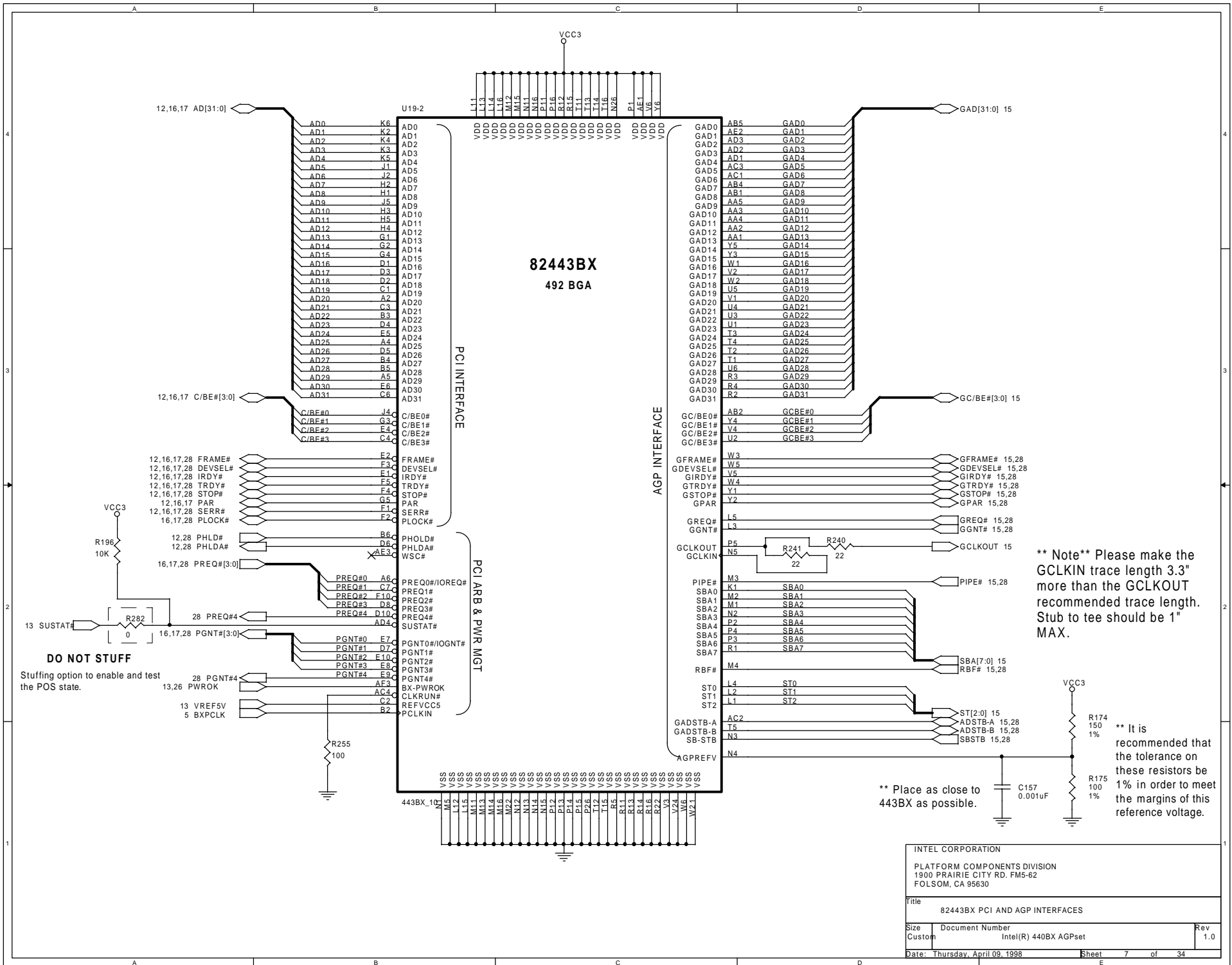
*The unused SDRAM clocks may be disabled using the SMBus interface.

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Title: 82443BX SYSTEM AND DRAM INTERFACES

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82443BX
492 BGA

PCI INTERFACE

AGP INTERFACE

PCI ARB & PWR MGT

**** Note**** Please make the GCLKIN trace length 3.3" more than the GCLKOUT recommended trace length. Stub to tee should be 1" MAX.

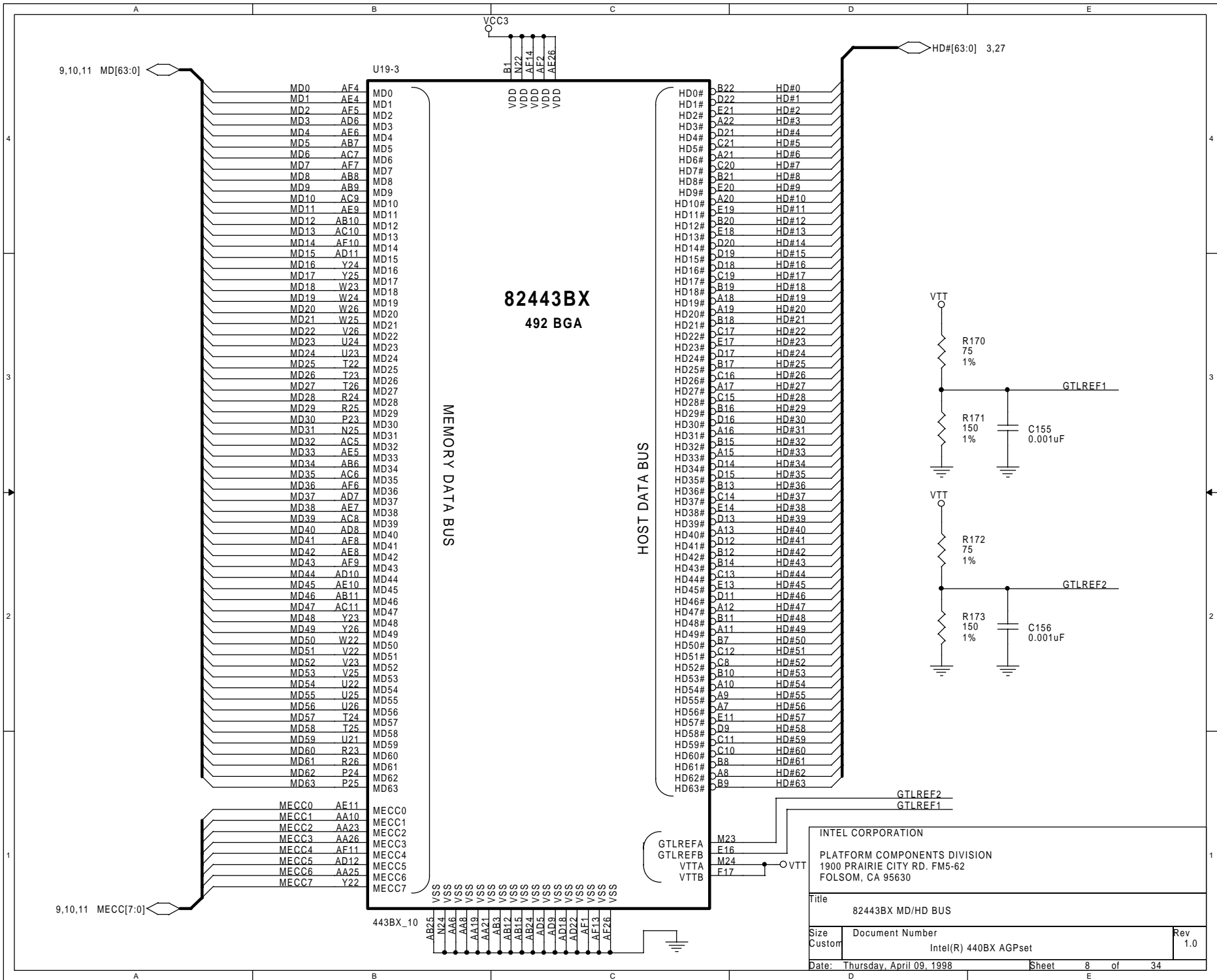
**** It is recommended that the tolerance on these resistors be 1% in order to meet the margins of this reference voltage.**

**** Place as close to 443BX as possible.**

DO NOT STUFF

Stuffing option to enable and test the POS state.

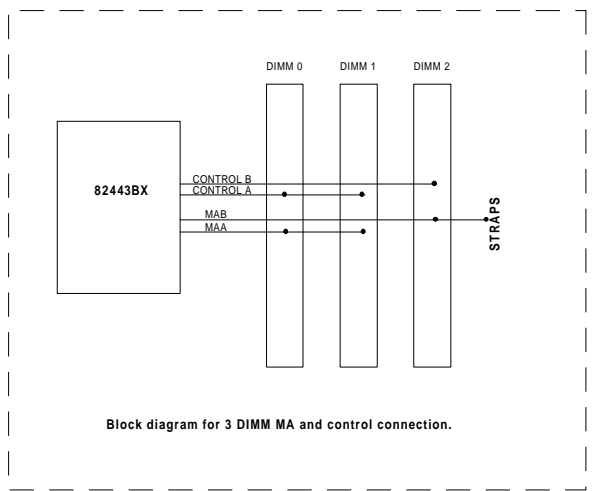
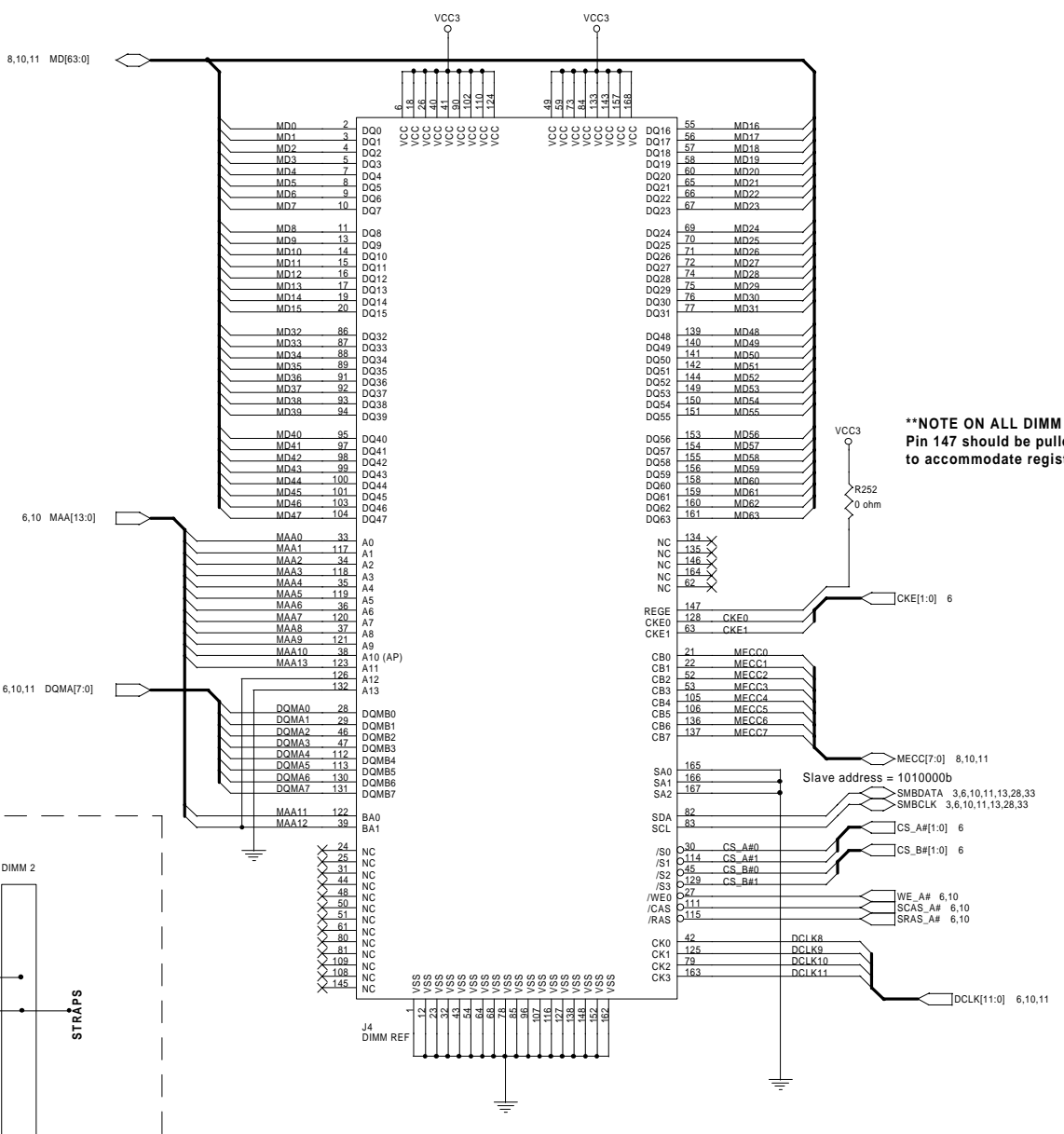
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Custom			1.0
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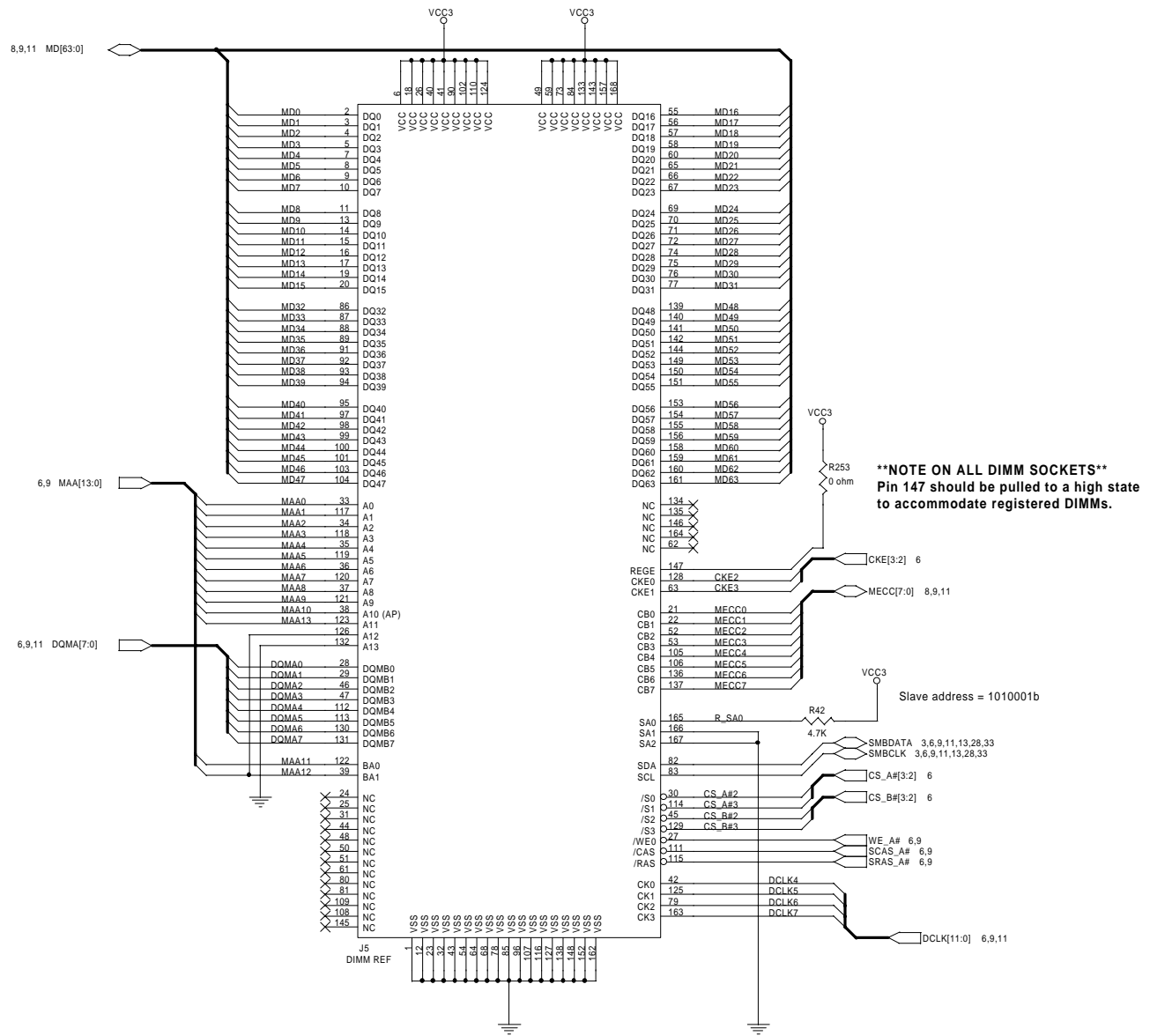
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Title		
82443BX MD/HD BUS		
Size	Document Number	Rev
Custom	Intel(R) 440BX AGPset	1.0
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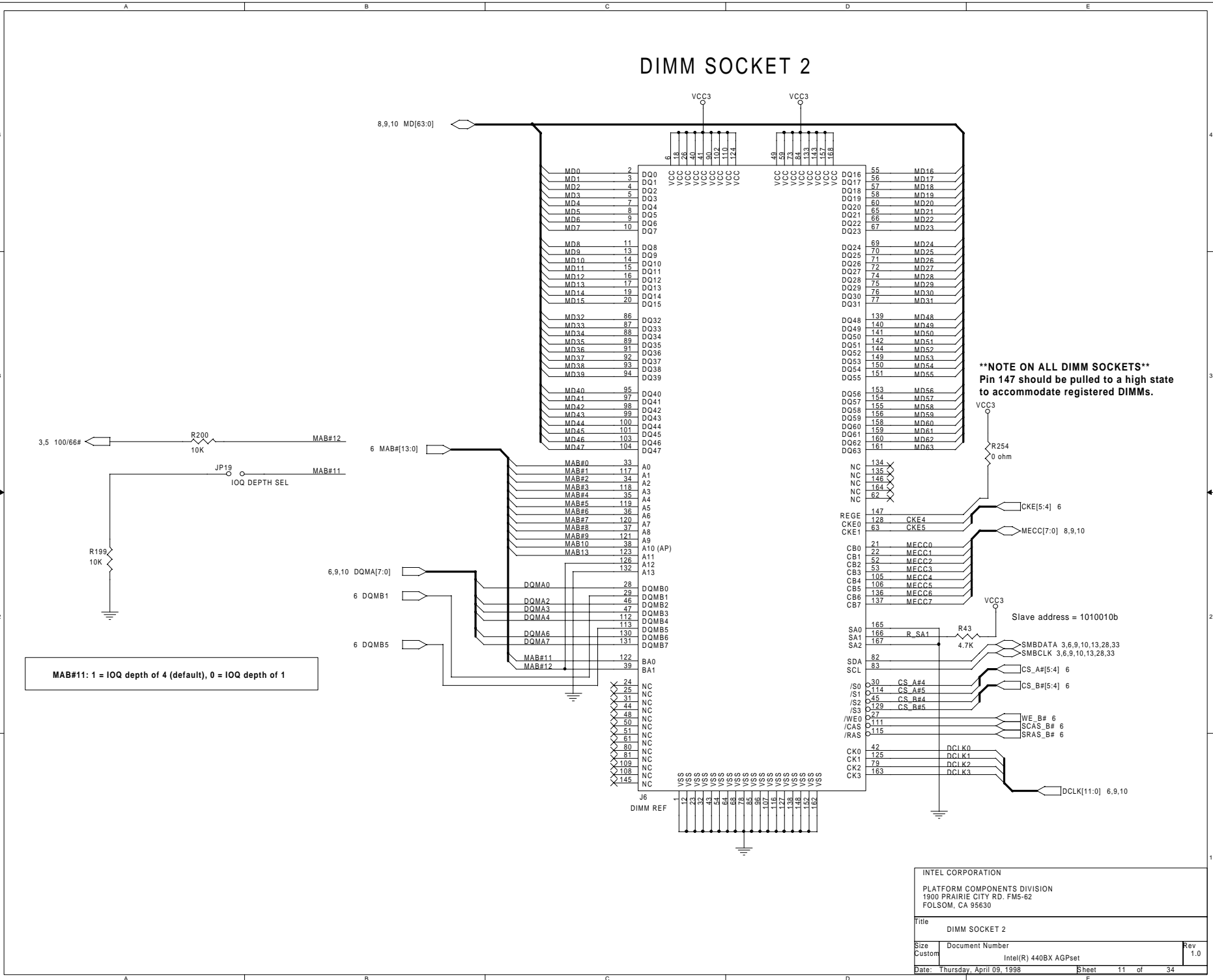
DIMM SOCKET 0

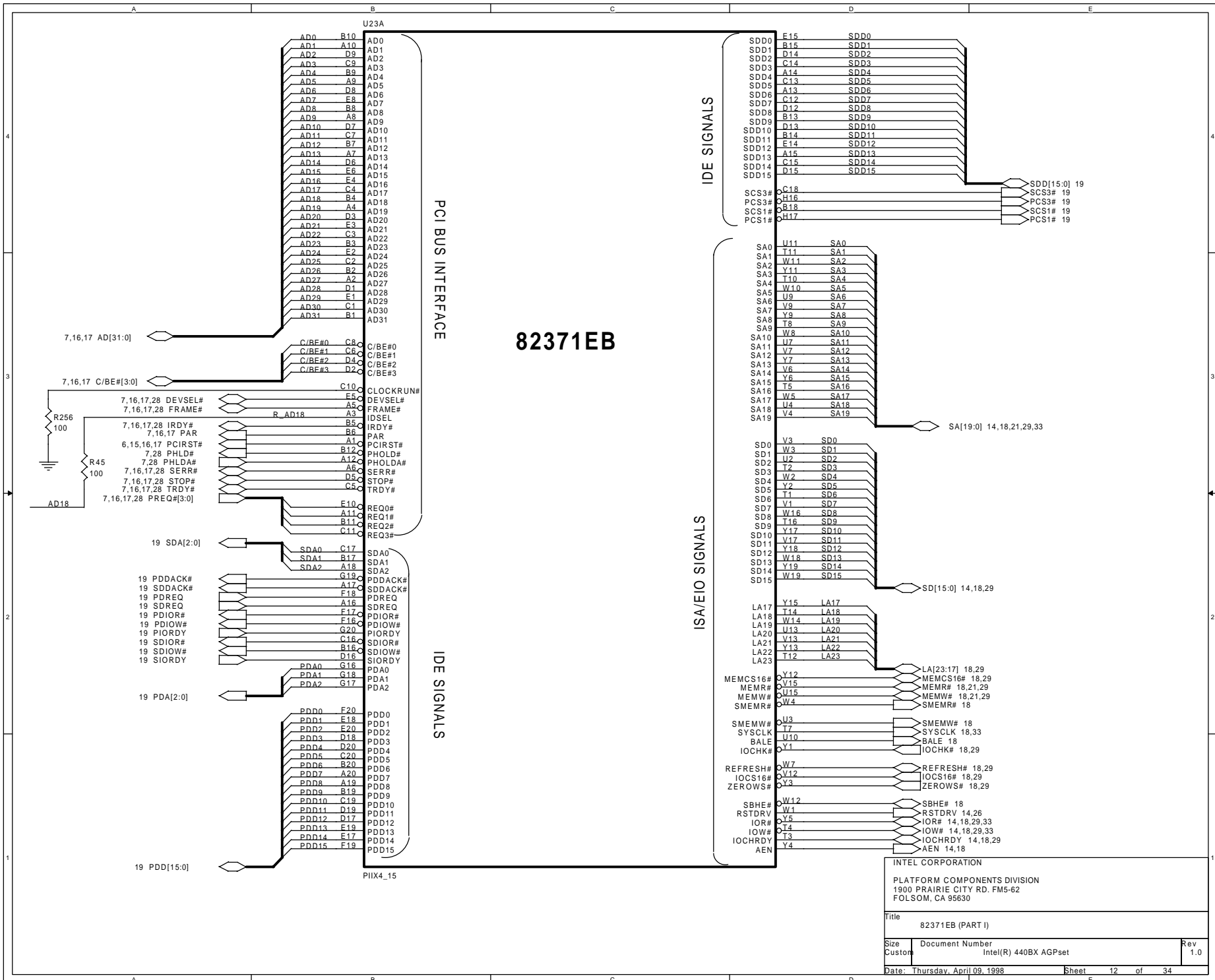


DIMM SOCKET 1



DIMM SOCKET 2





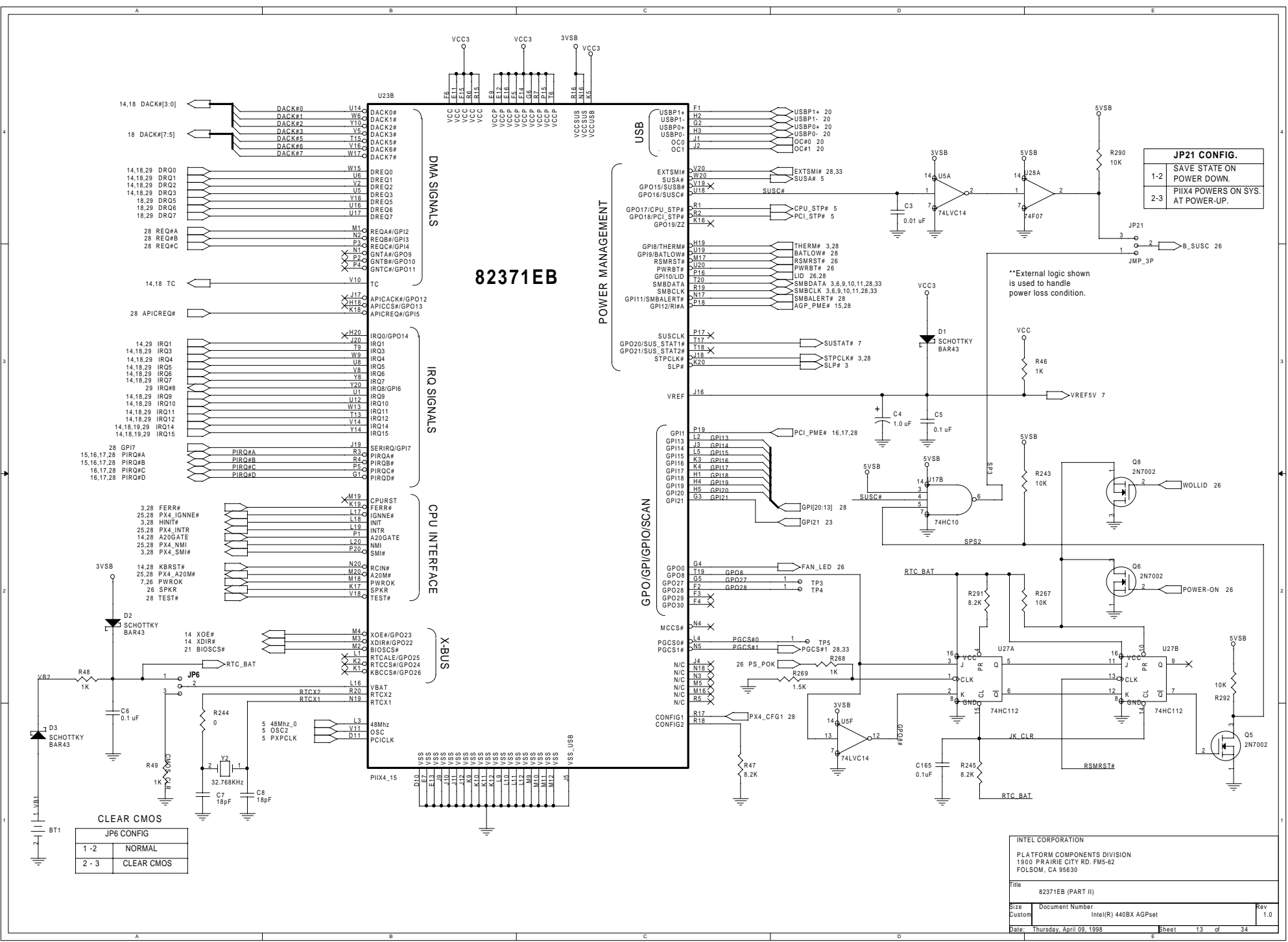
82371EB

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Title: 82371EB (PART I)

Size: Custom Document Number: Intel(R) 440BX AGPset Rev: 1.0

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82371EB

1-2	SAVE STATE ON POWER DOWN.
2-3	PIIX4 POWERS ON SYS. AT POWER-UP.

CLEAR CMOS

1 - 2	NORMAL
2 - 3	CLEAR CMOS

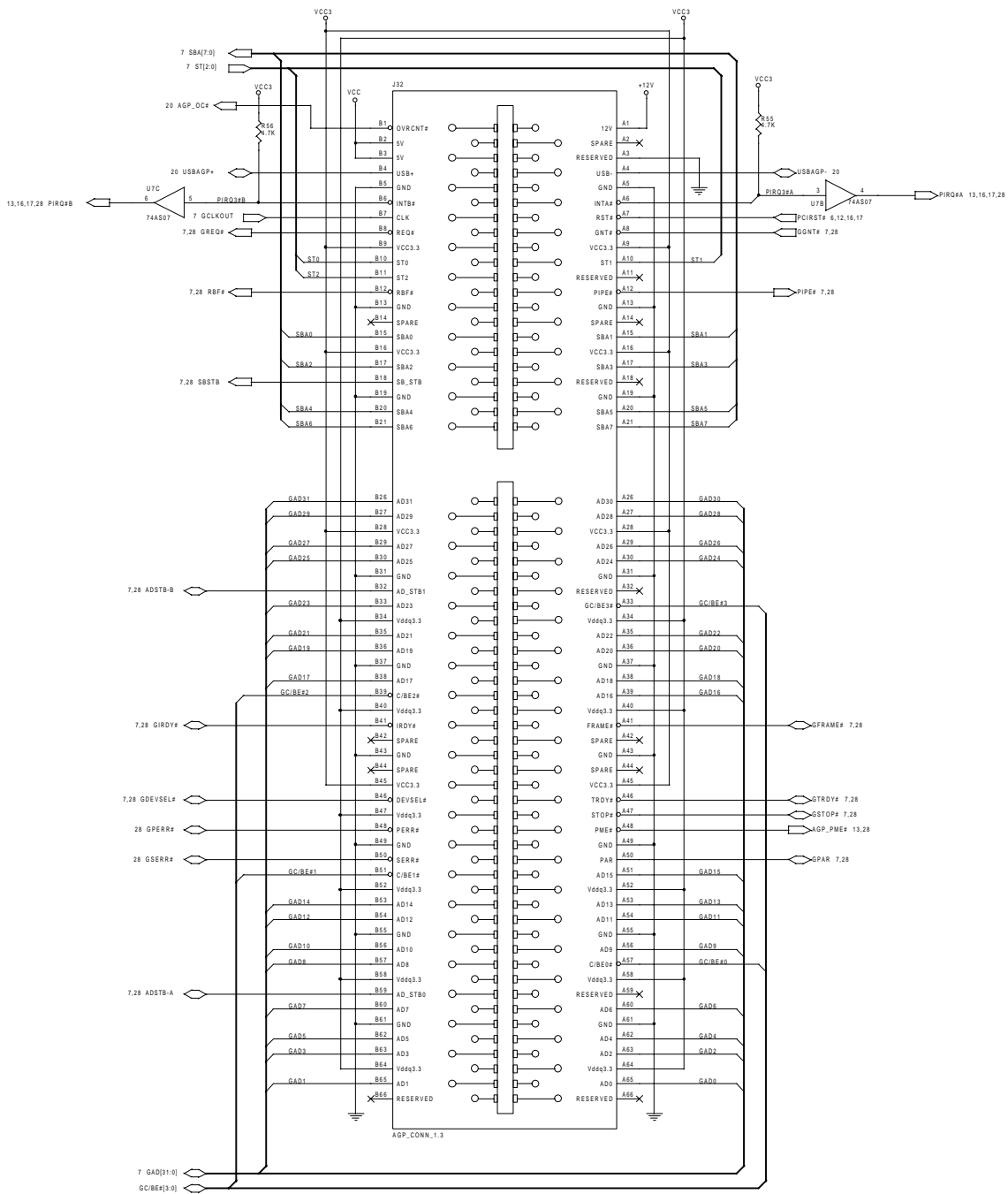
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Title: 82371EB (PART II)

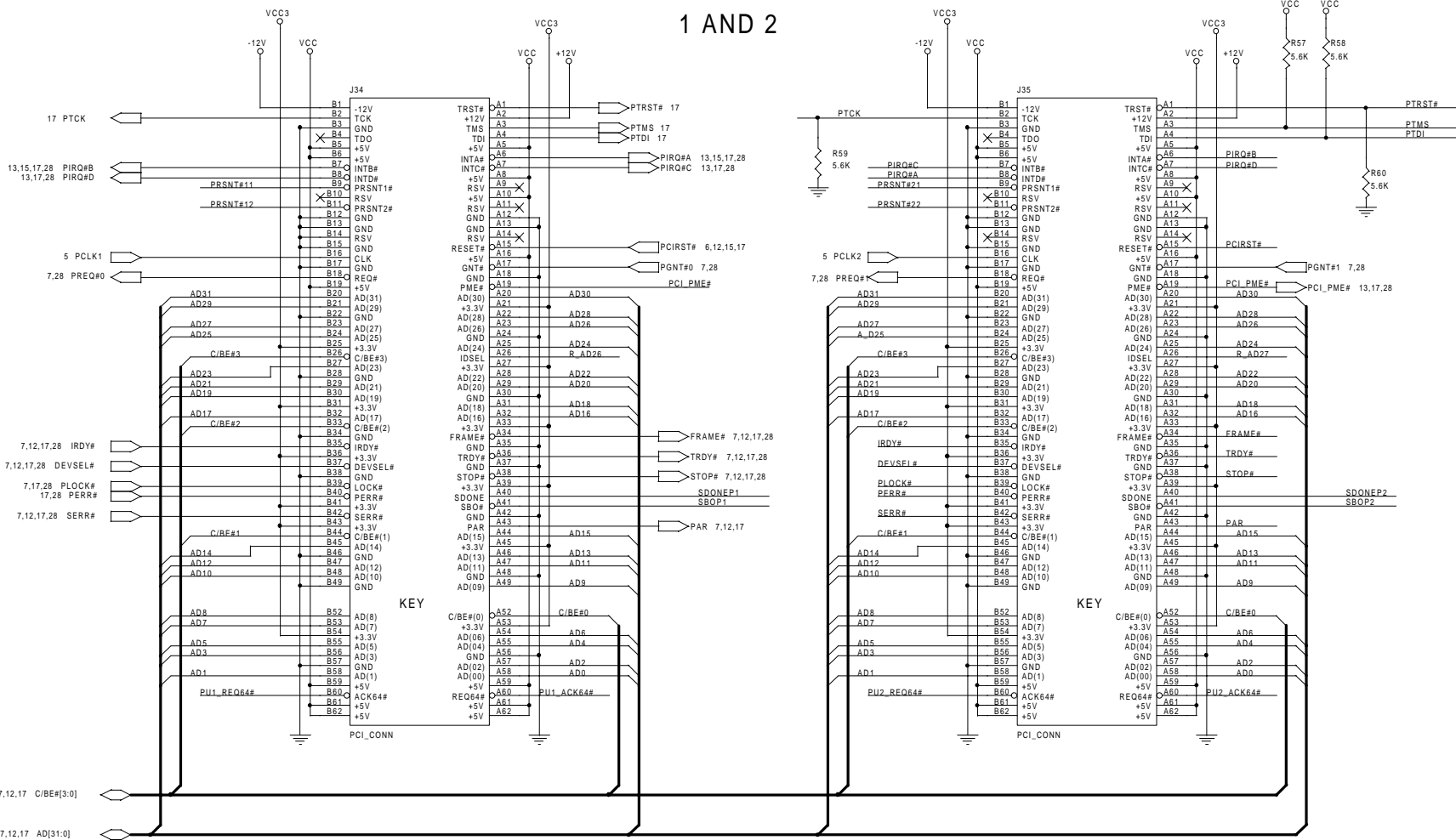
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AGP CONNECTOR

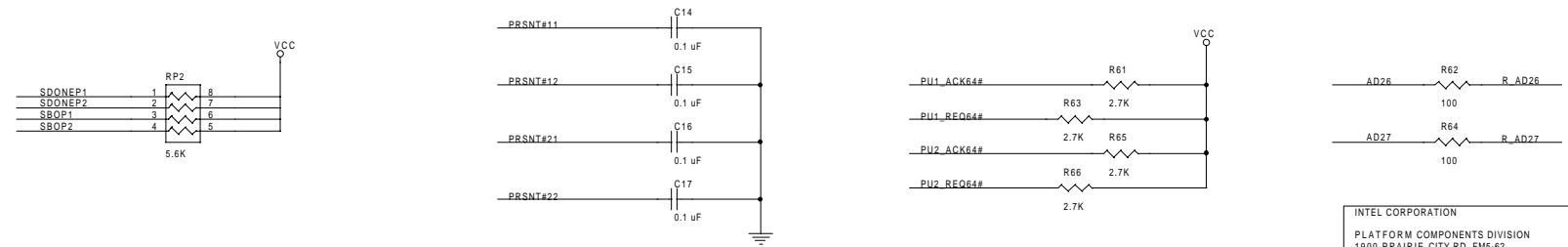


PCI CONNECTORS 1 AND 2



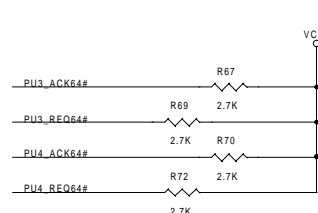
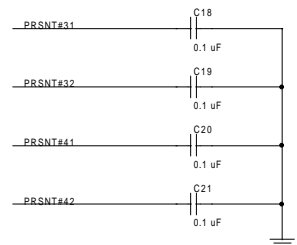
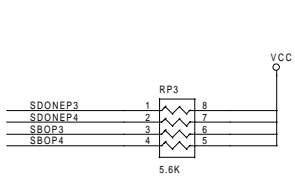
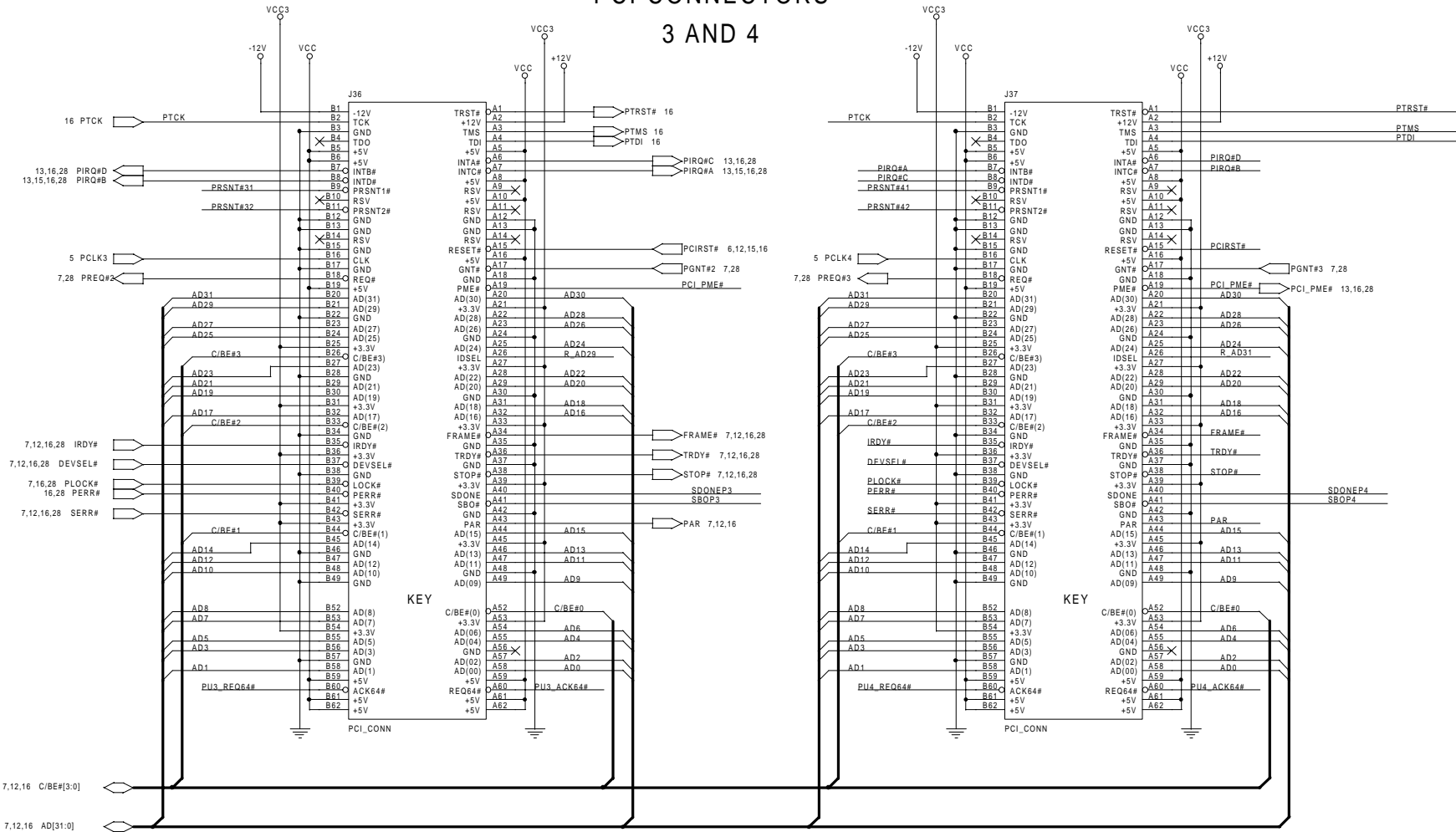
KEY

KEY



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Title: PCI CONNECTORS 1 & 2			
Size: Custom	Document Number: Intel(R) 440BX AGPset	Rev: 1.0	
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PCI CONNECTORS 3 AND 4



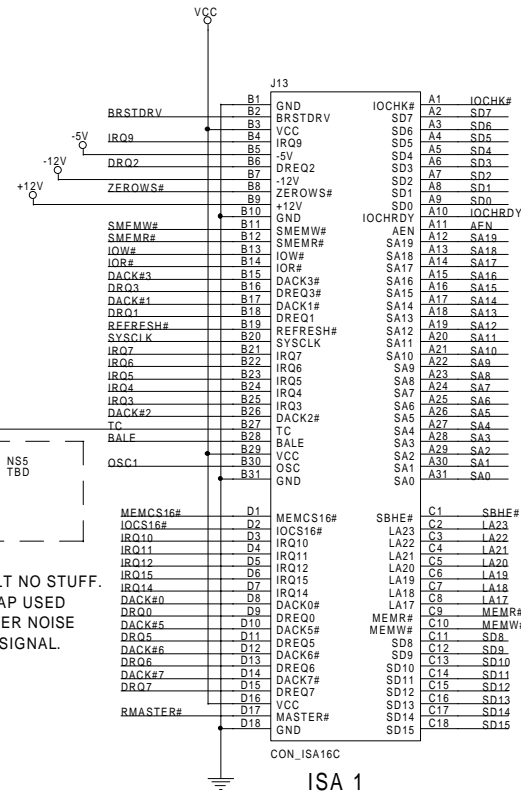
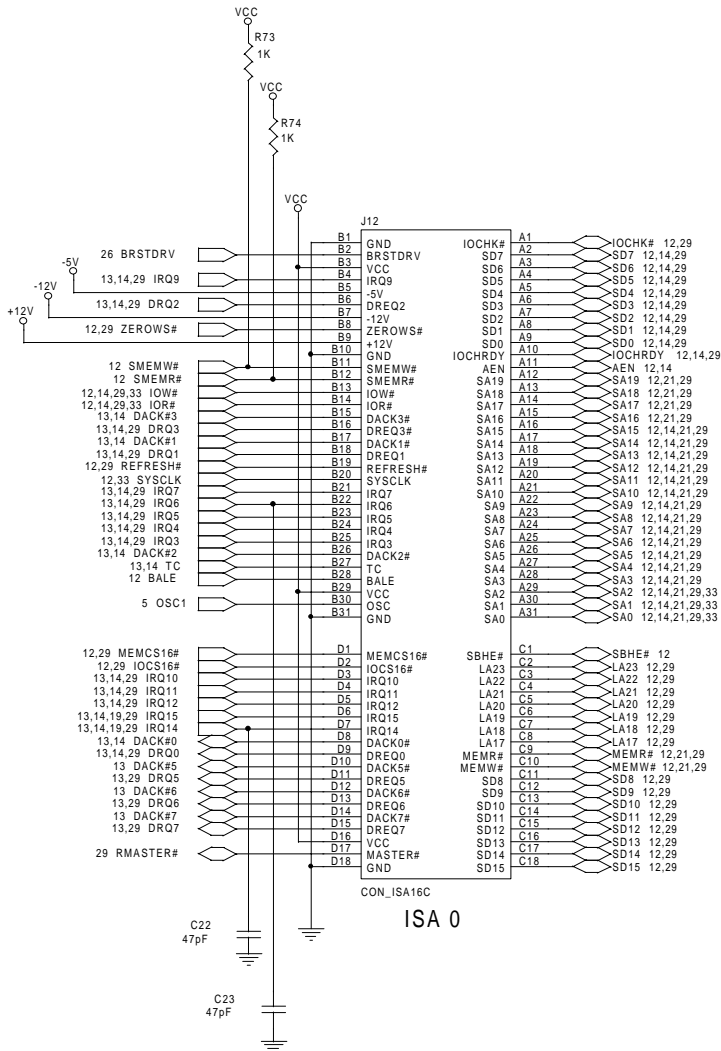
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Title: PCI CONNECTORS 3 & 4

Size: Custom Document Number: Intel(R) 440BX AGPset Rev: 1.0

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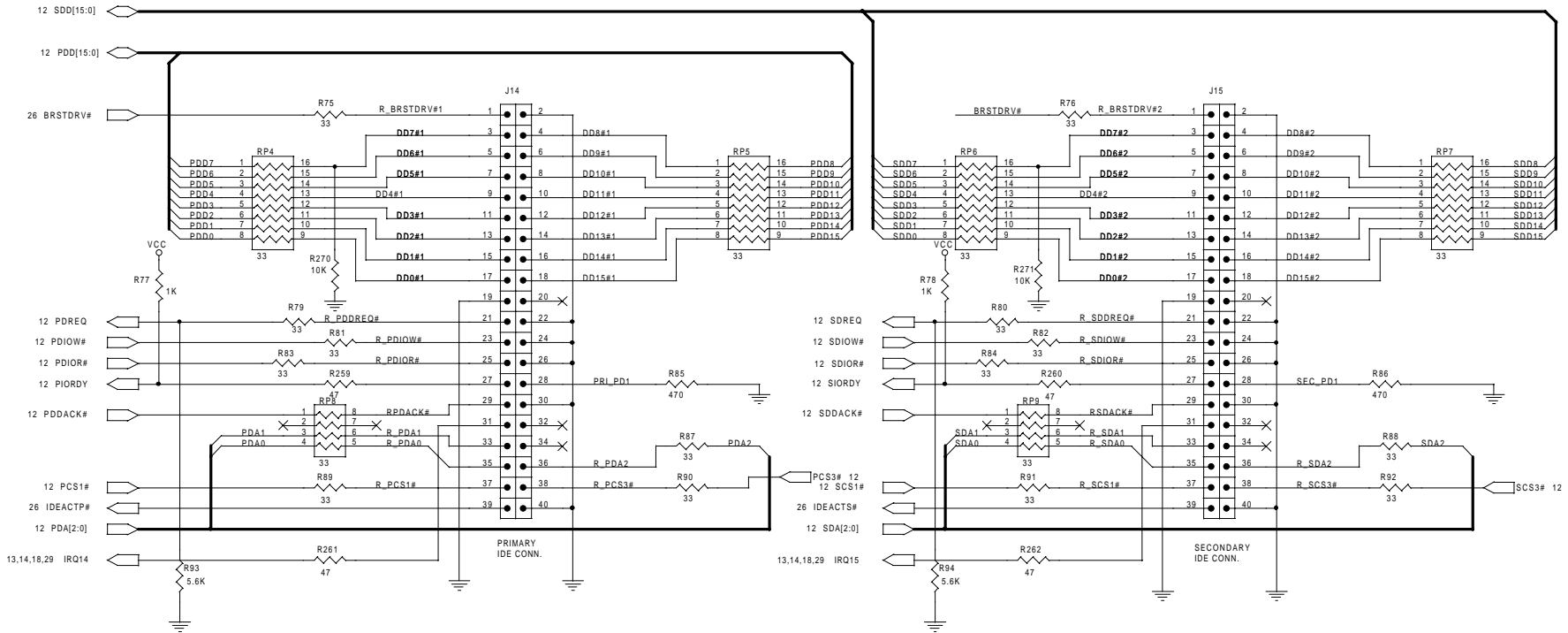
ISA SLOTS



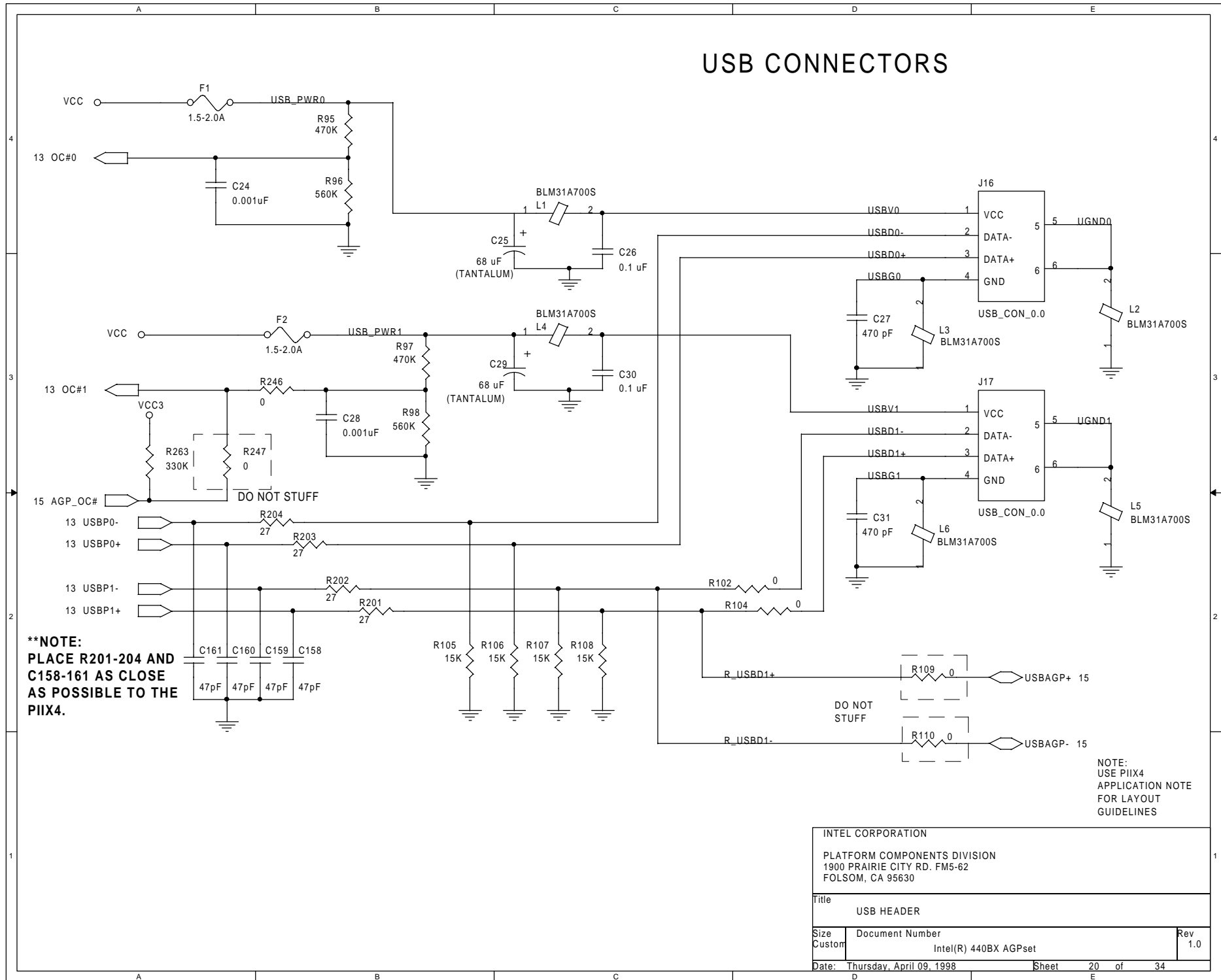
NOTE : DEFAULT NO STUFF.
THIS CAP USED
TO FILTER NOISE
ON TC SIGNAL.

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Title ISA SLOTS			
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IDE CONNECTORS



USB CONNECTORS



****NOTE:
PLACE R201-204 AND
C158-161 AS CLOSE
AS POSSIBLE TO THE
PIIX4.**

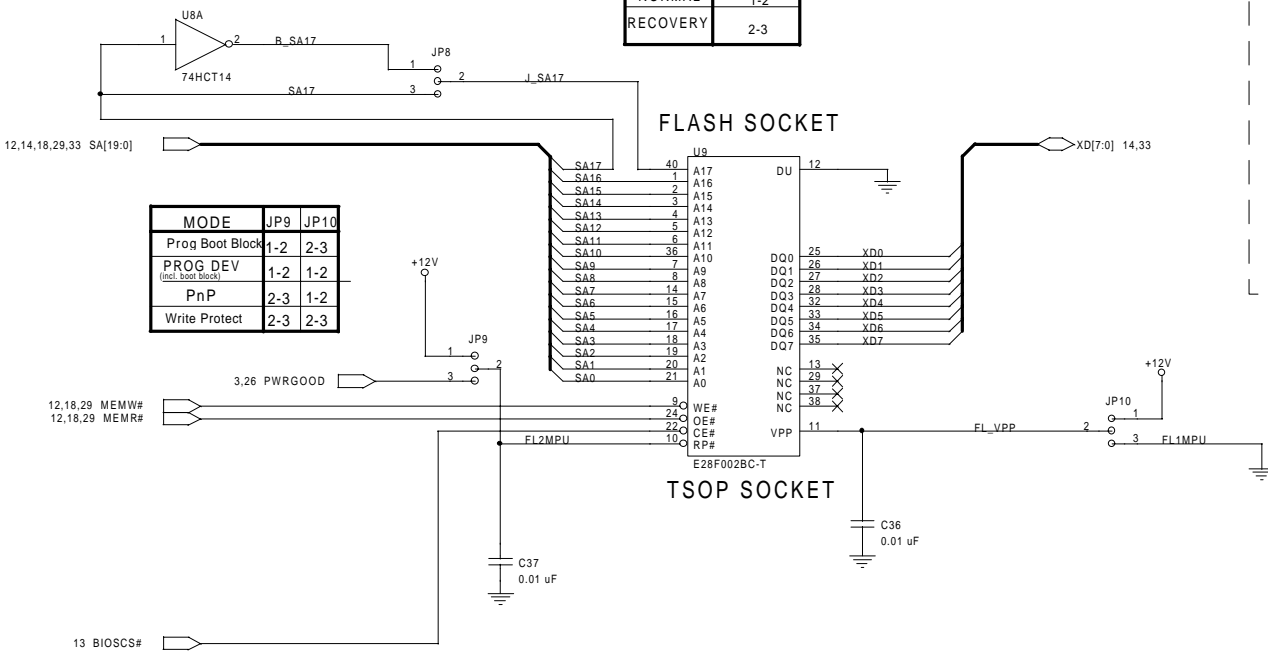
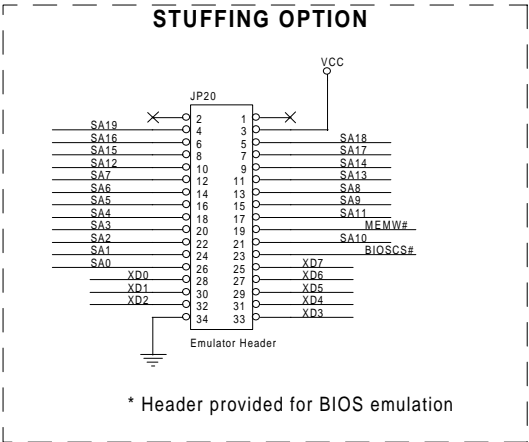
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Title		
USB HEADER		
Size	Document Number	Rev
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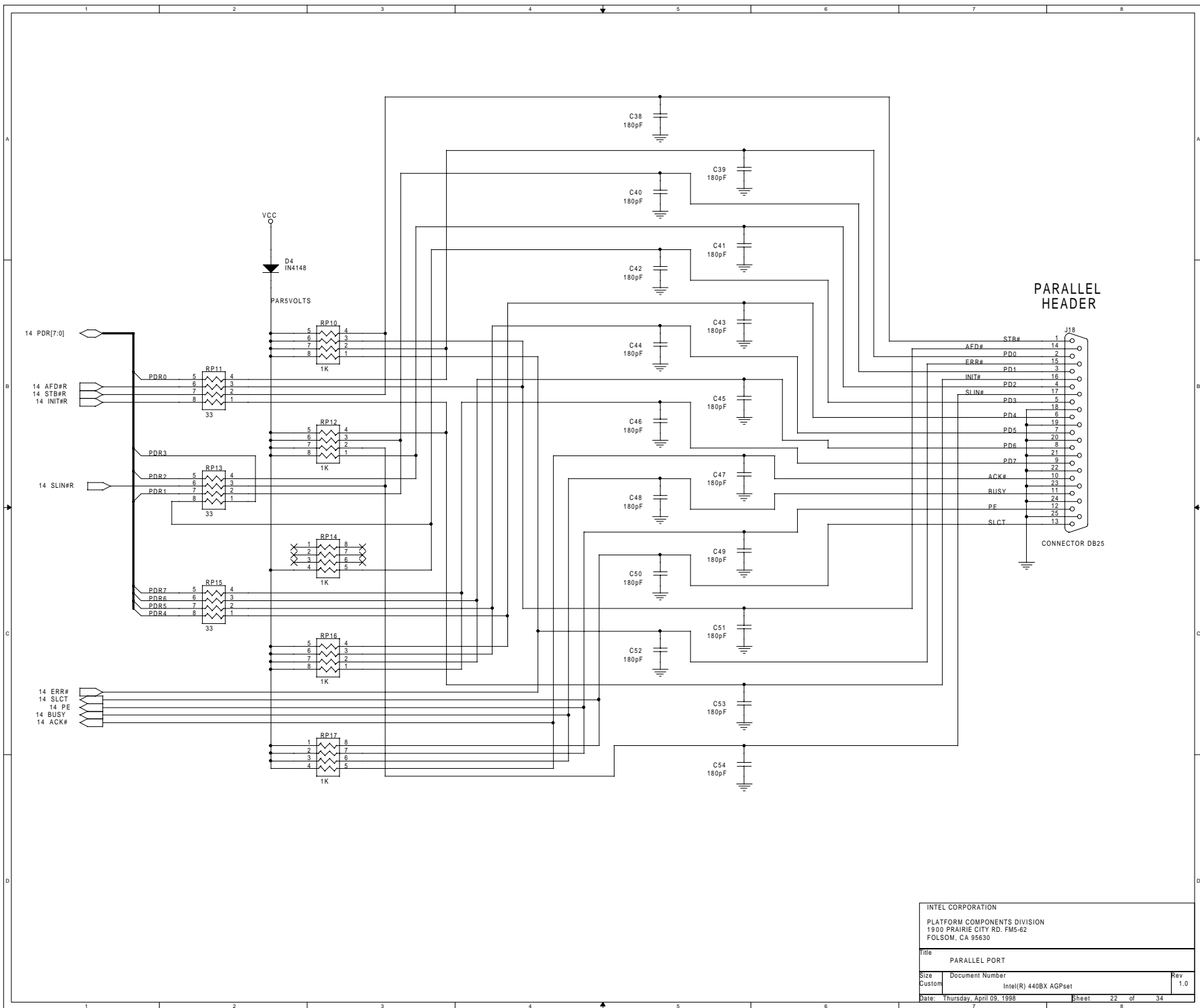
NOTE:
USE PIIX4
APPLICATION NOTE
FOR LAYOUT
GUIDELINES

SYSTEM ROM

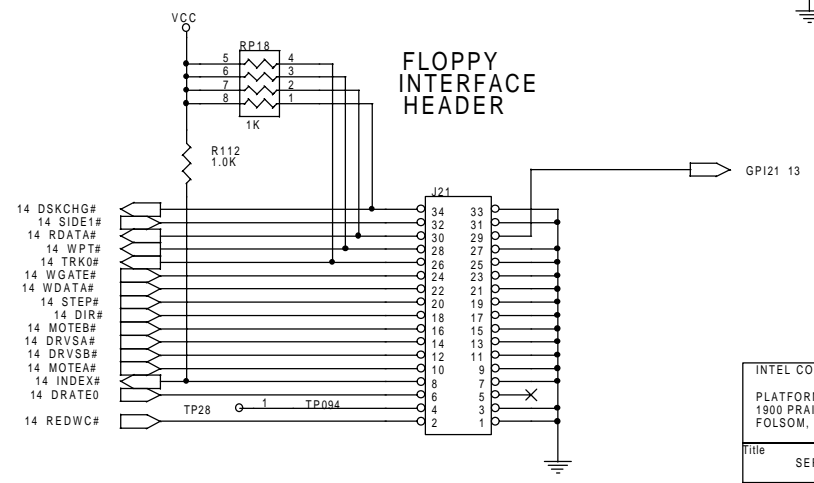
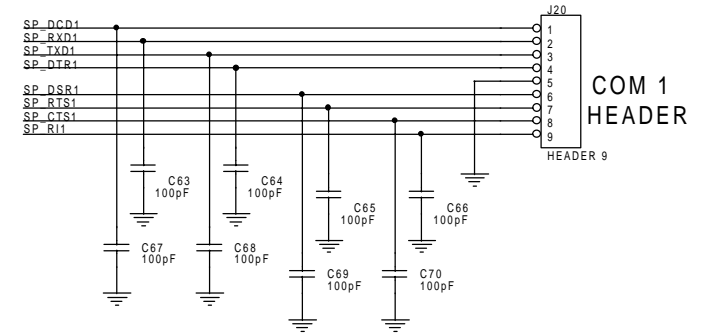
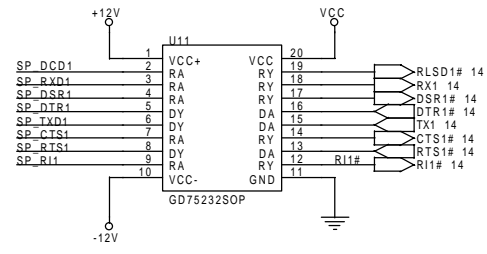
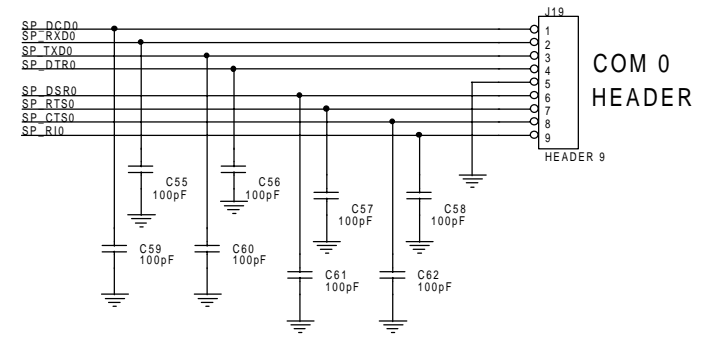
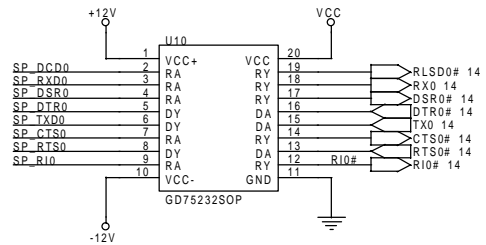
MODE	JP8
NORMAL	1-2
RECOVERY	2-3



MODE	JP9	JP10
Prog Boot Block	1-2	2-3
PROG DEV (incl. boot block)	1-2	1-2
PnP	2-3	1-2
Write Protect	2-3	2-3

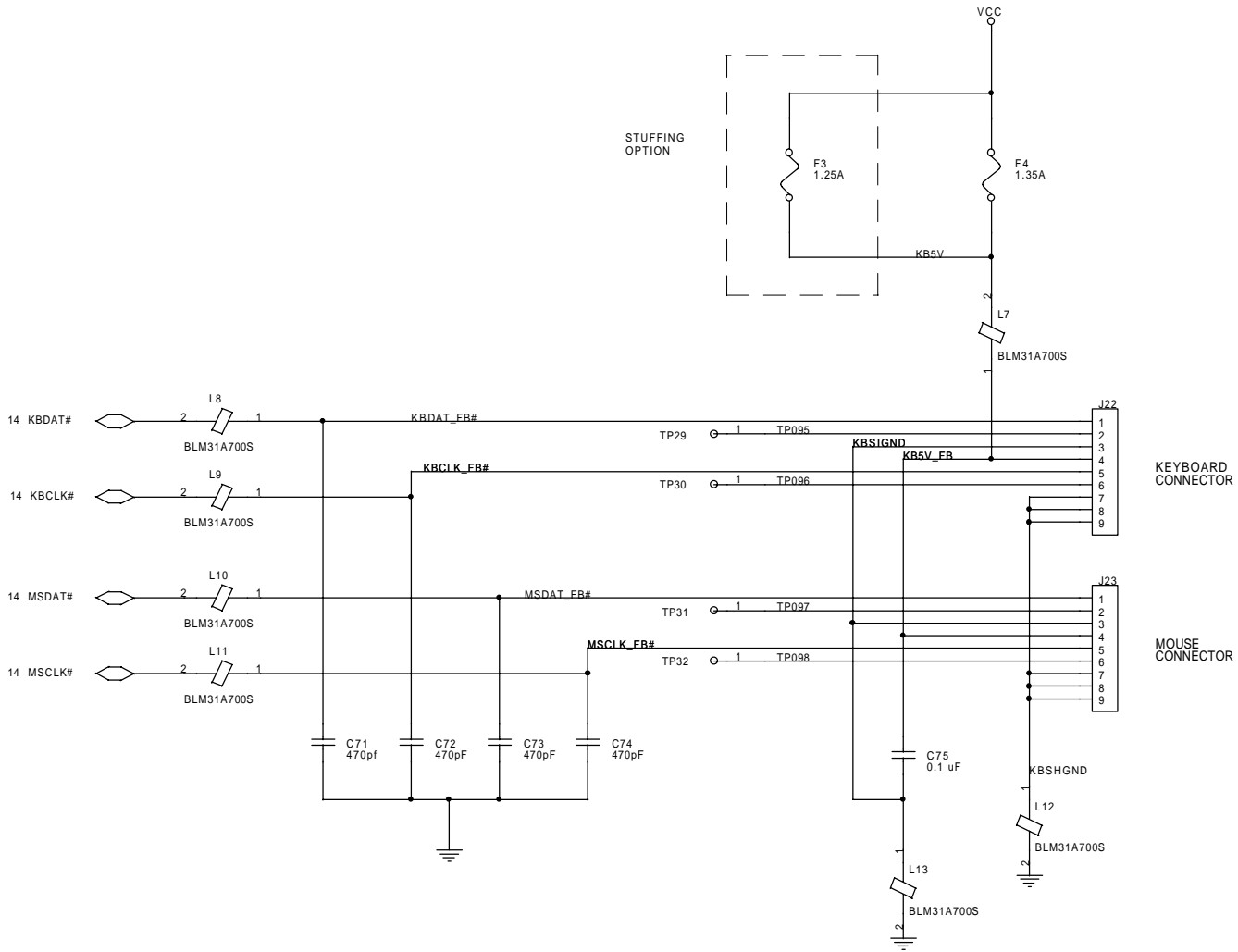


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Title PARALLEL PORT		
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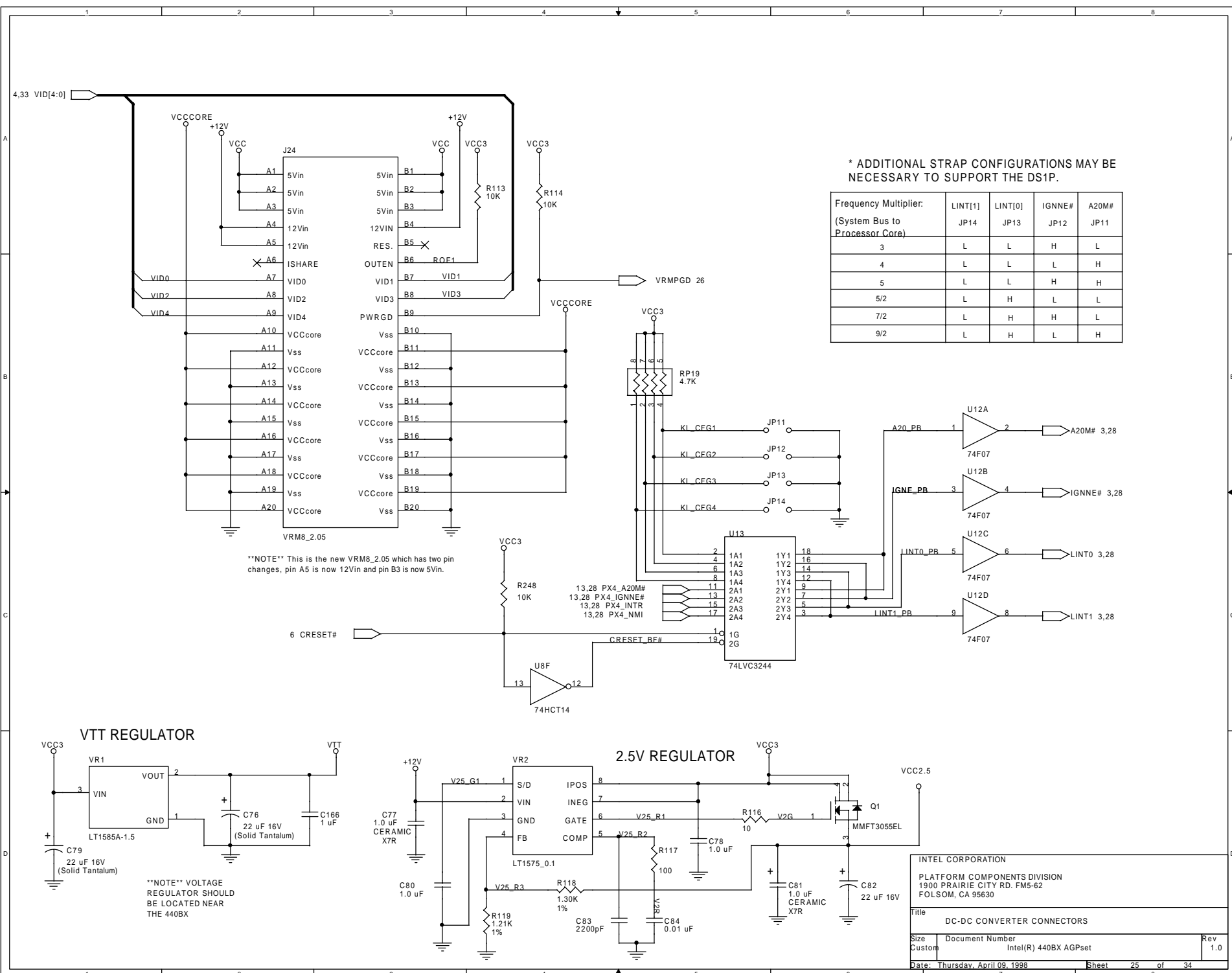


**** Connected to GPI21 of the PIIX4 for BIOS detection of a floppy drive.**

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Title		
KEYBOARD/MOUSE INTERFACE		
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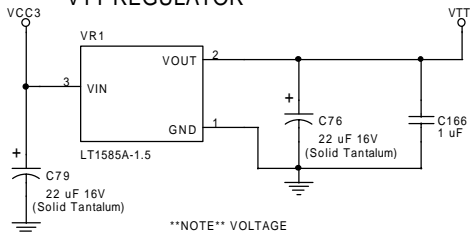


* ADDITIONAL STRAP CONFIGURATIONS MAY BE NECESSARY TO SUPPORT THE DS1P.

Frequency Multiplier: (System Bus to Processor Core)	LINT[1] JP14	LINT[0] JP13	IGNNE# JP12	A20M# JP11
3	L	L	H	L
4	L	L	L	H
5	L	L	H	H
5/2	L	H	L	L
7/2	L	H	H	L
9/2	L	H	L	H

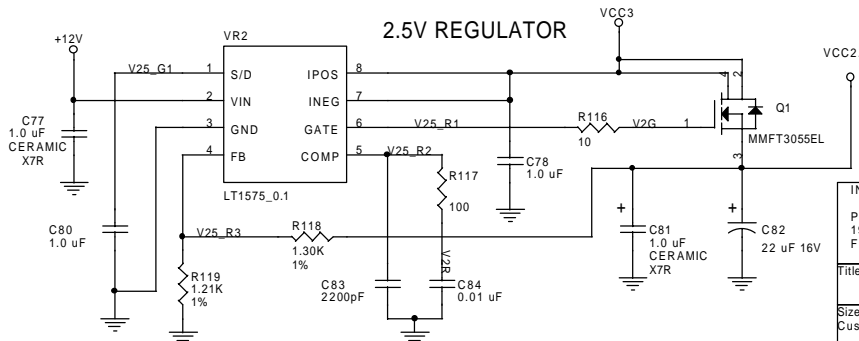
NOTE This is the new VRM8_2.05 which has two pin changes, pin A5 is now 12Vin and pin B3 is now 5Vin.

VTT REGULATOR



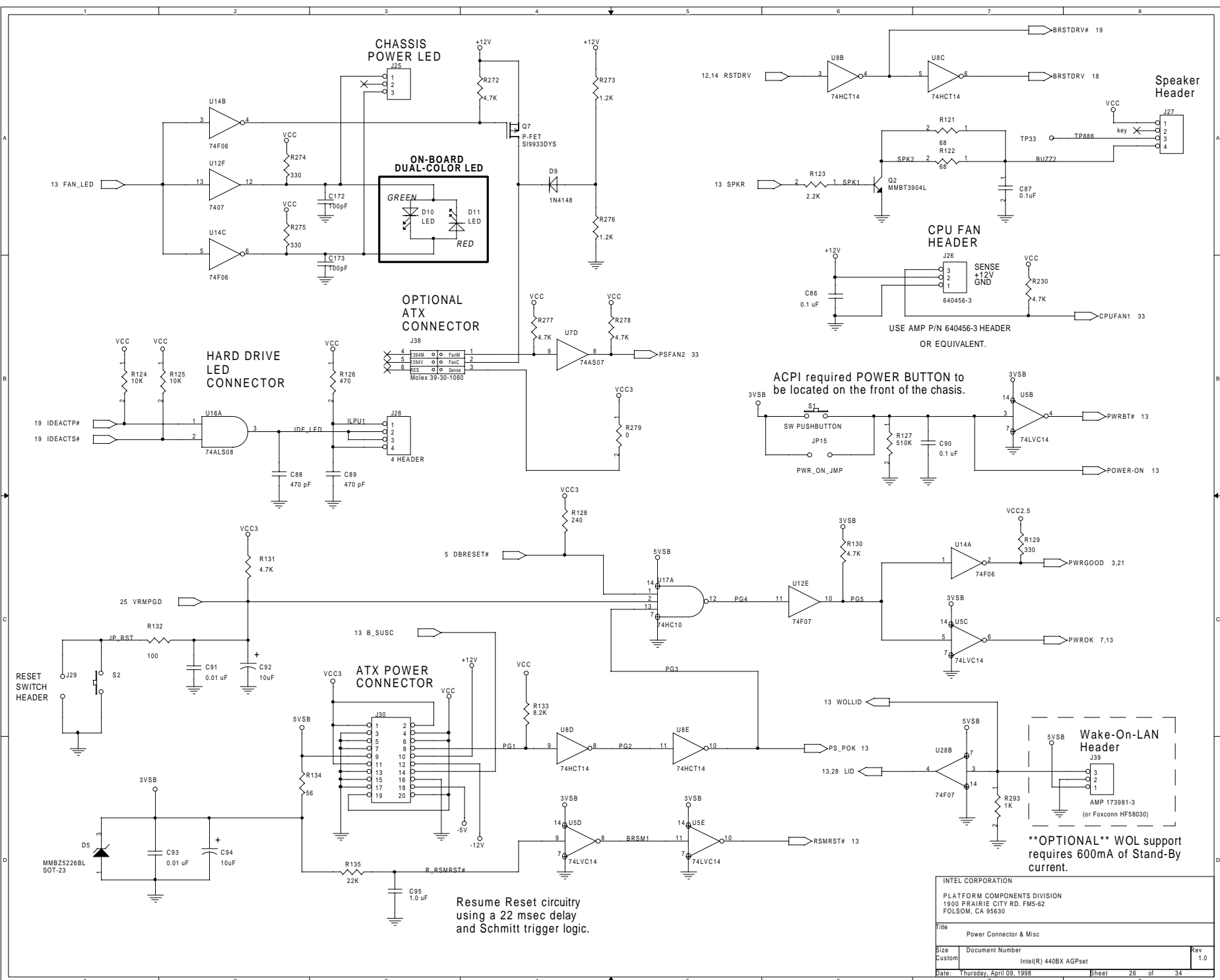
NOTE VOLTAGE REGULATOR SHOULD BE LOCATED NEAR THE 440BX

2.5V REGULATOR

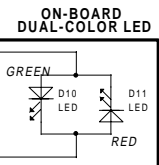


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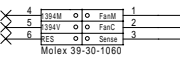
Title		DC-DC CONVERTER CONNECTORS	
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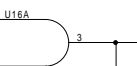
CHASSIS POWER LED



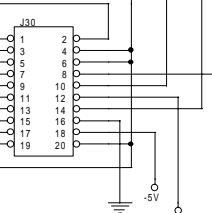
OPTIONAL ATX CONNECTOR



HARD DRIVE LED CONNECTOR

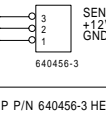


ATX POWER CONNECTOR

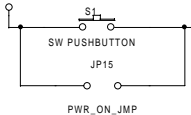


Resume Reset circuitry using a 22 msec delay and Schmitt trigger logic.

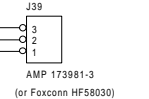
CPU FAN HEADER



ACPI required POWER BUTTON to be located on the front of the chassis.



Wake-On-LAN Header

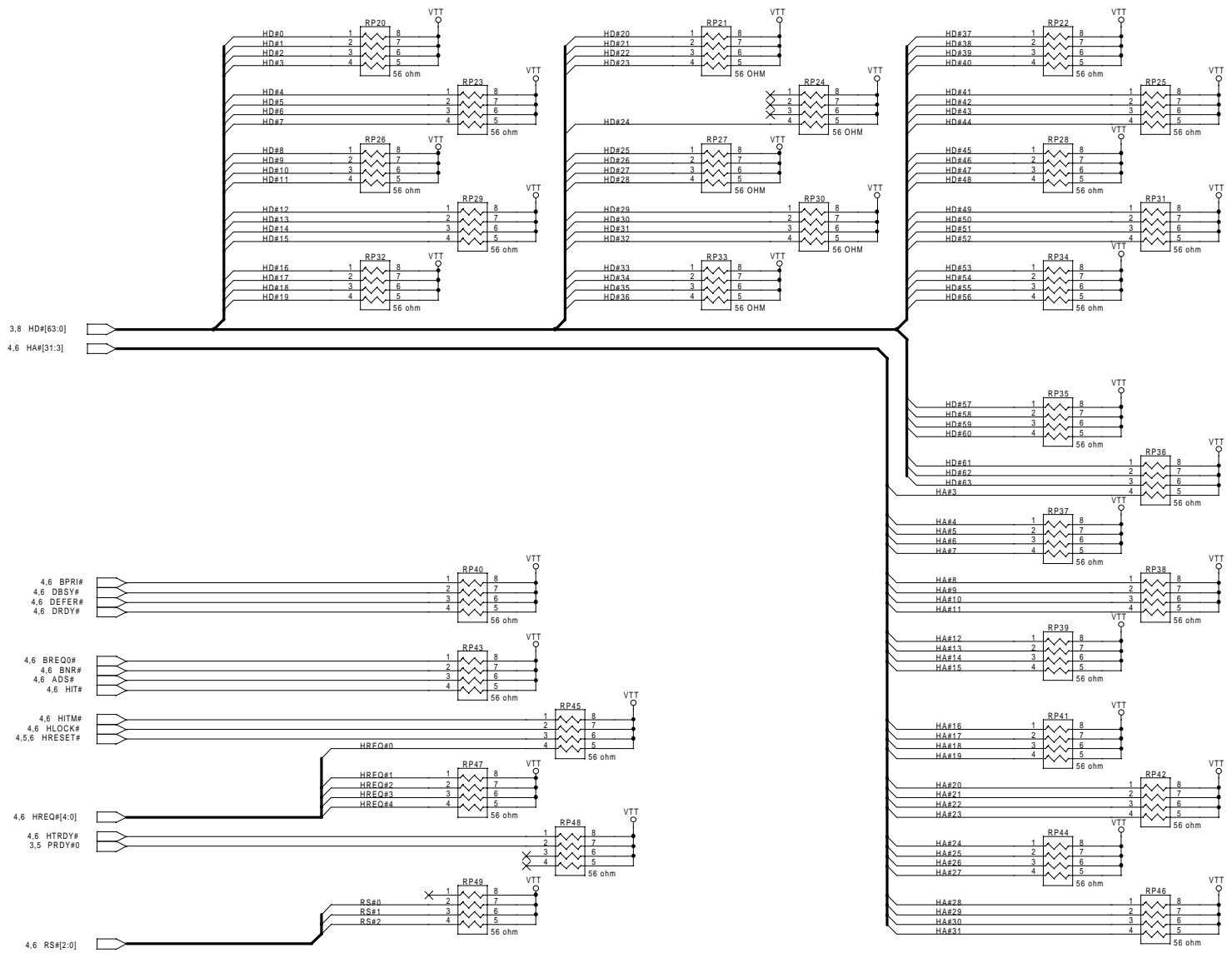


OPTIONAL WOL support requires 600mA of Stand-By current.

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GTL+ TERMINATION RESISTORS

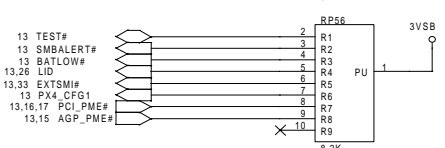
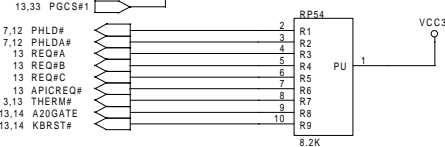
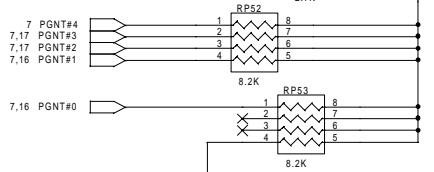
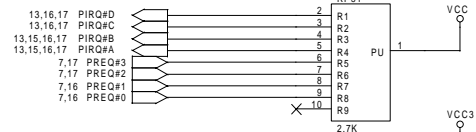
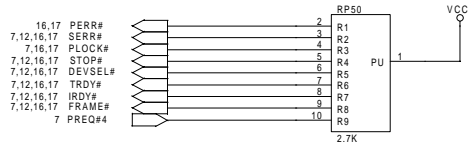
*NOTE: May be removed if route lengths can be restricted to 1.5" MIN to 4.0" MAX.



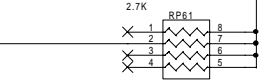
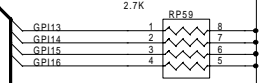
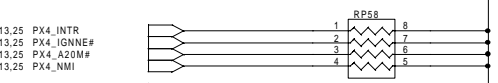
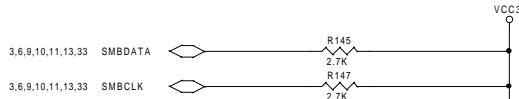
NOTE : VTT = TERMINATION VOLTAGE

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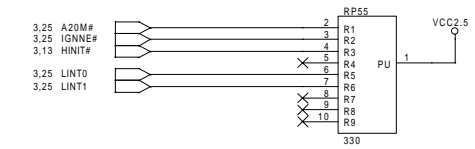
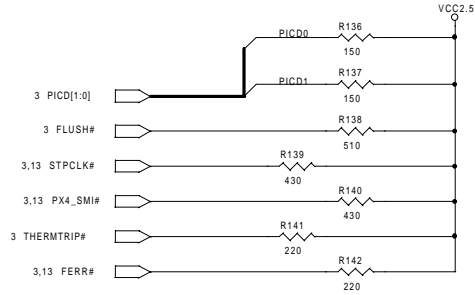
PCI BUS



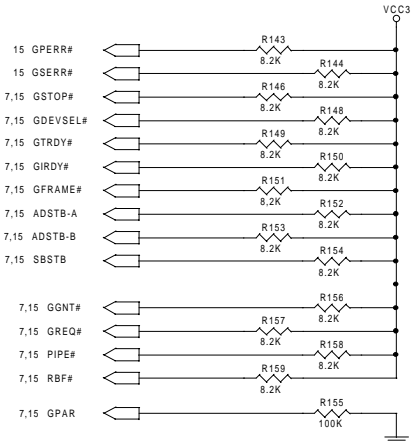
PIIX4



SLOT 1

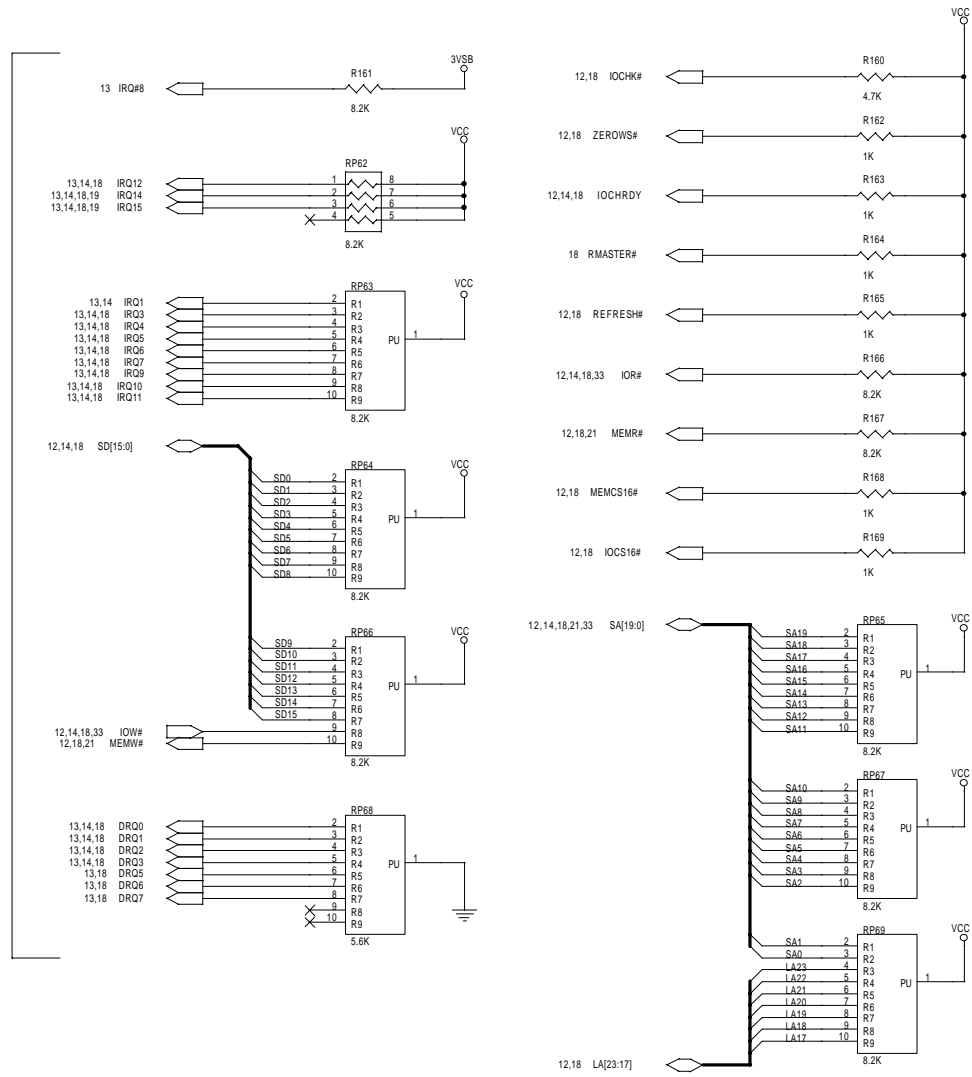


AGP

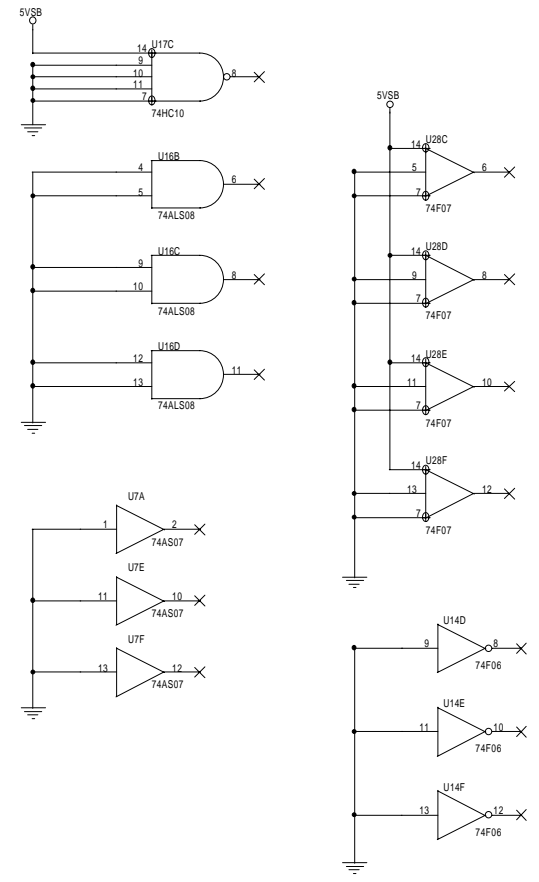


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ISA BUS

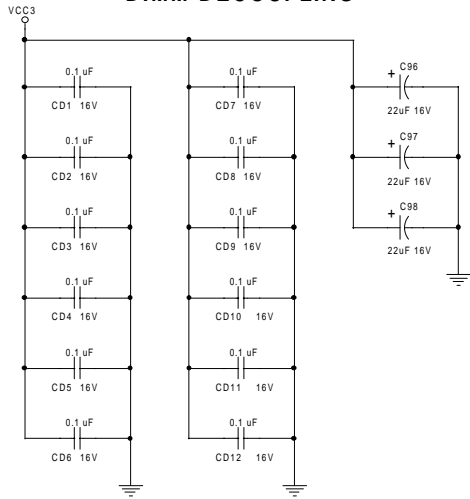


UNUSED GATES

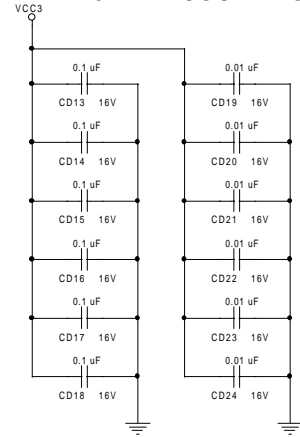


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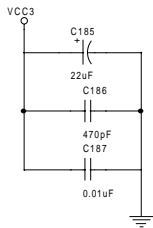
DIMM DECOUPLING



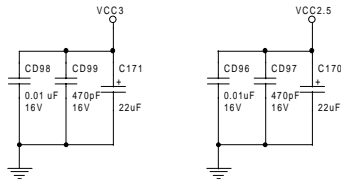
443BX DECOUPLING



CKBF DECOUPLING

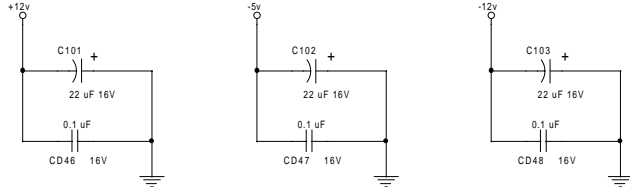
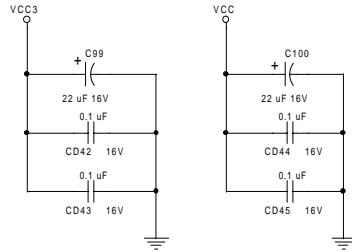


CK100 DECOUPLING

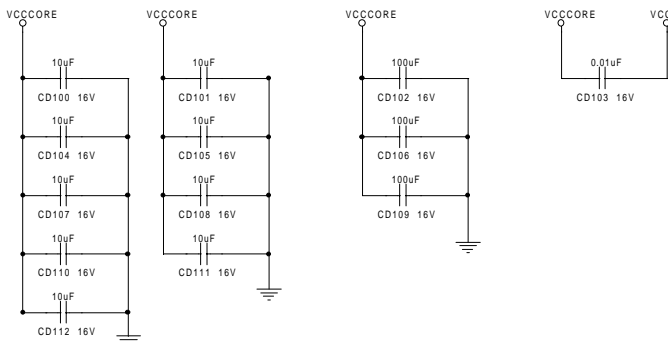


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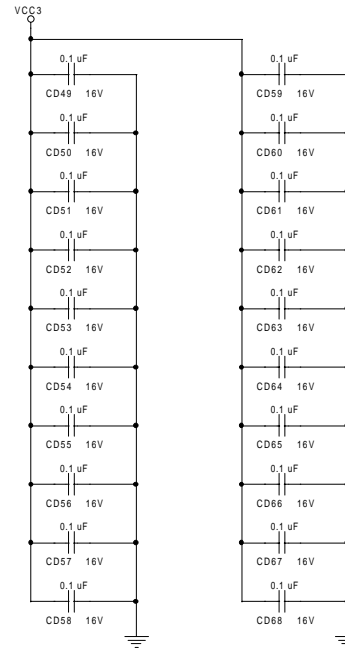
BULK POWER DECOUPLING



CORE VOLTAGE DECOUPLING

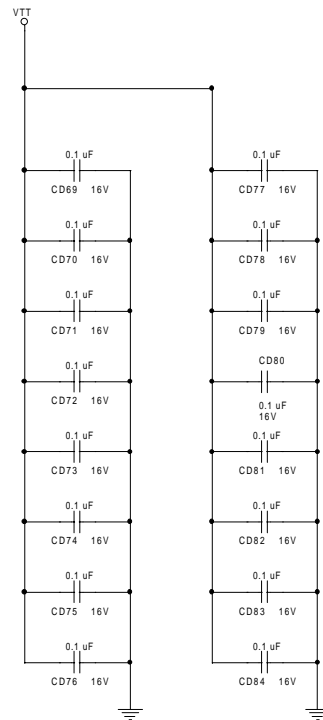


3 VOLT DECOUPLING

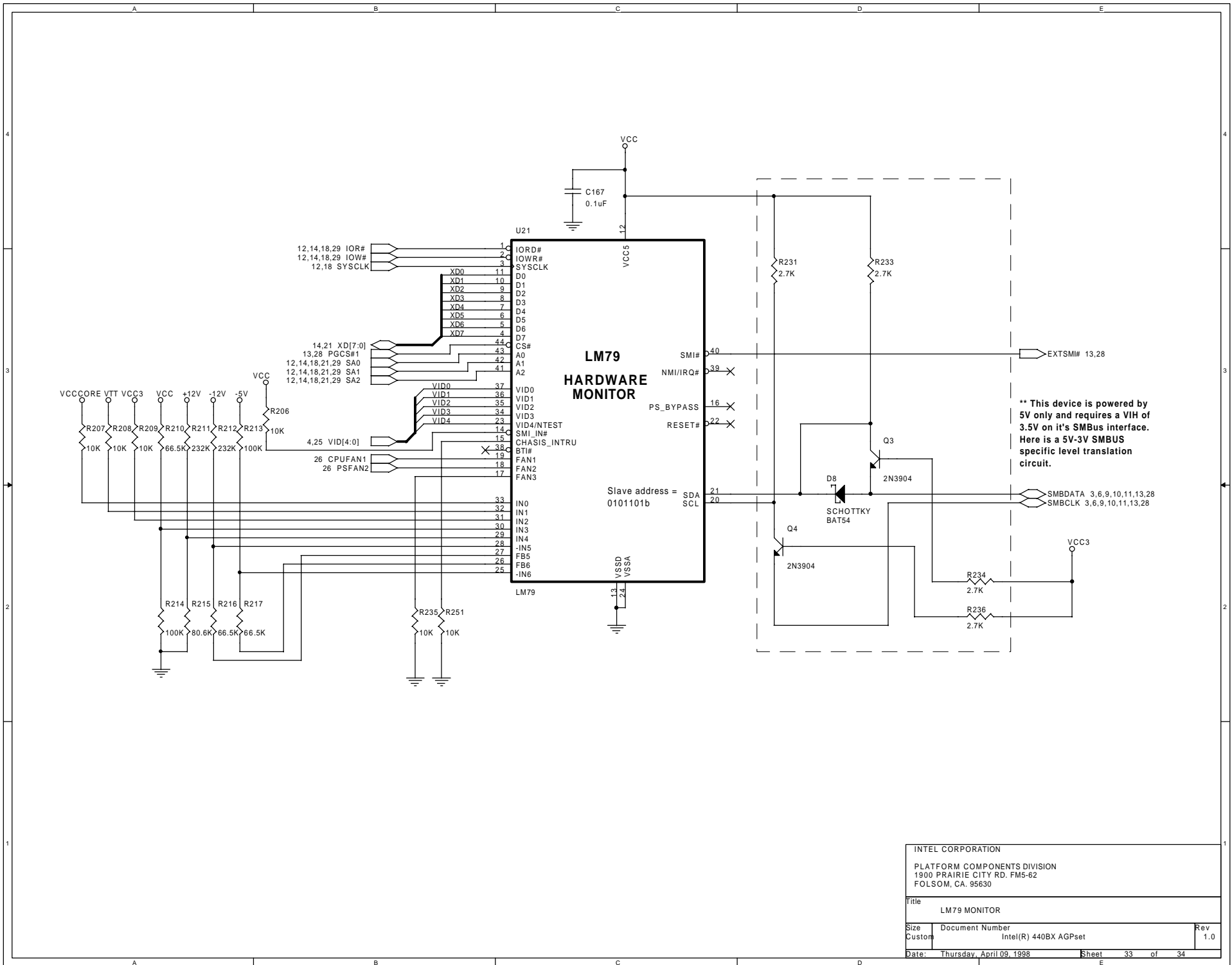


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TERMINATION VOLTAGE DECOUPLING



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