54ACT323

54ACT323 8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins



Literature Number: SNOS137

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General Description

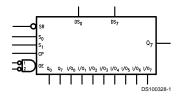
The 'ACT323 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

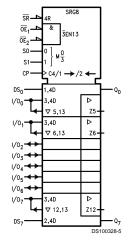
- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- TTL-compatible inputs
- Standard Military Drawing (SMD)
- 'ACT323: 5962-91607

Features

■ I_{CC} and I_{OZ} reduced by 50%

Logic Symbols

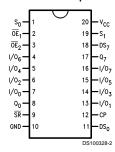




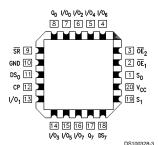
Pin Name	Description			
СР	Clock Pulse Input			
DS _o	Serial Data Input for Right Shift			
DS ₇	Serial Data Input for Left Shift			
S ₀ , S ₁	Mode Select Inputs			
SR	Synchronous Reset Input			
\overline{OE}_1 , \overline{OE}_2 $I/O_0-I/O_7$	TRI-STATE Output Enable Inputs			
I/O ₀ -I/O ₇	Multiplexed Parallel Data Inputs or			
	TRI-STATE Parallel Data Outputs			
Q ₀ , Q ₇	Serial Outputs			

Connection Diagrams

Pin Assignment for DIP and Flatpak



Pin Assignment for LCC



Functional Description

The 'ACT323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by $S_{\rm o}$ and $S_{\rm 1}$ as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. $Q_{\rm 0}$ and $Q_{\rm 7}$ are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on \overline{SR} overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either \overline{OE}_1 or \overline{OE}_2 disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
SR			СР	
L	Χ	Χ	~	Synchronous Reset; $Q_0-Q_7 = LOW$ Parallel Load; $I/O_n \rightarrow Q_n$ Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc. Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
Н	Н	Н	~	Parallel Load; I/O _n →Q _n
Н	L	Н	~	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
Н	Н	L	~	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
Н	L	L	Χ	Hold

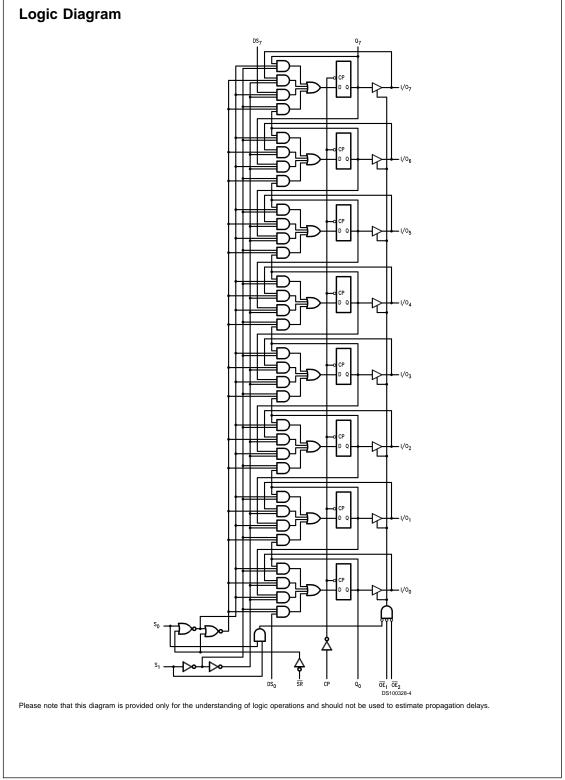
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

✓ = LOW-to-HIGH Clock Transition

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) -0.5V to +7.0V

DC Input Diode Current (IIK)

 $\begin{array}{c} \rm V_I = -0.5V & -20~mA \\ \rm V_I = V_{CC} + 0.5V & +20~mA \\ DC~Input~Voltage~(V_I) & -0.5V~to~V_{CC} + 0.5V \end{array}$

DC Output Diode Current (I_{OK})

 $V_{O} = -0.5V$ -20 mA $V_{O} = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) = -0.5V to V_{CC} + 0.5V

DC Output Source or

Sink Current (I_O) ± 50 mA

DC V_{CC} or Ground Current

Per Output Pin (I_{CC} or I_{GND}) ± 50 mA Storage Temperature (T_{STG}) -65° C to $+150^{\circ}$ C Junction Temperature (T_J)

175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})

 $\begin{tabular}{lll} 'ACT & 4.5V to 5.5V \\ Input Voltage (V_i) & 0V to V_{CC} \\ Output Voltage (V_O) & 0V to V_{CC} \\ \end{tabular}$

Operating Temperature (T_A)

54ACT -55°C to +125°C

Minimum Input Edge Rate ($\Delta V/\Delta t$)

'ACT Devices

 $\ensuremath{\text{V}_{\text{IN}}}$ from 0.8V to 2.0V

 $V_{CC} @ 4.5V, 5.5V$ 125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

DC Electrical Characteristics for 'ACT Family Devices

			54ACT		
Symbol	Parameter	V _{cc}	T _A =	Units	Conditions
		(V)	-55°C to +125°C		
			Guaranteed Limits		
V _{IH}	Minimum High Level	4.5	2.0	V	V _{OUT} = 0.1V
	Input Voltage	5.5	2.0		or V _{CC} - 0.1V
V _{IL}	Maximum Low Level	4.5	0.8	V	V _{OUT} = 0.1V
	Input Voltage	5.5	0.8		or V _{CC} - 0.1V
V _{OH}	Minimum High Level	4.5	4.4	V	I _{OUT} = -50 μA
	Output Voltage	5.5	5.4		
					(Note 2)
					$V_{IN} = V_{IL} \text{ or } V_{IH}$
		4.5	3.70	V	$I_{OH} = -24 \text{ mA}$
		5.5	4.70		I _{OH} = -24 mA
V _{OL}	Maximum Low Level	4.5	0.1	V	I _{OUT} = 50 μA
	Output Voltage	5.5	0.1		
					(Note 2)
					$V_{IN} = V_{IL} \text{ or } V_{IH}$
		4.5	0.50	V	$I_{OL} = -24 \text{ mA}$
-		5.5	0.50		$I_{OL} = -24 \text{ mA}$
I _{IN}	Maximum Input	5.5	±1.0	μA	$V_{I} = V_{CC}$, GND
	Leakage Current				
I _{OZT}	Maximum I/O	5.5	±5.5	μA	$V_{I/O} = V_{CC}$ or GND
	Leakage Current				$V_{IN} = V_{IH}, V_{IL}$
I _{CCT}	Maximum I _{CC} /Input	5.5	1.6	mA	$V_I = V_{CC} - 2.1V$
I _{OLD}	Minimum Dynamic Output	5.5	50	mA	V _{OLD} = 1.65V Max
I _{OHD}	Current (Note 3)	5.5	-50	mA	V _{OHD} = 3.85V Min
I _{cc}	Maximum Quiescent	5.5	80.0	μA	V _{IN} = V _{CC} or GND
	Supply Current				

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{CC} for 54ACT is identical to 74ACT @ 25°C.

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	Parameter		54/	Units	
		V _{cc}	T _A =		
Symbol		(V)	to +		
		(Note 5)	C _L = 50 pF		
			Min	Max	
f _{max}	Maximum Input Frequency	5.0	70		MHz
t _{PLH}	Propagation Delay	5.0	1.0	16.5	ns
	CP to Q ₀ or Q ₇				
t _{PHL}	Propagation Delay	5.0	1.0	17.0	ns
	CP to Q ₀ or Q ₇				
t _{PLH}	Propagation Delay	5.0	1.0	16.5	ns
	CP to I/O _n				
t _{PHL}	Propagation Delay	5.0	1.0	18.0	ns
	CP to I/O _n				
t _{PZH}	Output Enable Time	5.0	1.0	15.5	ns
t _{PZL}	Output Enable Time	5.0	1.0	15.5	ns
t _{PHZ}	Output Disable Time	5.0	1.0	15.5	ns
t _{PLZ}	Output Disable Time	5.0	1.0	15.0	ns

Note 5: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

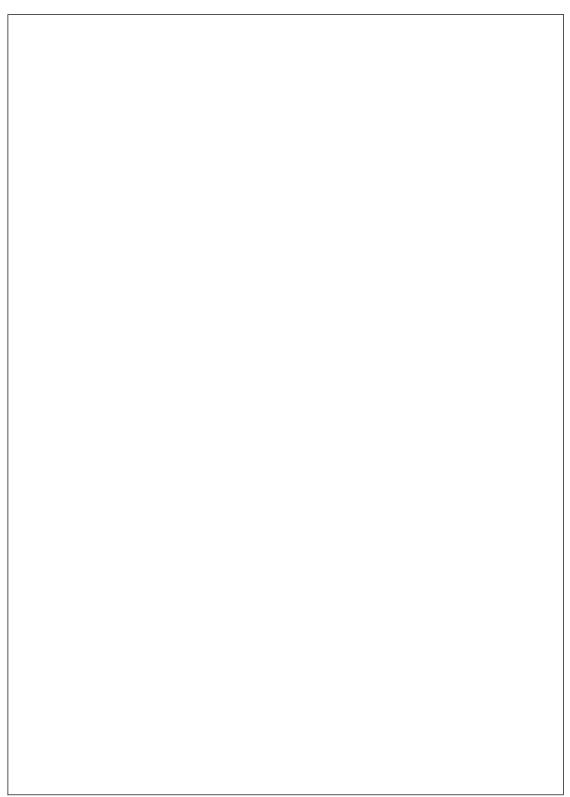
			54ACT	
			T _A = -55°C	
Symbol	Parameter	V _{cc}	to +125°C	Units
		(V)	C _L = 50 pF	
		(Note 6)	V _{CC} = +5.0V	
			Guaranteed Minimum	
t _s	Setup Time, HIGH or LOW	5.0	6.0	ns
	S₀ or S₁ to CP			
t _h	Hold Time, HIGH or LOW	5.0	2.0	ns
	S₀ or S₁ to CP			
t _s	Setup Time, HIGH or LOW	5.0	4.5	ns
	I/O _n , DS ₀ , DS ₇ to CP			
t _h	Hold Time, HIGH or LOW	5.0	2.0	ns
	I/O _n , DS ₀ , DS ₇ to CP			
t _s	Setup Time, HIGH or LOW	5.0	3.0	ns
	SR to CP			
t _h	Hold Time, HIGH or LOW	5.0	1.5	ns
	SR to CP			
t _w	CP Pulse Width	5.0	5.0	ns
	HIGH or LOW			

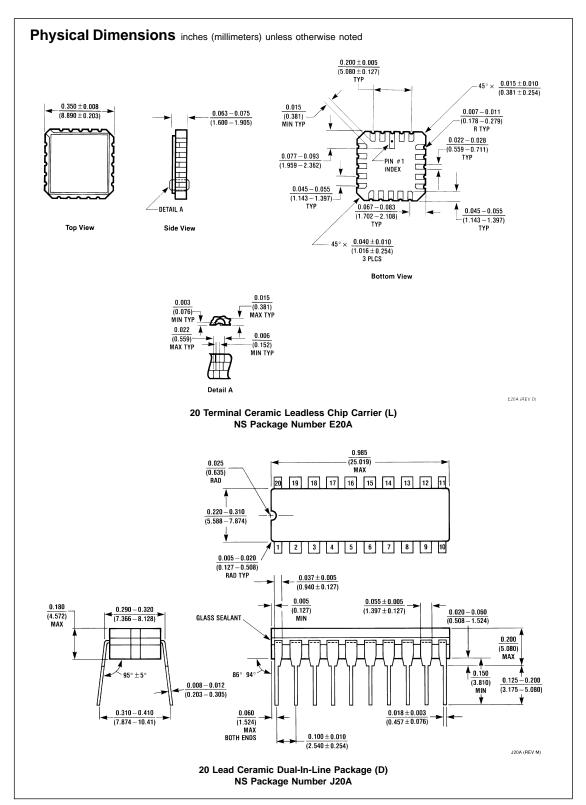
Note 6: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

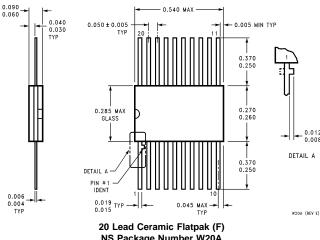
Symbol	Parameter	Тур	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	170	pF	V _{CC} = 5.0V

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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NS Package Number W20A

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www.national.com

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