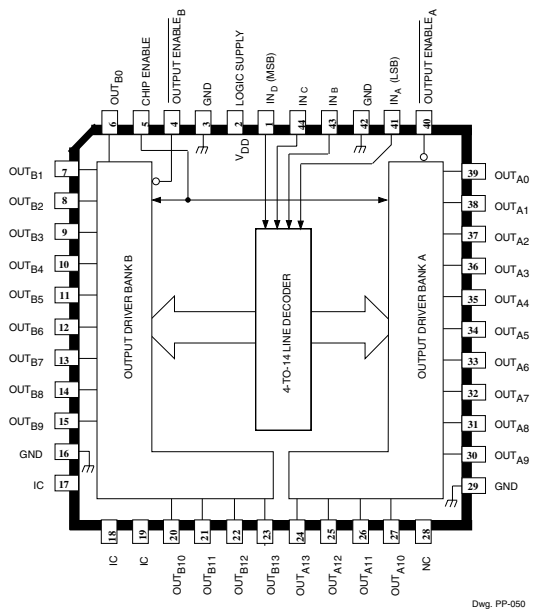
6817

Data Sheet
26186.22*

ADDRESSABLE 28-LINE DECODER/DRIVER



ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Output Voltage, V_{CE} ..... **30 V**
Logic Supply Voltage, V_{DD} ..... **7.0 V**
Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{DD} + 0.3 V**
Output Current, I_C ..... **600 mA**
Package Power Dissipation, P_D ..... **2.70 W***
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

*Derate at rate of 22 mW/°C above T_A = 25°C.

Caution: These CMOS devices have input static protection (Class 2) but are still susceptible to damage when exposed to extremely high static electrical charges.

Intended for use in ink-jet printer applications, the A6817SEP addressable 28-line decoder/driver combines low-power CMOS inputs and logic with 28 high-current, high-voltage bipolar outputs. A 4-to-14 line decoder determines the selected output driver (n) in each 14-driver bank. Two independent output-enable inputs (active low) then provide the final decoding to activate 1- or 2-of-28 outputs (OUT_{An} and/or OUT_{Bn}). Special internal circuitry is programmed at the time of manufacture to adjust the output pulse timing and thereby the energy the device delivers to the ink-jet print head. The DABiC-IV A6817SEP directly replaces the original BiMOS-II A5817SEP in most applications.

The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS logic. Use with TTL or DTL circuits may require appropriate pull-up resistors to ensure an input logic high. The internal CMOS logic operates from a 5 V supply. A CHIP ENABLE function is provided to lock out the drivers during system power up. The 28 bipolar power outputs are open-collector 30 V Darlington drivers capable of sinking 500 mA at ambient temperatures up to 85°C.

The A6817SEP is furnished in a 44-lead plastic chip carrier (quad pack) for minimum-area, surface-mount applications.

FEATURES

- Controlled Characteristics for Ink-Jet Printers
- Addressable Data Entry
- 30 V Minimum $V_{(BR)CEX}$
- CMOS, PMOS, NMOS Compatible Inputs
- Low-Power CMOS Logic

Always order by complete part number: **A6817SEP** .

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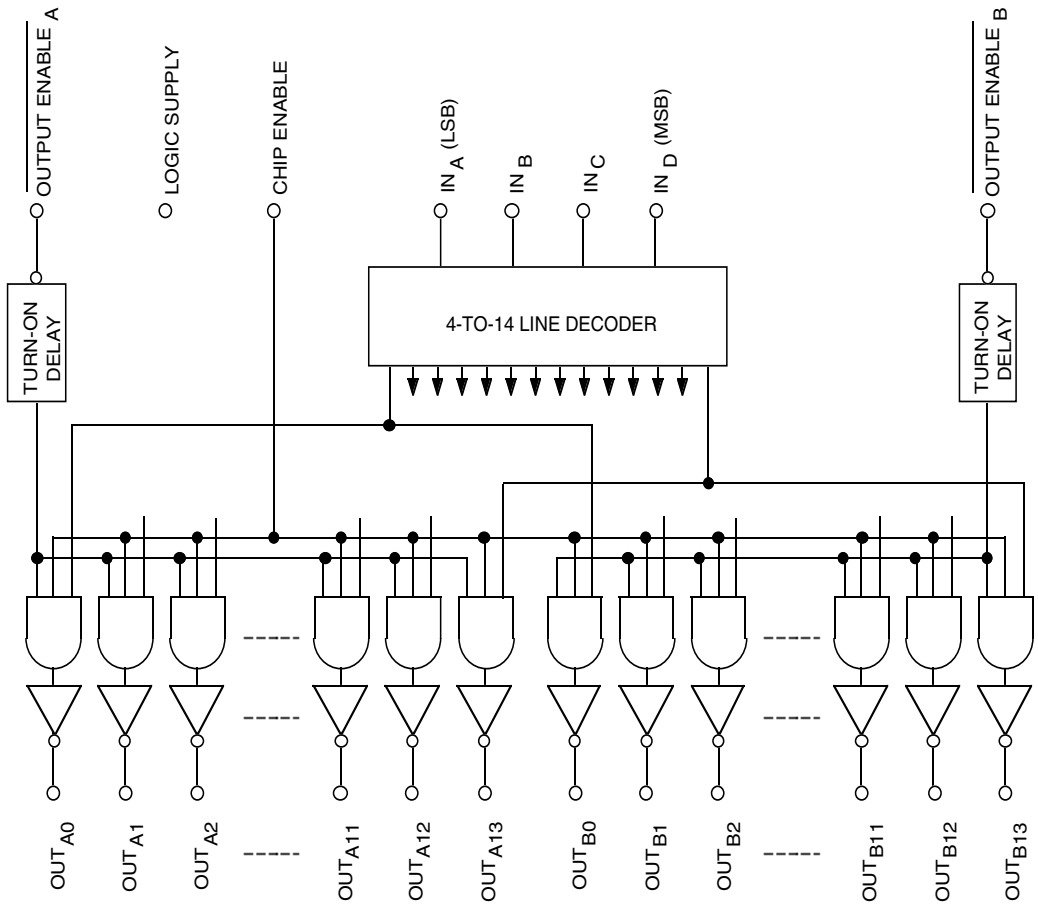
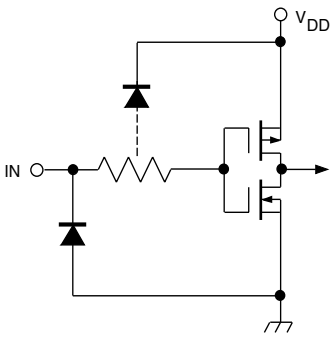
ADDRESSABLE 28-LINE DECODER/DRIVER

FUNCTIONAL BLOCK DIAGRAM



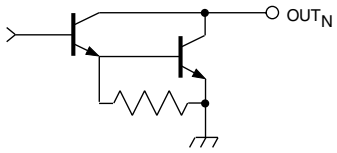
Dwg. FP-032

TYPICAL INPUT CIRCUIT



Dwg. EP-010-1

TYPICAL OUTPUT DRIVER



Dwg. EP-021-7

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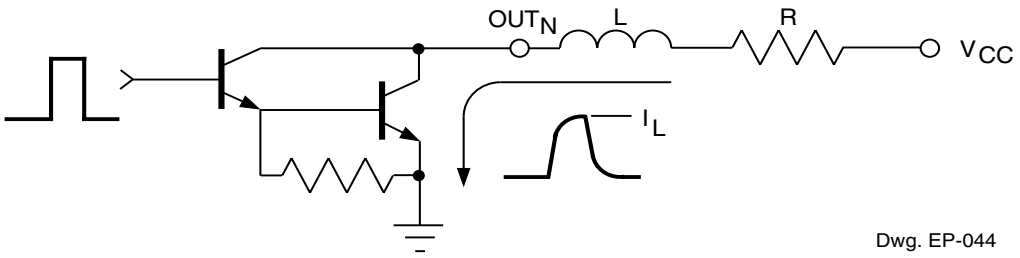
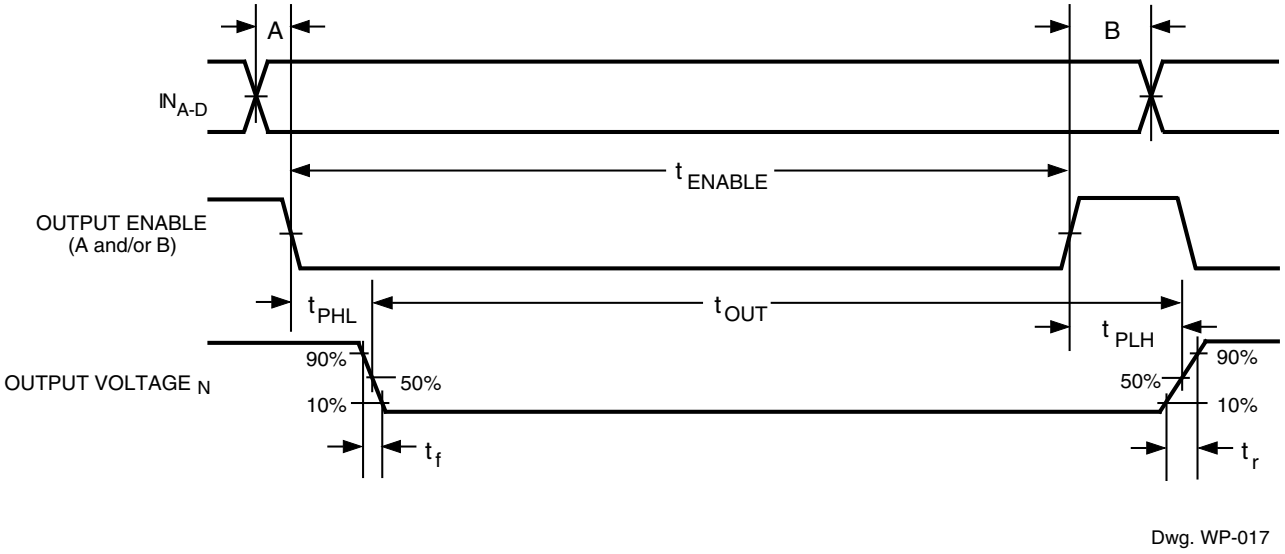
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5.0 V.

Characteristic	Symbol	Test Conditions	Limits			
			Min	Typ	Max	Units
Output Drivers						
Output Leakage Current	I_{CEX}	V_{CE} = 30 V	—	<1.0	100	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 450 mA	0.80	1.10	1.40	V
		I_{OUT} = 400 mA	0.75	1.05	1.35	V
Output Breakdown Voltage	$V_{(BR)CEX}$	R_L = 56 Ω	30	—	—	V
Unclamped Inductive Load Current	—	V_{CC} = 30 V, L = 3 µH, R_L = 56 Ω, I_L = 500 mA, Test Fig.	See Note			—
Turn-On Time	t_{PHL}	V_{CC} = 21 V, R_L = 39 Ω	25	100	425	ns
Fall Time	t_f	V_{CC} = 21 V, R_L = 39 Ω	—	20	—	ns
Turn-Off Time	t_{PLH}	V_{CC} = 21 V, R_L = 39 Ω	50	125	350	ns
Rise Time	t_r	V_{CC} = 21 V, R_L = 39 Ω	—	50	—	ns
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		3.5	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 5.0 V	—	<1.0	100	µA
	$I_{IN(0)}$	V_{IN} = 0 V	—	<-1.0	-100	µA
Input Resistance	R_{IN}		50	—	—	kΩ
Supply Current	$I_{DD(ON)}$	Two Outputs ON	—	6.0	10.0	mA
	$I_{DD(OFF)}$	All Drivers OFF, All Inputs = 0 V, OE_A = OE_B = V_{DD}	—	—	600	µA

Note: Device will turn off and meet all specifications after test.



UNCLAMPED INDUCTIVE LOAD CURRENT TEST FIGURE



TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Output Enable (Data Set-Up Time) ..... 150 ns
B. Minimum Data Hold Time After Output Enable (Data Hold Time) ..... 250 ns

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APPLICATIONS INFORMATION

This device is intended specifically for, although certainly not limited to, driving ink-jet print heads. In this application, a certain minimum energy (a function of load voltage and output pulse duration) is required for proper operation, while excessive energy will degrade the life of the print head. The output pulse duration (t_{OUT}) is equal to $t_{ENABLE} + t_{PLH} - t_{PHL}$, where t_{PHL} is adjusted during manufacture to compensate for variations in the output saturation voltage ($V_{CE(SAT)}$).

For the A6817SEP, the relationship between t_{OUT} and t_{ENABLE} at $T_A = 25°C$ is:

$$t_{OUT} = t_{ENABLE} ([V_{CE(SAT)}(\text{actual}) - V_{CE(SAT)}(\text{typical})] \times 330 \text{ ns}) + 25 \text{ ns} + 110 \text{ ns}.$$

For most applications, this will result in a driver-contribution-to-energy-error of less than ±4%.

A logic low on the CHIP ENABLE input will prevent the drivers from turning ON, regardless of the state of other inputs or the logic supply voltage. The CHIP ENABLE input has a slow response time and should not be used as a high-speed control line. For proper operation, all ground terminals should be connected to a common ground on the printed wiring board. The IC (Internal Connection) terminals are used to program the turn-on time of the device and **MUST** be left electrically unconnected (floating) for proper operation.

DECODER TRUTH TABLE

IN_D (MSB)	IN_C	IN_B	IN_A (LSB)	N
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	ALL OFF
1	1	1	1	ALL OFF

Depending on the four address inputs, the 4-to-14 line decoder selects one driver from each of the 14 output A and B banks of sink drivers according to the Decoder Truth Table. The state of the selected outputs is determined by the OUTPUT ENABLE inputs as shown in the Enable Truth Table.

ENABLE TRUTH TABLE

CHIP ENABLE	OUTPUT $ENABLE_A$	OUTPUT $ENABLE_B$	OUTPUTS (OFF unless otherwise specified. For the value of N see the Decoder Truth Table)
0	X	X	ALL OFF
1	1	1	ALL OFF
1	0	1	OUT_{AN} ON
1	1	0	OUT_{BN} ON
1	0	0	OUT_{AN} ON, OUT_{BN} ON

X = Irrelevant

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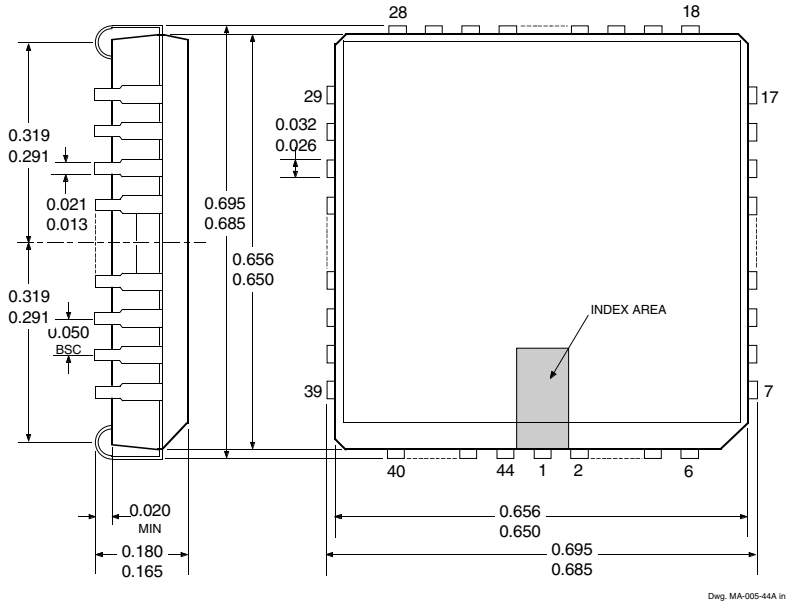
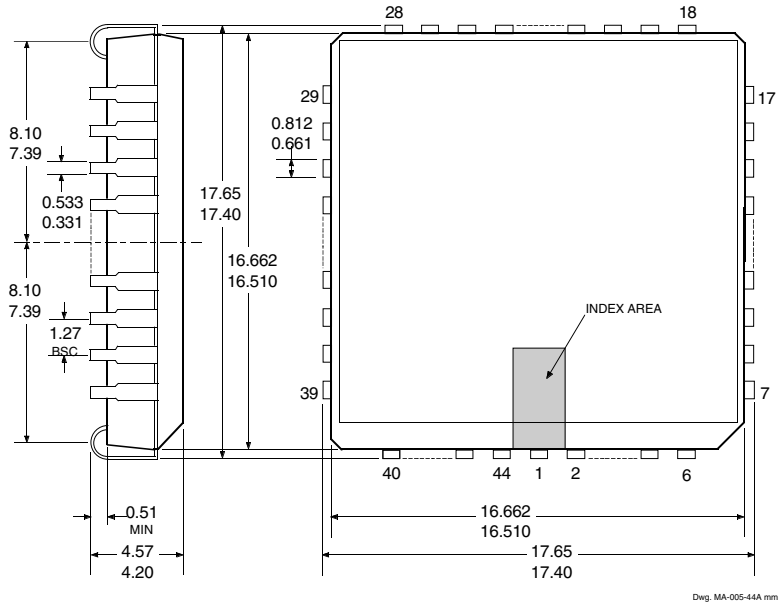
Dimensions in Inches
(for reference only)



Dimensions in Millimeters
(controlling dimensions)



NOTES:
1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 27 devices or add "TR" to part number for tape and reel.

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POWER INTERFACE DRIVERS

Function	Output Ratings*		Part Number†
SERIAL-INPUT LATCHED DRIVERS			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	80 V	5822
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
8-Bit (constant-current LED driver)	75 mA	17 V	6275
8-Bit (DMOS drivers)	250 mA	50 V	6595
8-Bit (DMOS drivers)	350 mA	50 V‡	6A595
8-Bit (DMOS drivers)	100 mA	50 V	6B595
10-Bit (active pull-downs)	-25 mA	60 V	5810-F and 6809/10
12-Bit (active pull-downs)	-25 mA	60 V	5811 and 6811
16-Bit (constant-current LED driver)	75 mA	17 V	6276
20-Bit (active pull-downs)	-25 mA	60 V	5812-F and 6812
32-Bit (active pull-downs)	-25 mA	60 V	5818-F and 6818
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
PARALLEL-INPUT LATCHED DRIVERS			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
8-Bit (DMOS drivers)	100 mA	50 V	6B273
8-Bit (DMOS drivers)	250 mA	50 V	6273
SPECIAL-PURPOSE DEVICES			
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804
Addressable 8-Bit Decoder/DMOS Driver	250 mA	50 V	6259
Addressable 8-Bit Decoder/DMOS Driver	350 mA	50 V‡	6A259
Addressable 8-Bit Decoder/DMOS Driver	100 mA	50 V	6B259
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

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