National Semiconductor

ADVANCE INFORMATION

54FCT377A/74FCT377A
Octal D Flip-Flop with Clock Enable

General Description

The FCT377A has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

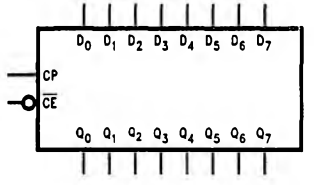
FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT377A is pin and functionally equivalent to IDT 54FCT/74FCT377A
- Ideal for addressable register applications
- Clock enables for address and data synchronization applications
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (com), 32 mA (mil)
- CMOS power levels
- ESD immunity ≥ 4 kV.
- Military product compliant to MIL-STD 883

Logic Symbols



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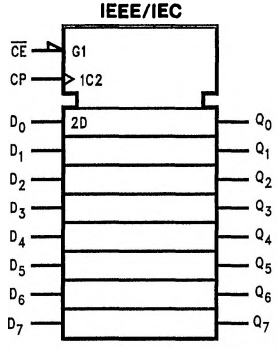

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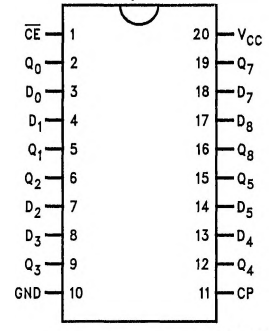
Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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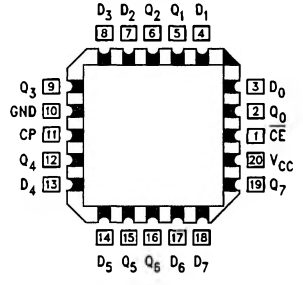
Pin Assignment for LCC



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