October 1995 Revised April 2001

FAIRCHILD

SEMICONDUCTOR

74LCX16841 Low Voltage 20-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

The LCX16841 contains twenty non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in a high impedance state.

The LCX16841 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16841 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

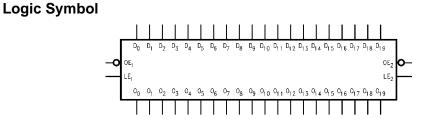
- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 5.5 ns t_{PD} max (V_{CC} = 3.3V), 20 μ A I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- \pm 24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
- Human body model > 2000V
- Machine model > 200V

Note 1: To ensure the high-impedance state during power up or down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCX16841MEA MS56A		56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
74LCX16841MTD MTD56		56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.



Pin Descriptions

Pin Names	Description
OEn	Output Enable Input (Active LOW)
LEn	Latch Enable Input
D ₀ -D ₁₉	Inputs
O ₀ -O ₁₉	Outputs

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'4LCX16841 Low Voltage 20-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

Connection Diagram

		_
οe ₁ —		56 — LE ₁
o ₀ —	2	55 0 ₀
o ₁ —	3	54 - D
GND —	4	53 — GND
02-	5	52 0 ₂
o ₃ —	6	5 1 D 3
v _{cc} —	7	50 — V _{CC}
0 ₄ —		49 0 ₄
0 ₅ —		48 0 ₅
o ₆ —		47 n ₆
GND —		46 — GND
0 ₇ —		45 0 ₇
°8 —		44 0 ₈
0 _g —		43 — D ₉
0 ₁₀ —		4 2 0 ₁₀
۹, , –		41 — D ₁₁
0 ₁₂ —		40 D ₁₂
GND —		39 — GND
0 ₁₃ —		38 — D ₁₃
0 ₁₄ —		37 — D ₁₄
0 ₁₅ —		36 — D ₁₅
v _{cc} —		35 — V _{CC}
0 ₁₆ —		34 — D ₁₆
0 ₁₇ —		33 — D ₁₇
GND —		32 — GND
с ₁₈ —		31 — D ₁₈
0 ₁₉		30 — D ₁₉
0E2 -	28	29 — LE ₂

Functional Description

The LCX16841 contains twenty D-type latches with 3-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 20-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change states each time

Truth Tables

	Inputs		Outputs
LE ₁	OE ₁	D ₀ –D ₉	0 ₀ –0 ₉
Х	Н	Х	Z
н	L	L	L
н	L	Н	н
L	L	Х	O ₀
	Inputs		Outputs
	1		
LE ₂	OE ₂	D ₁₀ –D ₁₉	O ₁₀ –O ₁₉
LE ₂ X	H	D ₁₀ –D ₁₉ Х	0 ₁₀ -0 ₁₉ Z
х	Н	Х	Z

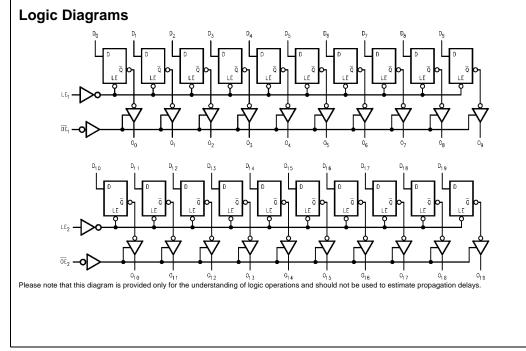
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

O₀ = Previous O₀ before HIGH-to-LOW transition of Latch Enable

its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW, the standard outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.



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Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	-0.5 to +7.0		V
VI	DC Input Voltage	-0.5 to +7.0		V
Vo	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to V _{CC} + 0.5	Output in HIGH or LOW State (Note 3)	v
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{ОК}	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	111/4
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current per Supply Pin	±100		mA
I _{GND}	DC Ground Current per Ground Pin	±100		mA
T _{STG}	Storage Temperature	-65 to +150		°C

74LCX16841

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Min	Max	Units	
V _{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	v
VI	Input Voltage		0	5.5	V
Vo	Output Voltage	HIGH or LOW State	0	V _{CC}	V
		3-STATE	0	5.5	v
I _{OH} /I _{OL}	Output Current	$V_{CC} = 3.0V - 3.6V$		±24	
		$V_{CC} = 3.0V - 3.6V$ $V_{CC} = 2.7V - 3.0V$ $V_{CC} = 2.3V - 2.7V$		±12	mA
		$V_{CC}=2.3V-2.7V$		±8	
Τ _Α	Free-Air Operating Temperature		-40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$, $V_{CC} = 3.0V$		0	10	ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_{O} Absolute Maximum Rating must be observed.

Note 4: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Cumber!	Parameter	Conditions	V_{CC} $T_{A} = -40^{\circ}C t$		to +85°C	Unit
Symbol	Parameter	Conditions	(V)	Min	Max	Unit
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		v
V _{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	- v
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100 μA	2.3 - 3.6	V _{CC} – 0.2		
		I _{OH} = -8 mA	2.3	1.8		-
		$I_{OH} = -12 \text{ mA}$	2.7	2.2		V
		I _{OH} = -18 mA	3.0	2.4		
		I _{OH} = -24 mA	3.0	2.2		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 - 3.6		0.2	
		I _{OL} = 8 mA	2.3		0.6	
		I _{OL} = 12 mA	2.7		0.4	\
		I _{OL} = 16 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
I	Input Leakage Current	$0 \le V_I \le 5.5V$	2.3 - 3.6		±5.0	μ
oz	3-STATE Output Leakage	$0 \le V_O \le 5.5V$	2.3 - 3.6		±5.0	μ
		$V_I = V_{IH} \text{ or } V_{IL}$	2.5 - 5.0		±3.0	μ
OFF	Power-Off Leakage Current	$V_1 \text{ or } V_0 = 5.5 \text{ V}$	0		10	μ

74LCX16841

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	v _{cc}	T _A = -40°	C to +85°C	Units
Cymbol	i alameter	Conditions	(V)	Min	Max	Onits
I _{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		20	μA
		$3.6V \le V_I, V_O \le 5.5V$ (Note 5)	2.3 – 3.6		±20	μΛ
ΔI_{CC}	Increase in I _{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3 - 3.6		500	μΑ

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

			T _A	= -40°C to +	85°C, R _L = 5	00 Ω		
Symbol	Parameter	V _{CC} = 3.	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$		$V_{CC}=\textbf{2.5V}\pm\textbf{0.2V}$		Units	
Symbol	T al allietter	C _L =			C _L = 50 pF		C _L = 30 pF	
tour		Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.5	5.5	1.5	6.0	1.5	6.6	ns
t _{PLH}	D _n to O _n	1.5	5.5	1.5	6.0	1.5	6.6	115
t _{PHL}	Propagation Delay	1.5	5.5	1.5	6.5	1.5	6.6	ns
t _{PLH}	LE to O _n	1.5	5.5	1.5	6.5	1.5	6.6	115
t _{PZL}	Output Enable Time	1.5	6.5	1.5	7.0	1.5	8.5	ns
t _{PZH}		1.5	6.5	1.5	7.0	1.5	8.5	115
t _{PLZ}	Output Disable Time	1.5	6.5	1.5	7.0	1.5	7.8	ns
t _{PHZ}		1.5	6.5	1.5	7.0	1.5	7.8	115
t _{OSHL}	Output to Output Skew (Note 6)		1.0					ns
t _{OSLH}			1.0					115
t _S	Setup Time, D _n to LE	2.5		2.5		3.0		ns
t _H	Hold Time, D _n to LE	1.5		1.5		2.0		ns
t _W	LE Pulse Width	3.3	1	3.3		3.8		ns

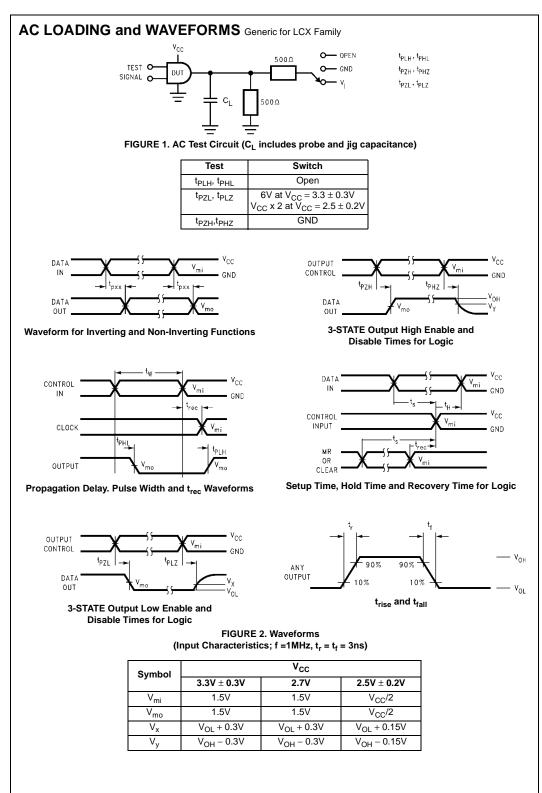
Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{cc}	$T_A = 25^{\circ}C$	Units
Cymbol	Tarameter	Conditions	(V)	Typical	onita
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	$C_{L} = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	3.3	0.8	V
		$C_L=30 \text{ pF}, V_{IH}=2.5 \text{V}, V_{IL}=0 \text{V}$	2.5	0.6	v
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	3.3	-0.8	V
		$C_L = 30 \text{ pF}, \text{ V}_{IH} = 2.5 \text{V}, \text{ V}_{IL} = 0 \text{V}$	2.5	-0.6	v

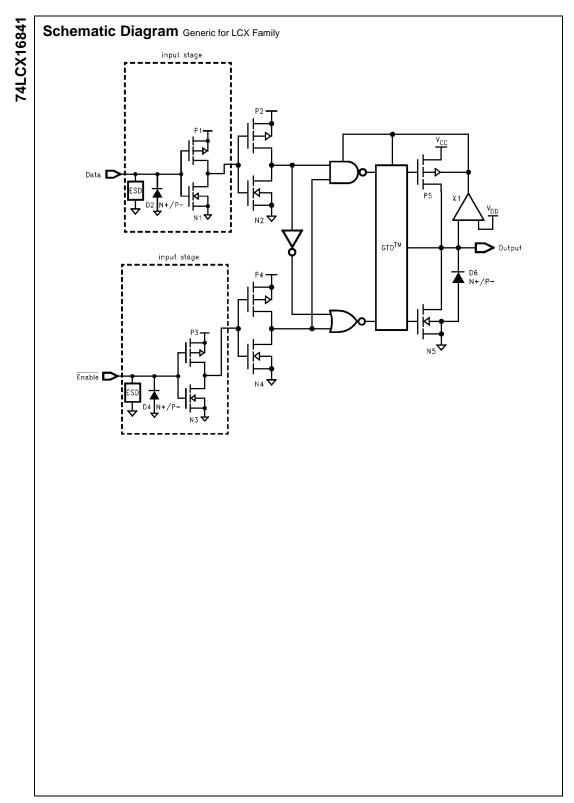
Capacitance

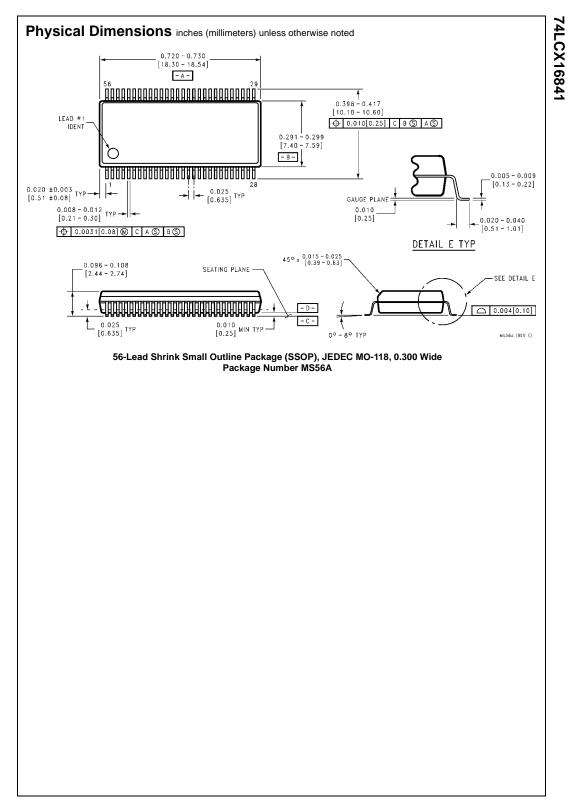
Symbol	Parameter	Conditions	Typical	Units
CIN	Input Capacitance	$V_{CC} = Open, V_I = 0V \text{ or } V_{CC}$	7	pF
Co	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC} , f = 10 MHz	20	pF

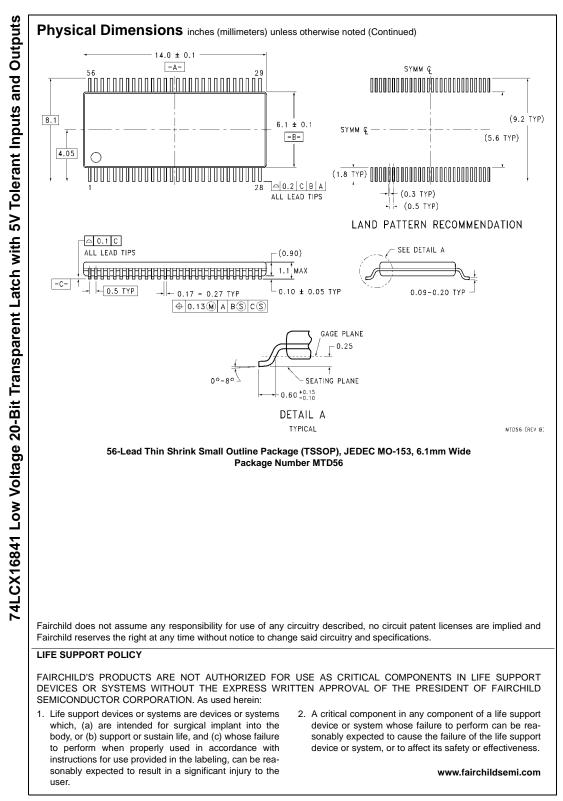


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