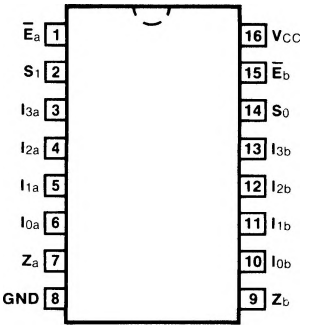
54/74153
54S/74S153
54LS/74LS153

DUAL 4-INPUT MULTIPLEXER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '153 is a high speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the '153 can generate any two functions of three variables.

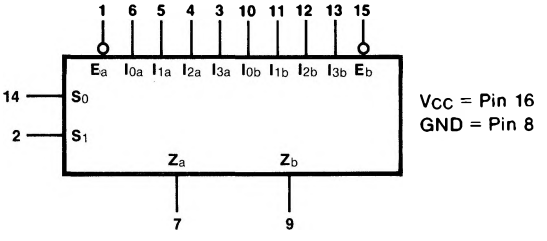
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	74153PC, 74S153PC 74LS153PC		9B
Ceramic DIP (D)	A	74153DC, 74S153DC 74LS153DC	54153DM, 54S153DM 53LS153DM	6B
Flatpak (F)	A	74153FC, 74S153FC 74LS153FC	54153FM, 54S153FM 54LS153FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
I_{0a} — I_{3a}	Side A Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
I_{0b} — I_{3b}	Side B Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
S_0, S_1	Common Select Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{E}_a$	Side A Enable Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{E}_b$	Side B Enable Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
Z_a	Side A Output	20/10	25/12.5	10/5.0 (2.5)
Z_b	Side B Output	20/10	25/12.5	10/5.0 (2.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The '153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The '153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$
$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

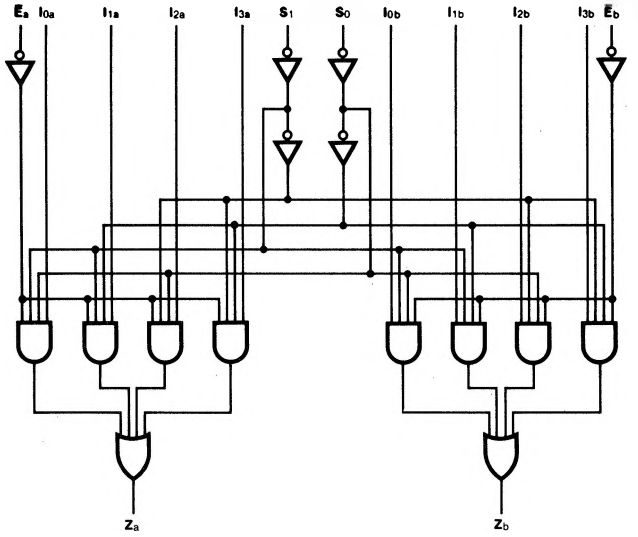
The '153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is a function generator. The '153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74		54/74S		54/74LS		UNITS	CONDITIONS
			Min	Max	Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	XM	-20	-55	-40	-100	-20	-100	mA	V_{CC} = Max
		XC	-18	-57	-40	-100	-20	-100		
I_{CC}	Power Supply Current	XM		52		70		10	mA	V_{CC} = Max
		XC		60		70		10		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configuration)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 30 pF, R_L = 400 Ω		C_L = 15 pF, R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n		34 34		18 18		29 29	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n		30 23		15 13.5		29 32	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n		18 23		9.0 9.0		15 20	ns	Figs. 3-1, 3-5