# BINARY HEXADECIMAL AND BCD DECADE, SYNCHRONOUS UP/DOWN COUNTERS 

## DESCRIPTION

The Up/Down Counter is a monolithic MSI circuit containing gates and binaries interconnected to provide a bidirectional divide-by-ten (decade) or divide-by-sixteen (hexadecimal) result as a function of the clock input.
The output code of the decade up/down counter is the commonly used BCD (8421) code, and the output sequence generated is the binary equivalent of the decimal numbers 0 through 9.

The hexadecimal up/down counter provides the output sequence 0 through 15 which is presented in a weighted binary code (8421).
Set and Reset on the binary elements provide asynchronous entry with respect to the clock line, causing a count of " 0 " or " 15 " (8284) or of " 0 " or " 9 " (8285), and also inhibit propagation of count enable data.

DIGITAL 8000 SERIES TTL/MSI

Entry and propagation of data is performed in a synchronous manner with the clock line, which is active on its negative going excursion. The input from a previous stage or other source is channeled through "Carry $\ln ^{\prime \prime}$ and its propagation can be inhibited by the "Count Enable" line. "Carry In" and "Count Enable" input duality gives added flexibility in multiple package cascading applications.

Direction of the counter is steered from a single line (Up/ $\overline{D o w n}$ ), where a " 0 " level will cause a "down" count and a " 1 " level will accomplish an "up" count.

All Q outputs of the four binaries are brought to the outside world, together with the $\overline{\mathrm{Q}}$ output of the most significant binary (O4) and the Carry Out.

## LOGIC DIAGRAMS


( ) = Denotes Pin Numbers
(8285)

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

| CHARACTERISTICS | LIMITS |  |  |  | TEST CONDITIONS |  |  |  |  |  |  | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | TYP. | MAX. | UNITS | SET | RESET | UP/DOWN | $\begin{aligned} & \text { COUNT } \\ & \text { ENABLE } \end{aligned}$ | CLOCK | CARRY IN | OUTPUTS |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{Q}_{1}, \mathrm{Q}_{4}$, Carry Out | 2.6 |  |  | V | 0.8 V | 2.0 V | 2.0 V |  |  | 2.0 V | -800 $\mu \mathrm{A}$ |  |
| $\mathrm{Q}_{2}, \mathrm{Q}_{3},(8284)$ |  |  |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{a}_{2}, \mathrm{Q}_{3}(8285)$ | 2.6 |  |  | $v$ | Pulse |  | 0.8 V |  |  | , | $-800 \mu \mathrm{~A}$ |  |
| Q4 | 2.6 |  |  | V | 2.0 V | 0.8 V |  |  |  |  | $-800 \mu \mathrm{~A}$ |  |
| " 0 ' Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Carry Out |  |  | 0.4 | $v$ | 2.0 V | 0.8V |  |  |  | 0.8V | 9.6 mA |  |
| $\overline{\mathrm{Q}}_{4}$ |  |  | 0.4 | V | 0.8 V | 2.0 V |  |  |  |  | 9.6 mA |  |
| "1" Input Current |  |  |  |  |  |  |  |  |  |  |  |  |
| Carry In |  |  | 120 | $\mu \mathrm{A}$ | Pulse |  | 5.0 V |  |  | 4.5V |  |  |
| Set |  |  | 200 | $\mu \mathrm{A}$ | 4.5V | Pulse |  |  |  |  |  |  |
| Reset |  |  | 40 | $\mu \mathrm{A}$ | Pulse | 4.5V |  |  |  |  |  |  |
| Count Enable |  |  | 40 | $\mu \mathrm{A}$ |  |  |  | 4.5 V |  |  |  |  |
| Clock and Up/Down |  |  | 40 | $\mu \mathrm{A}$ |  |  | 4.5 V |  | 4.5 V |  |  |  |
| "0'0 Input Current |  |  |  |  |  |  |  |  |  |  |  |  |
| Carry In |  |  | 3.2 | mA | Pulse |  | OV |  |  | 0.4 V |  |  |
| Set |  |  | 6.4 | mA | 0.4V |  |  |  |  |  |  |  |
| Reset |  |  | 6.4 | mA |  | 0.4V | . |  |  |  |  |  |
| Count Enable |  |  | 1.6 | mA |  |  |  | 0.4V |  |  |  |  |
| Clock |  |  | 1.6 | mA |  |  |  |  | 0.4 V |  |  |  |
| Up/Down |  |  | 1.6 | mA |  |  | 0.4V |  |  |  |  |  |
| Input Latch Voltage |  |  |  |  |  |  |  |  |  |  |  |  |
| Carry In | 5.5 |  |  | V |  | OV | 5.0 V | OV |  | 10 mA |  |  |
| Reset | 5.5 |  |  | V |  | 10 mA |  | OV |  | OV |  |  |
| Set | 5.5 |  |  | V | 10 mA |  |  | OV |  | OV |  |  |
| Count Enable | 5.5 |  |  | V | OV |  |  | 10 mA |  | OV |  |  |
| Up/Down | 5.5 |  |  | V |  |  | 10 mA |  |  |  |  |  |
| Output Short Circuit |  |  |  |  |  |  |  |  |  |  |  |  |
| Current | -20 |  | -70 | mA |  |  |  |  |  |  | OV |  |

$\mathrm{T}_{\mathrm{A}}=\mathbf{2 5}{ }^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$

| CHARACTERISTICS | LIMITS |  |  |  | TEST CONDITIONS |  |  |  |  |  |  | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | TYP. | MAX. | UNITS | SET | RESET | UP/DOWN | COUNT ENABLE | CLOCK | CARRY IN | OUTPUTS |  |
| Power Consumption |  | 315 | 420 | mW |  |  |  |  |  |  |  | 12 |
| Propagation Delay |  |  |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{t}_{\text {on }}$ Clock to $\mathrm{Q}_{4}$ \& $\overline{\mathrm{O}}_{\mathbf{4}}$ |  | 32 | 45 | ns |  |  |  |  |  |  |  | 7 |
| $t_{\text {on }}$ Clock to $\mathrm{Q}_{1}, \mathrm{Q}_{2}, \mathrm{Q}_{3}$ |  | 28 | 40 | ns |  |  |  |  |  |  |  | 7 |
| $t_{\text {off }} \text { Clock to } Q_{n}, \bar{\alpha}_{n}$ |  | 25 | 35 | ns |  |  |  |  |  |  |  | 7 |
| $t_{\text {on }}$ Reset to $Q_{n}$ |  | 24 | 35 | ns |  |  |  |  |  |  |  | 7 |
| $t_{\text {off }}$ Set to $Q_{n}$ |  | 15 | 25 | ns |  |  |  |  |  |  |  | 7 |
| ${ }^{\text {ton }}$ Reset to $\overline{\mathrm{Q}}_{\mathrm{n}}$ |  | 32 | 45 | ns |  |  |  |  |  |  |  | 7 |
| $t_{\text {on }}$ Carry In to Carry Out |  | 15 | 25 | ns |  |  |  |  |  |  |  | 7 |
| $t_{\text {off }}$ Carry In to Carry Out |  | 20 | 30 | ns |  |  |  |  |  |  |  | 7 |
| Clock Min. "1" Interval | 20 | 15 |  | ns |  |  |  |  |  |  |  | 7 |
| Count Rate | 20 | 30 |  | MHz |  |  |  |  |  |  |  |  |
| Carry In, Count Enable, |  |  |  |  |  |  |  | 4 |  |  |  |  |
| \& Up/Down Set-Up Time |  | 15 | 25 | ns |  |  |  |  |  |  |  |  |
| Carry In, Count Enable |  |  |  |  |  |  |  |  |  |  |  |  |
| \& Up/Down Hold Time |  | 0 | 2 | ns |  |  |  |  |  |  |  |  |
| Set/Reset Pulse Width |  | 20 | 25 | ns |  |  |  |  |  |  |  |  |

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current is defined as into the terminal referenced.
4. Positive NAND Logic Definition:
"UP" Level $=" 1 "$, "DOWN" Level $=" 0 "$.
5. Output source current is supplied through a resistor to ground.
6. Output sink current is supplied through a resistor to $\mathrm{V}_{\mathrm{CC}}$
7. Refer to $A C$ Test Figure.
8. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. Connect $Q_{4}$ to count enable, set the counter (1001), and count down. The counter will halt at BCD-7 (0111).
11. Pulse is normally at +4.0 volts, falling to 0 volts for at least 100 nsec.
12. $V_{C C}=5.25$ volts.

## AC TEST FIGURES AND WAVEFORMS



AC TEST FIGURES AND WAVEFORMS (Cont'd)


CARRY IN/CARRY OUT ( $t_{\text {on }}$ and $t_{\text {off }}$ )


Carry in pulse
Pulse amplitude $=2.6 \mathrm{~V}$
Pulse width $(0)=50 \mathrm{~ns}$
Frequency $=10 \mathrm{MHz}$
$t_{r}=t_{f}=5 n$ at $10 \%$ to $90 \%$ points

TYPICAL APPLICATIONS


