REFER TO PAGE 18 FOR A, F AND O PACKAGE PIN CONFIGURATIONS.

## DESCRIPTION

The 8292 Decade Counter and 8293 Binary Counter are low power devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8292 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8293 Binary Counter may be connected as a divide-bytwo, four, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state, A " 1 "
or " 0 " at a data input will be transferred to the associated output when the strobe input is put at the " 0 " level. For additional flexibility, both units are provided with a reset input which is common to all four bits. A " 0 " on the reset line produces " 0 " at all four outputs.
The counting operation is performed on the falling (negativegoing) edge of the input clock pulse.

Triggering requirements are compatible with any of the 8000 Series elements.

The various counter arrangements, as well as additional applications suggestions may be found in the Signetics handbook "DESIGNING WITH MSI." Counters and Shift Registers, Volumn I.

LOGIC DIAGRAMS AND TRUTH TABLES


ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

| CHARACTERISTICS | LIMITS |  |  |  | TEST CONDITIONS |  |  |  |  |  | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | TYP. | MAX. | UNITS | DATA STROBE | DATA INPUTS | RESET | CLOCK | $\underset{2}{\text { CLOCK }}$ | OUTPUTS |  |
| "1" Output Voltage | 2.6 | 3.5 |  | $v$ | 0.8 V | 2.0 V | 2.0 V |  | ${ }^{\text {A OUT }}$ | $-100 \mu \mathrm{~A}$ | 6,8 |
| " 0 " Output Voltage |  |  | 0.4 | v | 0.8 V | 0.8V | 0.8 V |  | AOUT | 3.2 mA | 6,9 |
| '00' Input Current |  |  |  |  |  |  |  |  |  |  |  |
| Data Strobe | -0.1 |  | -0.4 | mA | 0.4 V |  | 5.25 V |  |  |  |  |
| Data Inputs | -0.1 |  | -0.4 | mA |  | 0.4V |  |  |  |  |  |
| Reset | -0.1 |  | -0.6 | mA | 5.25 V |  | 0.4V |  |  |  |  |
| Clock 1 | -0.1 |  | -0.6 | mA | 5.25 V |  |  | 0.4V |  |  |  |
| Clock 2 (8292) | -0.1 |  | -1.2 | mA | 5.25 V |  |  |  | 0.4V |  |  |
| Clock 2 (8293) | -0.1 |  | -0.6 | mA | 5.25 V |  |  |  | 0.4V |  |  |
| " 1 " Input Current |  |  |  |  |  |  |  |  |  |  |  |
| Data Strobe |  |  | 20 | $\mu \mathrm{A}$ | 4.5 V |  | 0.0V |  |  |  |  |
| Data Inputs |  |  | 20 | $\mu \mathrm{A}$ |  | 4.5 V |  |  |  |  |  |
| Reset |  |  | 40 | $\mu \mathrm{A}$ | 0.0V |  | 4.5 V |  |  |  |  |
| Clock 1 |  |  | 40 | $\mu \mathrm{A}$ | 0.0V |  |  | 4.5 V |  |  |  |
| Clock 2 (8292) |  |  | 80 | $\mu \mathrm{A}$ | 0.0V |  |  |  | 4.5 V |  |  |
| Clock 2 (8293) |  |  | 40 | $\mu \mathrm{A}$ | 0.0V |  |  |  | 4.5 V |  |  |
| Output Short Circuit Current | -5 |  | -45 | mA | 0.0V |  |  |  |  | 0.0V | 7 |
| Input Voltage Rating |  |  |  |  |  |  |  |  |  |  |  |
| Data Strobe |  |  |  |  | 10 mA |  |  |  |  |  |  |
| Clock 1 and 2 | 5.5 |  |  | $v$ |  |  |  | 10 mA | 10 mA |  |  |
| . Data Inputs | 5.5 |  |  | v |  | 10 mA |  |  |  |  |  |
| Reset | 5.5 |  |  | v |  |  | 10 mA |  |  |  |  |

$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$

| CHARACTERISTICS | LIMITS |  |  |  | TEST CONDITIONS |  |  |  |  |  | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN. | TYP. | MAX. | UNITS | DATA STROBE | DATA INPUTS | RESET | CLOCK | $\underset{2}{\text { CLOCK }}$ | OUTPUTS |  |
| Power/Current Consumption |  | 52.51 | 69/ | mw/ |  |  | 0.0V | 0.0V | 0.0V |  | 13 |
|  |  | 10 | 13.1 | mA |  |  |  |  |  |  |  |
| Clock Mode $\mathrm{t}_{\text {on }}$ Delay (All Bits) |  | 37 | 55 | ns |  |  |  |  |  |  | 10 |
| Clock Mode $t_{\text {off }}$ Delay (All Bits) |  | 32 | 55 | ns |  |  |  |  |  |  | 10 |
| Strobed Data ton Delay (All Bits) |  | 80 | 100 | ns |  |  |  |  |  |  | 10 |
| Strobed Data toff Delay (All Bits) |  | 80 | 100 | ns |  |  |  |  |  |  | 10 |
| Clock Mode Switching Test |  |  | 75 | ns |  |  |  |  |  |  | 12 |
| Strobe Pulse Width |  | 60 | 75 | ns |  | 0.8 V | 2.0 V | 2.0 V | ${ }^{\text {A OUT }}$ |  |  |
| Reset Pulse Width |  | 45 | 60 | ns |  | 2.0 V | 2.0 V | 2.0 V | AOUT |  |  |
| Strobe/Reset Release Time |  | 80 |  | ns |  |  |  |  | ${ }^{\text {A OUT }}$ |  |  |
| Toggle Rate | 5 | 10 |  | MHz |  |  |  |  |  |  |  |

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic Definition:
"UP" Level $=" 1 "$, "DOWN" Level $=" 0 "$.
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each output and the associated data input independently.
7. Not more than one output should be shorted at a time.
8. Output source current is supplied through a resistor to ground.
9. Output sink current is supplied through a resistor to $\mathrm{V}_{\mathrm{CC}}$.
10. Refer to AC Test Figure.
11. Manufacturer reserves the right to make design and process changes and improvements.
12. This test guarantees the device will reliably trigger on a pulse with a 75 ns fall-time or less.
13. $\quad V_{C C}=5.25$ volts.

## AC TEST FIGURES AND WAVEFORMS

## CLOCK MODE $\mathbf{t o n}^{\prime} / \mathrm{t}_{\text {off }}$ DELAY



NOTE:
INPUT PULSE:
Amplitude $=2.6 \mathrm{~V}$
P.W. $=30$ ns, $50 \%$ to $50 \%$
$t_{r}=t_{f}=5 \mathrm{~ns}$
$P R R=1 \mathrm{MHz}$

1. $t_{0 n}$ and $t_{\text {off }}$ are measured from the clock input of each binary to the $\mathbf{O}$ output of that binary.

STROBED DATA $\mathrm{t}_{\mathrm{on}} / \mathrm{t}_{\text {off }}$ DELAY


Strobe,
P.A. $=2.6 \mathrm{~V}$
P.W. $=300$ ns, 50\% to 50\%

PRR $=1 \mathrm{MHz}$
$\mathbf{t}_{\mathbf{r}}=\mathbf{t}_{\mathrm{f}}=\mathbf{5 n s}$

Data,
P.A. $=2.6 \mathrm{~V}$
P.W. $=500 \mathrm{~ns}, 50 \%$ to 50\%

PRR $=500 \mathrm{KHz}$
$\mathbf{t}_{\mathbf{r}}=\mathbf{t}_{\mathbf{f}}=\mathbf{5 n s}$

AC TEST FIGURES AND WAVEFORMS (Cont'd)

## CLOCK MODE SWITCHING TEST



INPUT PULSE:
Amplitude $=3.4 \mathrm{~V}$
P.W. $=100 \mathrm{~ns}, 50 \%$ to $50 \%$
$\mathrm{PRR}=2.5 \mathrm{MHz}$
$\mathrm{t}_{\mathrm{r}}=20 \mathrm{~ns}$
$t_{f}=75 \mathrm{~ns}$


MINIMUM STROBE PULSE WIDTH


INPUT PULSE:
Amplitude $=2.6 \mathrm{~V}$
$t_{r}=t_{f}=5 n s$ max.

## AC TEST FIGURES AND WAVEFORMS (Cont'd)

## MINIMUM RESET PULSE WIDTH



OUTPUTS OUTPUTS
A,B,C,D

## INPUT PULSE:

Amplitude 2.6V
$\mathbf{t}_{\mathbf{r}}=\mathbf{t}_{\mathbf{f}}=5 \mathrm{~ns}$ max.
NOTE: Outputs must be previously brought high by placing a "Q" on the D strobe input. A pulse generator mav be substituted for the switch.

TOGGLE RATE


INPUT PULSE:
Amplitude $=2.6 \mathrm{~V}$
$P R R=5 \mathrm{MHz}, 50 \%$ duty cycle
$\mathbf{t}_{\mathbf{r}}=\mathbf{t}_{\mathbf{f}}=5 \mathrm{~ns}$ max.

## AC TEST FIGURES AND WAVEFORMS (Cont'd)



NOTES:

1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent, $f=1 \mathrm{MHz}, V_{\text {ac }}=25 \mathrm{mV}_{\mathrm{rms}}$.
3. All diodes are 1N916.
