

DESCRIPTION

The 82S180 and 82S181 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S180 and 82S181 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

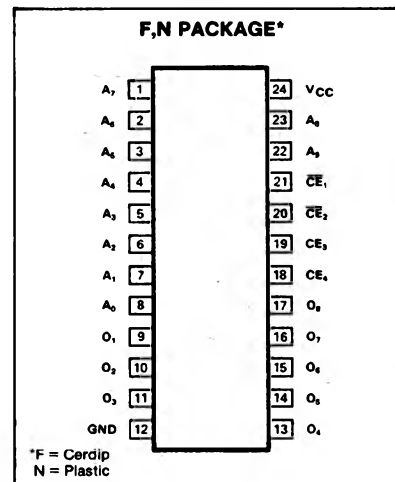
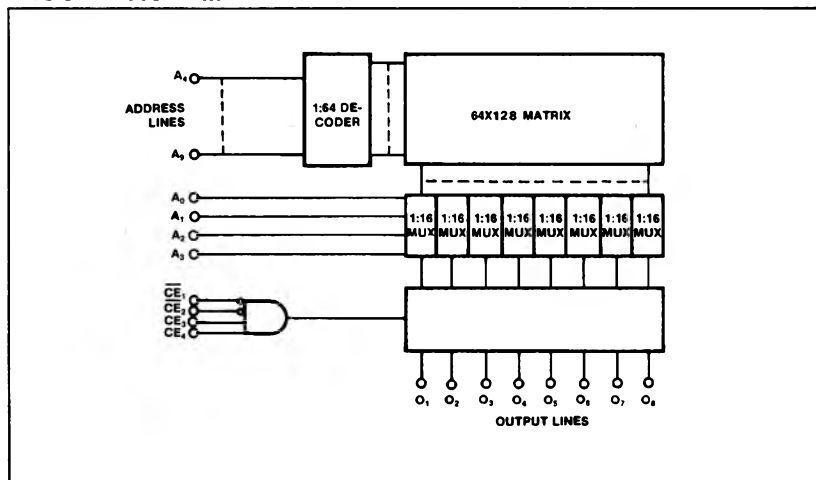
The 82S180 and 82S181 are available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S180/181, F or N, and for the military temperature range (-55°C to +125°C) specify S82S180/181, F.

FEATURES

- **Address access time:**
N82S180/181: 70ns max
S82S180/181: 90ns max
- **Power dissipation:** 85μW/bit typ
- **Input loading:**
N82S180/181: -100μA max
S82S180/181: -150μA max
- **On-chip address decoding**
- **Output options:**
82S180: Open collector
82S181: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION**BLOCK DIAGRAM****ABSOLUTE MAXIMUM RATINGS**

PARAMETER		RATING	UNIT
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
V _{OH}	Output voltage		Vdc
V _O	High (82S180)	+5.5	
	Off-state (82S181)	+5.5	
T _A	Temperature range		°C
	Operating		
	N82S180/181	0 to +75	
	S82S180/181	-55 to +125	
T _{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS N82S180/181: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82S180/181: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TEST CONDITIONS ¹	N82S180/181			S82S180/181			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp	2.0	-0.8	.85	2.0	-0.8	.80	V
				-1.2			-1.2	
V _{OL} V _{OH}	Output voltage Low High (82S181)	2.4		0.45	2.4		0.5	V
I _{IL} I _{IH}	Input current Low High			-100			-150	μA
				40			50	
I _{OLK}	Output current Leakage (82S180)			40			60	μA
I _{O(OFF)}	Hi-Z state (82S181)			-40			-60	μA
				40			60	μA
I _{OS}	Short circuit (82S181)			-70			-85	mA
I _{CC}	V _{CC} supply current		140	175		140	185	mA
C _{IN} C _{OUT}	Capacitance Input Output		5 8			5 8		pF

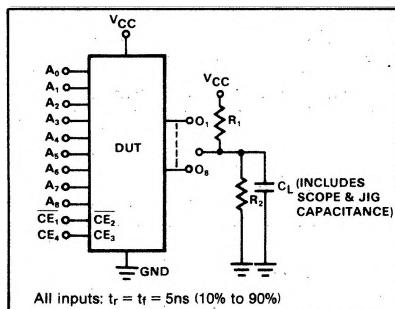
AC ELECTRICAL CHARACTERISTICS R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82S180/181: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82S180/181: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TO	FROM	N82S180/181			S82S180/181			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
T _{AA} T _{CE}	Access time Output	Address Chip enable		50 20	70 40		50 20	90 50	ns
T _{CD}	Disable time Output	Chip disable		20	40		20	50	ns

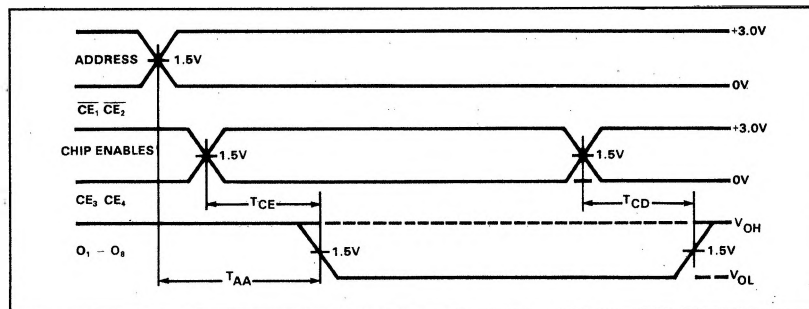
NOTES

- Positive current is defined as into the terminal referenced.
- Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM

PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{CCP} Power supply voltage To program ¹	$I_{CCP} = 375 \pm 75\text{mA}$, Transient or steady state	8.5	8.75	9.0	V
V_{CCH} Verify limit Upper		5.3	5.5	5.7	V
V_{CCL} Lower		4.3	4.5	4.7	V
V_S Verify threshold ²		1.4	1.5	1.6	V
I_{CCP} Programming supply current	$V_{CCP} = +8.75 \pm .25\text{V}$	300		450	mA
V_{IH} Input voltage High		2.4		5.5	V
V_{IL} Low		0	0.4	0.8	V
I_{IH} Input current High	$V_{IH} = +5.5\text{V}$			50	μA
I_{IL} Low	$V_{IL} = +0.4\text{V}$			-500	
V_{OUT} Output programming voltage ³	$I_{OUT} = 200 \pm 20\text{mA}$, Transient or steady state	16.0	17.0	18.0	V
I_{OUT} Output programming current	$V_{OUT} = +17 \pm 1\text{V}$	180	200	220	mA
T_R Output pulse rise time		10		50	μs
t_p CE programming pulse width		0.3	0.4	0.5	ms
t_D Pulse sequence delay		10			μs
T_{PR} Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PSI} Initial programming pause	$V_{CC} = 0\text{V}$	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$ Programming duty cycle ⁴				50	%
FL Fusing attempts per link				2	cycle

NOTES

1. Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the $17 \pm 1\text{V}$ output voltage is maintained during the entire fusing cycle.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a $10k\Omega$ resistor to V_{CC} . Apply \overline{CE}_1 = High, \overline{CE}_2 = Low, \overline{CE}_3 = High and \overline{CE}_4 = High.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$.
3. After $10\mu s$ delay, apply $V_{OUT} = +17 \pm 1V$ to the output to be programmed. Program one output at the time.
4. After $10\mu s$ delay, pulse the \overline{CE}_1 input to logic low for 0.3 to 0.5ms.
5. After $10\mu s$ delay, remove $+17V$ from the programmed output.
6. To verify programming, after $10\mu s$ delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic low level to the \overline{CE}_1 input. The programmed output should remain in the high state. Again, lower V_{CC} to $V_{CCL} =$
7. $+4.5 \pm .2V$, and verify that the programmed output remains in the high state.
8. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$, and repeat steps 3 through 6 to program other bits at the same address.
9. After $10\mu s$ delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE