82S27-F

DESCRIPTION

The 82S27 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S27 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The device includes on-chip decoding, 2 chip enable inputs, and open collector outputs for ease of memory expansion.

The 82S27 is available in the commercial temperature range (0°C to +75°C) and is specified as N82S27, F.

FEATURES

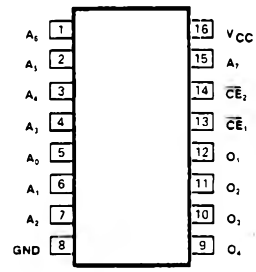
- **Address access time: 40ns max**
- **Power dissipation: 0.6mW/bit typ**
- **Input loading: 1.6mA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

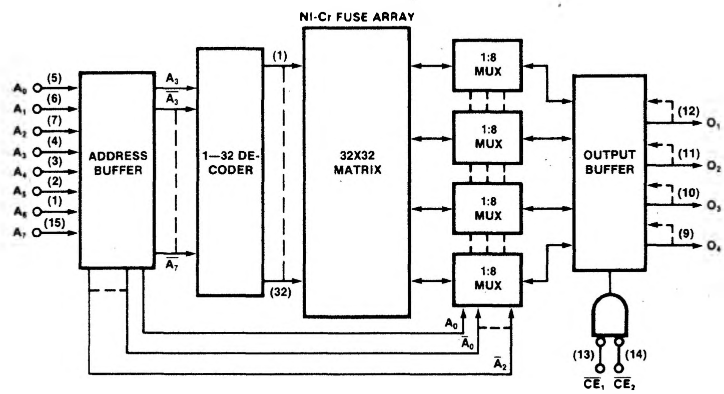
PIN CONFIGURATION

F PACKAGE*



*F = Cerdip

BLOCK DIAGRAM



Vcc = (16)
GND = (8)
( ) = Pin number

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

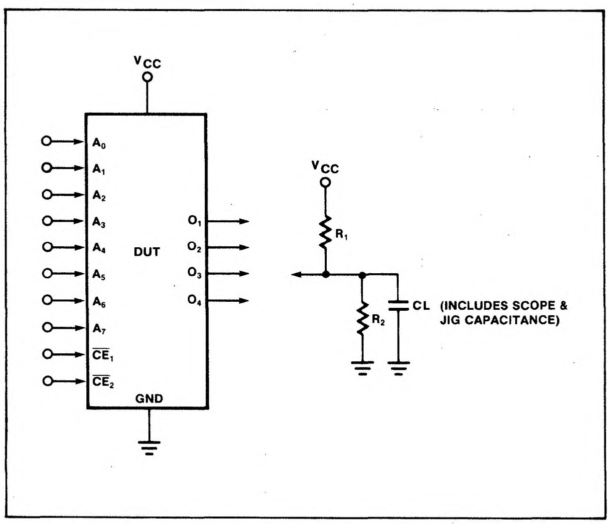
PARAMETER		TEST CONDITIONS[1]	LIMITS Min	Typ[2]	Max	UNIT
	Input voltage					V
V_{IL}	Low				.80	
V_{IH}	High		2.0			
V_{IC}	Clamp	I_{IN} = -12mA		-1.0	-1.5	
	Output voltage					V
V_{OL}	Low	I_{OUT} = 32mA		0.45	0.50	
	Input current					
I_{IL}	Low	V_{IN} = 0.50V			-1.6	mA
I_{IH}	High	V_{IN} = 2.4V			40	μA
		V_{IN} = 5.5V			1	mA
	Output current					μA
I_{OLK}	Leakage	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			100	
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V, $\overline{CE}_1$ or $\overline{CE}_2$ = High		8		

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$, $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$

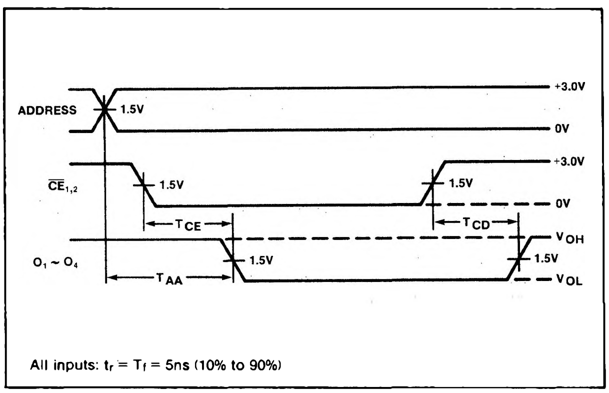
PARAMETER		TO	FROM	LIMITS Min	Typ[2]	Max	UNIT
	Access time						ns
T_{AA}		Output	Address		30	40	
T_{CE}		Output	Chip enable		15	20	
	Disable time						ns
T_{CD}		Output	Chip disable		15	20	

NOTES
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEMS SPECIFICATIONS

(Testing of these limits may cause programming of device.) $T_A = +25°C$

	PARAMETER	TEST CONDITIONS	LIMITS Min	Typ	Max	UNIT
	Power supply voltage					V
V_{CCP}	To program[1]	$I_{CCP} = 300 \pm 50mA$, Transient or steady state	5.0		5.25	
	Verify limit					V
V_{CCH}	Upper		5.0	5.25	5.5	
V_{CCL}	Lower		4.5	4.75	5.0	
V_S	Verify threshold[2]		0.9	1.0	1.1	V
	Input voltage					V
V_{IH}	High (except $\overline{CE}_1$)		3.0		5.0	
V_{IL}	Low		0	0.4	0.5	
V_{IN}	Program level ($\overline{CE}_1$ only)		14.0	14.5	15.0	
	Input current					
I_{IH}	High	$V_{IH} = +3.0V$			100	μA
I_{IL}	Low	$V_{IL} = +0.5V$			-1.6	mA
I_{IN}	Program level ($\overline{CE}_1$ only)	$V_{IN} = +15.0V$			15	mA
V_{OUT}	Output programming voltage[3]	$I_{OUT} = 115 \pm 10mA$, Transient or steady state	16.5	17.0	17.5	V
I_{OUT}	Output programming current	$V_{OUT} = +17.0 \pm 0.5V$	105	115	125	mA
T_R	Output pulse rise time[4]		0.2		0.5	μs
t_p	Programming pulse width		0.25		0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PS}	Programming pause	$V_{CC} = 0V$	6			sec
$\frac{T_{PR}}{T_{PR} + T_{PS}}$	Programming duty cycle[5]			50		%

NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 0.5V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. Measured with a 1K dummy load connected across the fusing source.
5. Continuous fusing for an unlimited time is also allowed, provided that a 50% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a rest period (V_{CC} = 0V) of 0.5ms.

PROGRAMMING PROCEDURE

The 82S27 is shipped with all bits at logical low. To write logical high, proceed as follows:

Set-up

1. Apply GND to pin 12.
2. Terminate all device outputs with a 10kΩ resistor to V_{CC}.
3. Set $\overline{CE}_2$ to logic low.

Program-Verify Sequence

1. Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL high and low logic levels to the device address inputs.
2. After 10μs delay, apply to $\overline{CE}_1$ (pin 13) a voltage source of 14.5 ± 0.5V, with 15mA sourcing current capability.
3. After 10μs delay, apply a voltage source of +17.0 ± 0.5V to the output to be programmed. The source must have a current limit of 115mA. Prgram one output at the time.
4. After 10μs delay, remove +17.0V supply from programmed output.
5. To verify programming, after 10μs delay, return $\overline{CE}_1$ to 0V. Raise V_{CC} to V_{CCH} = +5.25 ± .25V. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.75 ± .25V, and verify that the programmed output remains in the high state.
6. Raise V_{CC} to V_{CCP}, and repeat steps 2 through 5 to program other bits at the same address.
7. Repeat steps 1 through 6 to program all other address locations.

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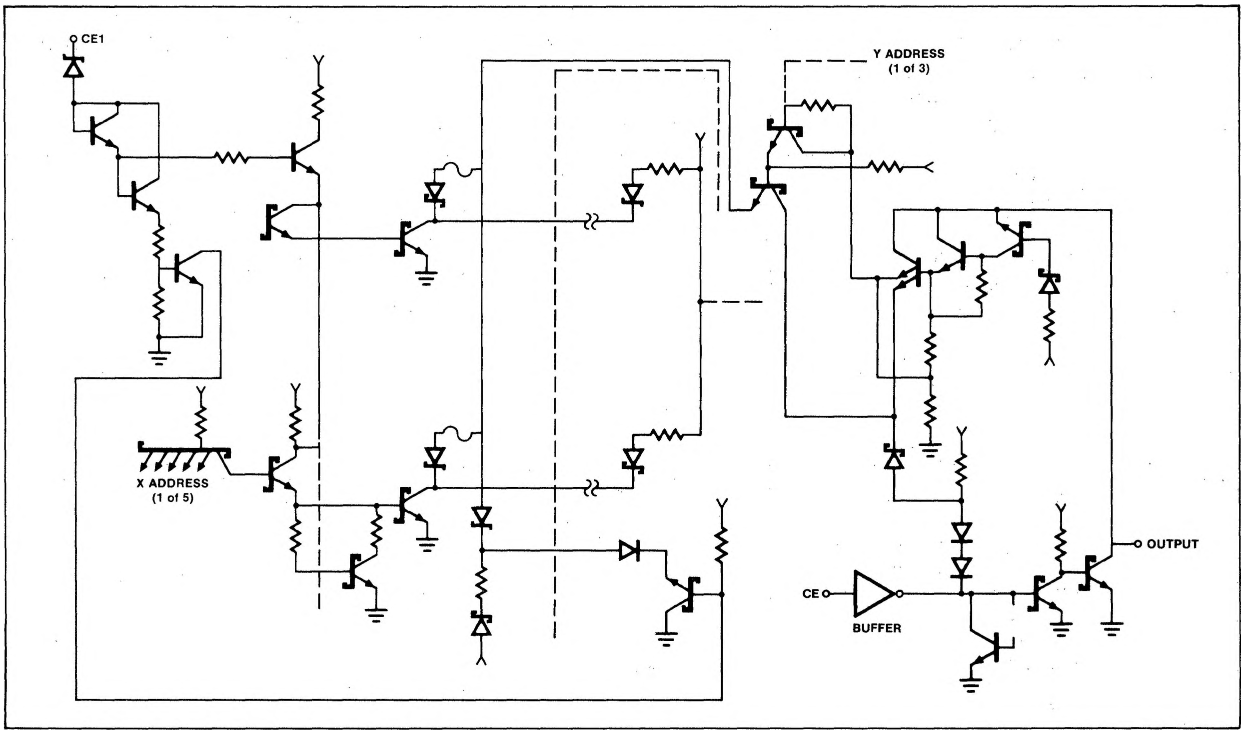
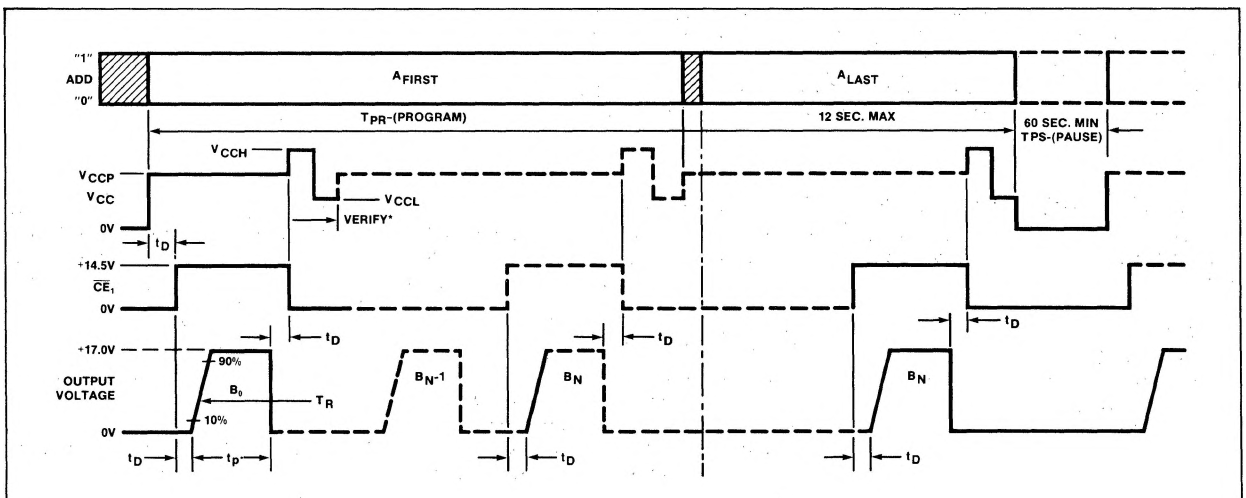
TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low Vcc margins is optional. For convenience, verification can also be executed at the operating Vcc limits specified in the dc characteristics.