

96LS42

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ADDRESS MULTIPLEXER/REFRESH COUNTER

(For 16K Dynamic RAMs)

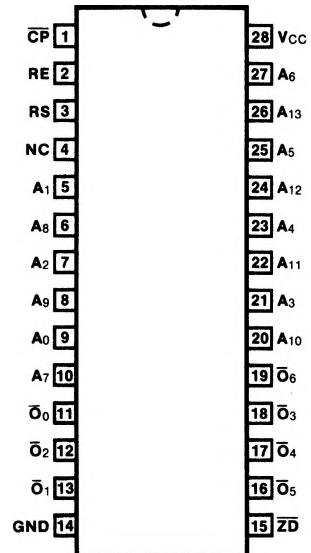
DESCRIPTION — The 96LS42 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of 64 or 128 cycles. It multiplexes 14 bits of system supplied address to seven output address pins. The device also contains a 7-bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 96LS42 makes it especially suitable for use with high speed n-channel RAMs like the F16K. The 96LS42 is manufactured using Fairchild's advanced low power Schottky process.

- SIMPLIFIES SYSTEM DESIGN
- REDUCES PACKAGE COUNT
- DRIVES HIGH CAPACITIVE LOADS
- EITHER BURST OR DISTRIBUTED REFRESH
- LOW POWER SCHOTTKY DESIGN
- STANDARD 28-PIN PACKAGE

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	96LS42PC		9Y
Ceramic DIP (D)	A	96LS42DC	96LS42DM	8E

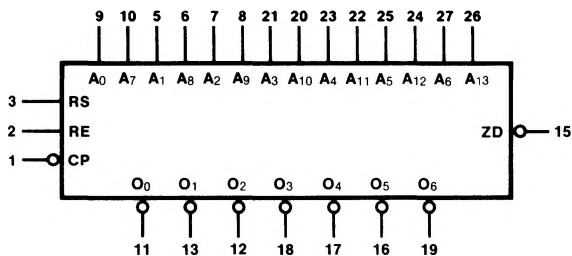
CONNECTION DIAGRAM PINOUT A



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

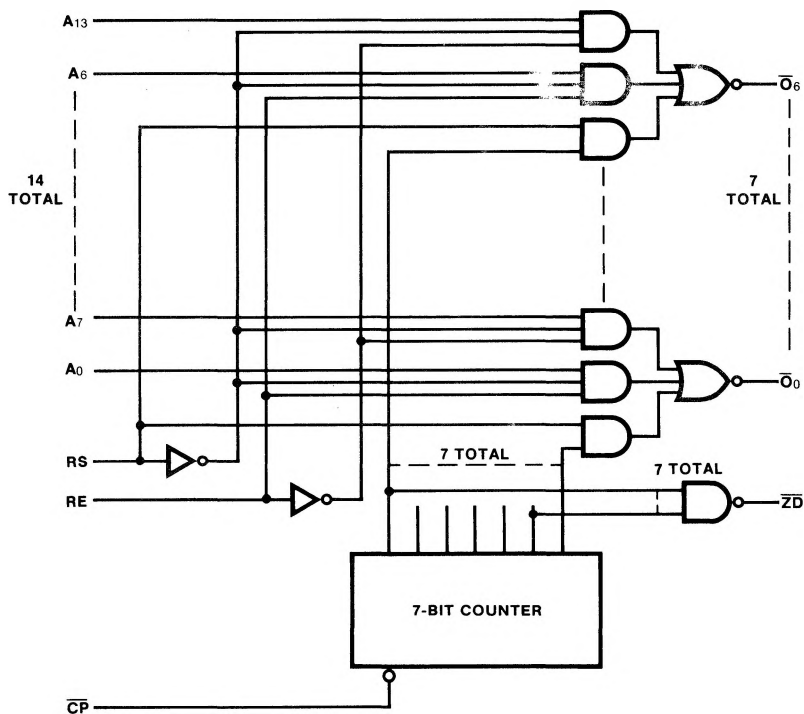
PIN NAMES	DESCRIPTION	96XX (U.L.) HIGH/LOW
A ₀ — A ₆	Row Address Inputs	0.5/0.13
A ₇ — A ₁₃	Column Address Inputs	0.5/0.13
CP	Clock Pulse Input (Active Falling Edge)	0.5/0.13
RE	Reirefresh Enable Input	0.5/0.13
RS	Row Select Input	0.5/0.13
ZD	Refresh Counter Zero Detect Output (Active LOW)	25/3.1
O ₀ — O ₆	Multiplexer Outputs (Active LOW)	25/3.1

LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

LOGIC DIAGRAM



96LS42

FUNCTIONAL DESCRIPTION — The 96LS42 address multiplexer/refresh counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh

These functions are controlled by two signals, Refresh Enable and Row Select, both of which are active HIGH TTL inputs. The Function Table shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter)
2. Row addresses (A_0 through A_6)
3. Column addresses (A_7 through A_{13})

Burst Refresh Mode — When refresh is requested the Refresh Enable input is HIGH. This input is AND-ed with the seven outputs of the internal 7-bit counter. At each \overline{CP} pulse the counter increments by one, sequencing the outputs (\overline{O}_0 — \overline{O}_6) through all 128 row addresses. When the counter sequences to all zeroes, the Zero Detect output goes LOW signaling the end of the refresh sequence. Due to counter decoding spikes, the Zero Detect output is valid only after t_{cz} following the LOW going edge of \overline{CP} .

Distributed Refresh Mode — In the distributed refresh mode, one row is selected for refresh each $(t_{refresh}/n)$ time where n = number of rows in the device and refresh is the specified refresh rate for the device. For the F16 k, Refresh = 2.0 ms and $n = 128$, therefore one row is refreshed each $62 \mu\text{s}$. Following the refresh cycle at row n , the \overline{CP} input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row $n + 1$. The \overline{CP} input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address — All 14 system address lines are applied to the inputs of the 96LS42. When Refresh Enable is LOW and Row Select is HIGH, the input Addresses A_0 — A_6 are gated to the outputs and applied to the driven memories. Conversely, when Row Select is LOW (with Refresh Enable still LOW), input addresses A_7 — A_{13} are gated to the outputs and applied to the driven memories. When memory devices are driven directly by the 96LS42, the address applied to the memory devices is the inverse of the address at the inputs due to the inverted outputs of the 96LS42. This should be remembered when checking out the memory system.

FUNCTION TABLE

Refresh Enable	Row Select	Outputs
H	X	Refresh Address (from internal counter)
L	H	Row Address (complement of A_0 — A_6)
L	L	Column Address (complement of A_7 — A_{13})

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial