8/16-Channel, 5V Single Supply, 12/14-Bit, Voltage-Output DACs

Preliminary Technical Data AD5390/AD5391/AD5392

FEATURES

AD5390: 16-Channel, 14-Bit, Voltage Out DAC
AD5391: 16-Channel, 12-Bit Voltage Out DAC
AD5392: 8-Channel, 14-Bit, Voltage Out DAC
INL: ±1 LSBmax (AD5391) ±4Lsb max AD390/92
All Devices Guaranteed Monotonic
Package: All available in 64-lead LFCSP (9mm x 9mm)
Interface: Serial DSP/Microcontroller Compatible and I2C compatible
On-chip Output Amplifier with Rail to Rail Operation
System Calibration Function allowing User Programmable Offset and Gain Adjust
On-chip 1.25/2.5V, 10ppm/°C Reference
Clear Function
Simultaneous Update of DAC Outputs (LDAC Pin)
Power-On-Reset

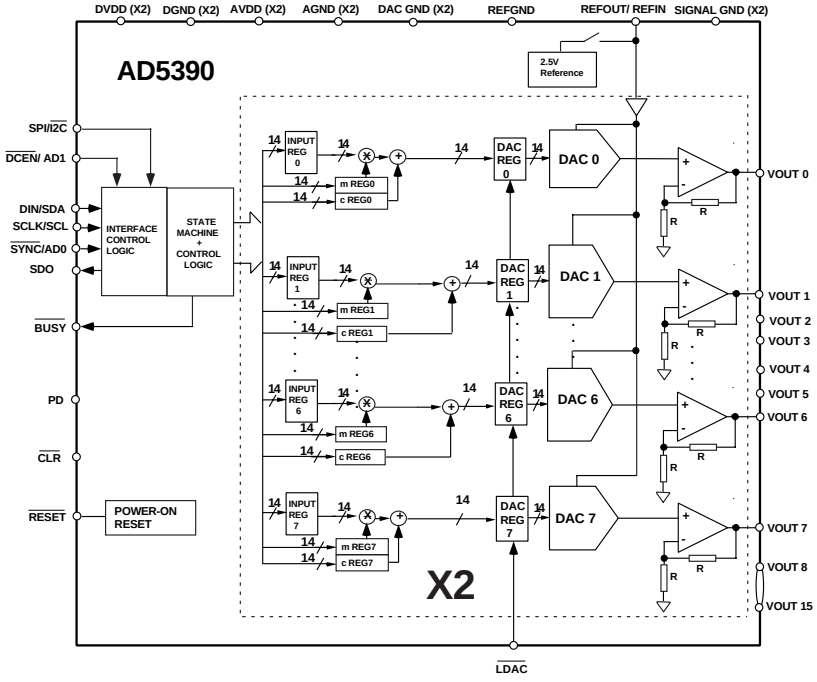
APPLICATIONS

Instrumentation and Industrial Control
Power Amplifier Control
Level Setting
Control Systems
Optical Microelectromechanical Systems (MEMs)
Variable Optical Attenuators (VOA)

GENERAL DESCRIPTION

The AD5390/91 are complete single supply, 16-channel, 14/12-bit DACs while the AD5392 is a complete single supply, 8-channel, 14-bit DAC. All devices are available in 64-lead LFCSP package. All channels have an on-chip output amplifier with rail-to-rail operation. All devices include an internal 1.25/2.5V, 10ppm/°C reference, an on-chip channel monitor function that multiplexes the analog outputs to a common MON_OUT pin for external monitoring and an output amplifier boost mode that allows the amplifier settling time to be optimized.
The AD5390/91/92 contain a 3-wire serial interface with interface speeds in excess of 30MHz that is compatible with SPI™, QSPI™, MICROWIRE™ and DSP interface standards and an I2C compatible interface supporting 400kHz data transfer rate. An input register followed by a DAC register provides double buffering allowing the DAC outputs to be updated independantly or simultaneously using the LDAC input. Each channel has a programmable gain and offset adjust register allowing the user to fully calibrate any DAC Channel.
Power consumption is typically 0.3mA/channel.

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent Nos. 5,969,657; other patents pending.
SPI and **QSPI** are Trademarks of Motorola, Inc.
MICROWIRE is a Trademark of National Semiconductor Corporation.

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AD5390/91/92–SPECIFICATIONS

(AV_{DD} = 4.5V to 5.5V ; DV_{DD}=2.7V to 5.5V, AGND=DGND = 0 V; C_L = 200 pF to AGND; R_L = 5kΩ ; V_{REF} =2.5V; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	AD5390/92[1]	AD5391[1]	Units	Test Conditions/Comments
ACCURACY				
Resolution	14	12	Bits	
Relative Accuracy	±4	±1	LSB max	
Differential Nonlinearity	-1/+2	±1	LSB max	Guaranteed Monotonic Over Temp
Zero-Scale Error	±10	±10	mV max	
Offset Error	±10	±10	mV max	Measured at code X in the linear region
Offset Error TC	±5	±5	uV/°C typ	
Gain Error	±0.02	±0.02	% FSR max	
Gain Temperature Coefficient[2]	20	20	ppm FSR/°C typ	
DC Crosstalk[2]	0.5	0.5	mV max	Typically TBD mV
REFERENCE INPUT/OUTPUT				
REFERENCE INPUT[2]				
Reference Input Voltage	2.5	2.5	V	±1% for Specified Performance
DC Input Impedance	1	1	MΩ min	Typically 100 MΩ
Input Current	±10	±10	µA max	Typically ±30 nA
Reference Range	1V to V_{DD}/2	1V to V_{DD}/2	V min/max	
REFERENCE OUTPUT[4]				
Output Voltage	2.495/2.505	2.495/2.505	V min/max	At Ambient
	1.248/1.252	1.248/1.252	V min/max	
Reference TC	±10	±10	ppm typ	
OUTPUT CHARACTERISTICS[2]				
Output Voltage Range[3]	0/AV_{DD}	0/AV_{DD}	V min/max	
Short Circuit Current	40	40	mA max	
Load Current	±1	±1	mA max	
Capacitive Load Stability				
R_L=∞	200	200	pF max	
R_L=5kΩ	TBD	TBD	pF max	
DC Output Impedance	0.5	0.5	Ω max	
MONITOR OUTPUT PIN				
Output Impedance	500	500	Ω typ	
Tristate Leakage Current	100	100	nA typ	
LOGIC INPUTS[2]				DV_{DD} = 2.7 V to 5.5 V
V_{IH}, Input High Voltage	2	2	V min	
V_{IL}, Input Low Voltage	0.8	0.8	V max	
Input Current	±10	±10	µA max	Total for All Pins. T_A = T_{MIN} to T_{MAX}
Pin Capacitance	10	10	pF max	
LOGIC INPUTS (SCL, SDA ONLY)				
V_{IH}, Input High Voltage	0.7 DV_{DD}	0.7 DV_{DD}	V min	SMBus-Compatible at DV_{DD} < 3.6 V
V_{IL}, Input Low Voltage	0.3 DV_{DD}	0.3 DV_{DD}	V max	SMBus-Compatible at DV_{DD} < 3.6 V
I_{IN}, Input Leakage Current	±1	±1	µA	
V_{HYST}, Input Hysteresis	0.05 DV_{DD}	0.05 DV_{DD}	V	
C_{IN}, Input Capacitance	8	8	pF	
Glitch Rejection	50	50	ns	Input filtering suppresses noise spikes of less than 50 ns.
LOGIC OUTPUTS (BUSY, SDO)[2]				
Output Low Voltage	0.4	0.4	V max	DV_{DD}= 5V ± 10%, Sinking 200µA
Output High Voltage	DV_{DD}-1	DV_{DD}-1	V min	DV_{DD}= 5V ± 10%, SDO Only, Sourcing 200µA
Output Low Voltage	0.4	0.4	V max	DV_{DD}= 2.7V to 3.6V, Sinking 200µA
Output High Voltage	DV_{DD}-0.5	DV_{DD}-0.5	V min	DV_{DD}= 2.7V to 3.6V, SDO Only, Sourcing 200µA
High Impedance Leakage Current	±1	±1	µA max	
High Impedance Output Capacitance	5	5	pF typ	
LOGIC OUTPUT (SDA)[2]				
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{SINK} = 3 mA
	0.6	0.6	V max	I_{SINK} = 6 mA
Three-State Leakage Current	±1	±1	µA	
Three-State Output Capacitance	8	8	pF	

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(AV_{DD} = 4.5V to 5.5V ; DV_{DD}=2.7V to 5.5V, AGND=DGND = 0 V; C_L = 200 pF to AGND; R_L = 5kΩ ; V_{REF} =2.5V; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

POWER REQUIREMENTS				
AV_{DD}	4.5/5.5	4.5/5.5	V min/max	
DV_{DD}	2.7/5.5	2.7/5.5	V min/max	
Power Supply Sensitivity[2]				
ΔMid Scale/ΔAV_{DD}	-85	-85	dB typ	
AI_{DD}	0.5	0.5	mA/Channel max	Outputs Unloaded. Boost Off. XXmA typ
AI_{DD}	0.57	0.57	mA/Channel max	Outputs Unloaded. Boost On. XXmA typ
DI_{DD}	5	5	mA max	V_{IH} = DV_{DD}, V_{IL} = DGND. XXmA typ
AI_{DD} (Power Down)	5	5	uA max	
DI_{DD} (Power Down)	5	5	uA max	
Power Dissipation	65	65	mW max	AD5390/91 with Outputs Unloaded.
	45	45	mW max	AD5392 with Outputs Unloaded.

NOTES
[1]Temperature range for All Versions: -40°C to +85°C
[2]Guaranteed by characterization. Not production tested.
[3]Accuracy guaranteed from Vout = 10mV to AV_{DD}-50mV
[4]Programmable to either 1.25V typ or 2.5V typ via the AD539X control register.
Specifications subject to change without notice.

AC CHARACTERISTICS[1] (AV_{DD}= 4.5V to 5.5V ; DV_{DD}=2.7V to 5.5V; AGND = DGND= 0 V; C_L = 200 pF to AGND)

Parameter	All	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time			Boost Mode Off
AD5390/92	8	µs typ	1/4 Scale to 3/4 Scale Change settling to ±1LSB.
	10	µs max	
AD5391	6	µs typ	1/4 Scale to 3/4 Scale Change settling to ±1LSB.
	8	µs max	
Output Voltage Settling Time			Boost Mode On
AD5390/92	3	µs typ	1/4 Scale to 3/4 Scale Change settling to ±1LSB.
	5	µs max	
AD5391	2	µs typ	1/4 Scale to 3/4 Scale Change settling to ±1LSB.
	4	µs max	
Slew Rate	0.7	V/µs typ	Boost Mode Off
	1.5	V/µs typ	Boost Mode On
Digital-to-Analog Glitch Energy	12	nV-s typ	
Glitch Impulse Peak Amplitude	5	mV max	
Channel-to-Channel Isolation	100	dB typ	See Terminology
DAC-to-DAC Crosstalk	10	nV-s typ	See Terminology
Digital Crosstalk	10	nV-s typ	
Digital Feedthrough	1	nV-s typ	Effect of Input Bus Activity on DAC Output Under Test
Output Noise Spectral Density			
@ 1 kHz	150	nV/(Hz)$^{1/2}$ typ	
@ 10 kHz	100	nV/(Hz)$^{1/2}$ typ	

[1]Guaranteed by design and characterization, not production tested.
[2] The settling time and slew rate can be programmed via the current boost control bit in the AD539X control registers.
Specifications subject to change without notice.

TIMING CHARACTERISTICS

(DV_{DD}= 2.7V to 5.5V ; AV_{DD}=+4.5V to +5.5V; AGND= DGND = 0 V;) All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

SERIAL INTERFACE

Parameter[1,2,3]	Limit at T_{MIN}, T_{MAX}	Units	Description
t_1	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	13	ns min	SYNC Falling Edge to SCLK Falling Edge Setup Time
t_5[4]	13	ns min	24th SCLK Falling Edge to SYNC Falling Edge
t_6[4]	33	ns min	Minimum SYNC Low Time
t_7	10	ns min	Minimum SYNC High Time
t_8	5	ns min	Data Setup Time
t_9	4.5	ns min	Data Hold Time
t_{10}[4,5]	30	ns max	24th SCLK Falling Edge to BUSY Falling Edge
t_{11}	900	ns typ	BUSY Pulse Width Low (Single Channel Update)
t_{12}[4]	20	ns min	24th SCLK Falling Edge to LDAC Falling Edge
t_{13}	20	ns min	LDAC Pulse Width Low
t_{14}	100	ns max	BUSY Rising Edge to DAC Output Response Time
t_{15}	0	ns min	BUSY Rising Edge to LDAC Falling Edge
t_{16}	100	ns min	LDAC Falling Edge to DAC Output Response Time
t_{17}	8	µs typ	DAC Output Settling Time, AD5390/92 with Boost Off
t_{18}	20	ns min	CLR Pulse Width Low
t_{19}	12	µs max	CLR Pulse Activation Time
t_{20}[6,7]	20	ns max	SCLK Rising Edge to SDO Valid
t_{21}[7]	5	ns min	SCLK Falling Edge to SYNC Rising Edge
t_{22}[7]	8	ns min	SYNC Rising Edge to SCLK Rising Edge
t_{23}[7]	20	ns min	SYNC Rising Edge to LDAC Falling Edge

NOTES

[1]Guaranteed by design and characterization, not production tested.

[2]All input signals are specified with t_r = t_f = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.2 V.

[3]See Figures 3 and 4

[4]Stand-Alone Mode only.

[5]This is measured with the load circuit of Figure 1a.

[6]This is measured with the load circuit of Figure 1b.

[7]Daisy-Chain Mode only.

Specifications subject to change without notice.

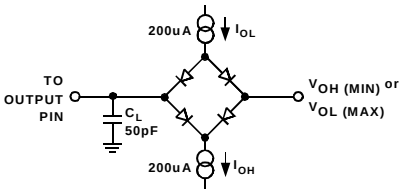


Figure 1. Load Circuit for SDO Timing Diagram (Serial Interface, Daisy-Chain mode)

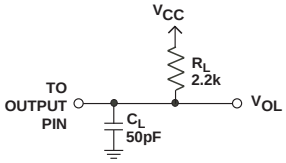


Figure 1a Load Circuit for BUSY Timing Diagram

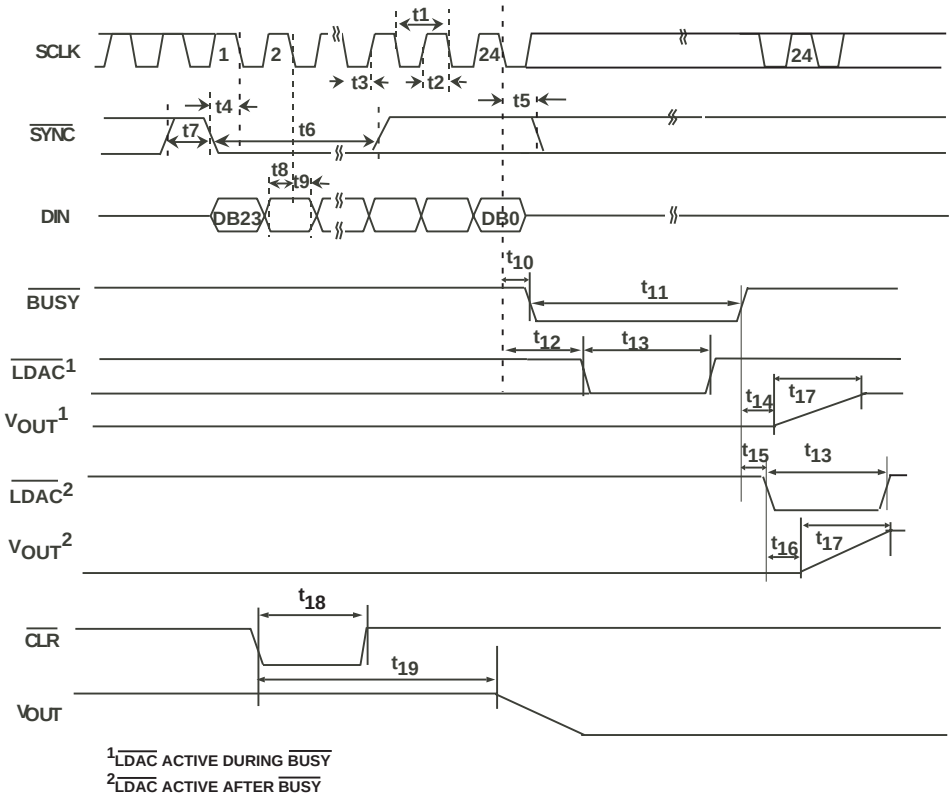


Figure 3. Serial Interface Timing Diagram (Stand-Alone mode)

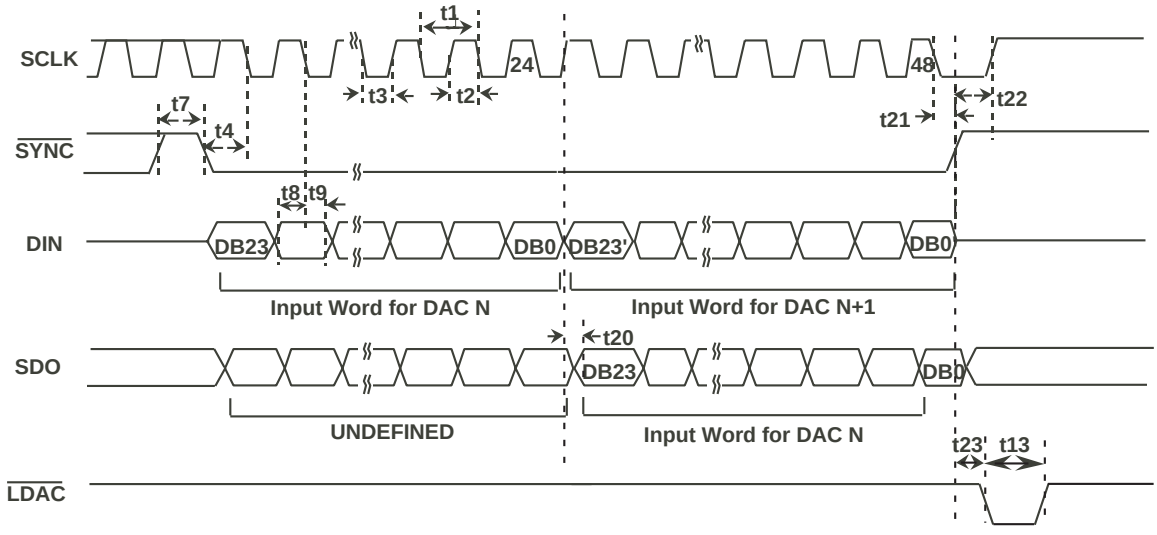


Figure 4. Serial Interface Timing Diagram (Daisy-Chain mode)

TIMING CHARACTERISTICS

(DV_{DD}= 2.7V to 5.5V ; AV_{DD}=+4.5V to +5.5V; AGND= DGND = 0 V;)
All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

I2C SERIAL INTERFACE

Parameter[1,2]	Limit at T_{MIN}, T_{MAX}	Units	Description
F_{SCL}	400	kHz max	SCL Clock Frequency
t_1	2.5	µs min	SCL Cycle Time
t_2	0.6	µs min	t_{HIGH}, SCL High Time
t_3	1.3	µs min	t_{LOW}, SCL Low Time
t_4	0.6	µs min	$t_{HD,STA}$, Start/Repeated Start Condition Hold Time
t_5	100	ns min	$t_{SU,DAT}$, Data Setup Time
t_6[3]	0.9	µs max	$t_{HD,DAT}$, Data Hold Time
	0	µs min	$t_{HD,DAT}$, Data Hold Time
t_7	0.6	µs min	$t_{SU,STA}$, Setup Time for Repeated Start
t_8	0.6	µs min	$t_{SU,STO}$, Stop Condition Setup Time
t_9	1.3	µs min	t_{BUF}, Bus Free Time Between a STOP and a START Condition
t_{10}	300	ns max	t_R, Rise Time of SCL and SDA when Receiving
	0	ns min	t_R, Rise Time of SCL and SDA when Receiving (CMOS-Com patible)
t_{11}	300	ns max	t_F, Fall Time of SDA when Transmitting
	0	ns min	t_F, Fall Time of SDA when Receiving (CMOS-Compatible)
	300	ns max	t_F, Fall Time of SCL and SDA when Receiving
	20 + $0.1C_B$[3]	ns min	t_F, Fall Time of SCL and SDA when Transmitting
C_B	400	pF max	Capacitive Load for Each Bus Line

NOTES
[1]Guaranteed by design and characterization, not production tested.
[2]See Figures 5

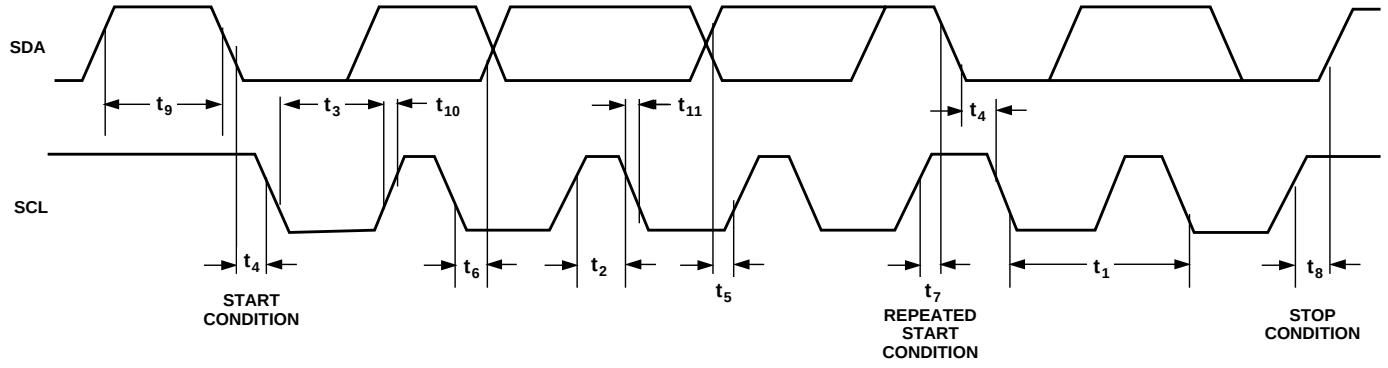


Figure 5. I2C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1,2]

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND.....-0.3 V to +7 V
DV_{DD} to DGND.....-0.3 V to +7 V
Digital Inputs to DGND..... .....-0.3 V to DV_{DD} + 0.3 V
Digital Outputs to DGND.....-0.3 V to DV_{DD} + 0.3 V
V_{REF} to AGND.....-0.3 V to +7 V
REFOUT to AGND.....-0.3 V to +7 V
AGND to DGND.....-0.3 V to +0.3 V
VOUT0-39 to AGND..... - 0.3 V to AV_{DD} + 0.3 V

Operating Temperature Range
Commercial (B Version).....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Junction Temperature (T_J max).....+150°C
64-lead LFCSP Package, θ_{JA} Thermal Impedance...TBD°C/W
Reflow Soldering
Peak Temperature.....230°C

NOTES:
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100mA will not cause SCR latch-up

ORDERING GUIDE

Model Option	Resolution	Output Channels	Linearity Error (LSBs)	Package	Package Description
AD5390BCP	14-Bits	16	±4	64-lead LFCSP	CP-64
AD5391BCP	12-Bits	16	±1	64-lead LFCSP	CP-64
AD5392BCP	14-Bits	8	±4	64-lead LFCSP	CP-64

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5390/91/92 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error and is expressed in Least Significant Bits.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error
Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC register.
Ideally, with all 0s loaded to the DAC and m = all 1s, c = 2^{n-1}:

$$VOUT_{(Zero\text{-}Scale)} = 0V$$

Zero-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal) expressed in mV. It is mainly due to offsets in the output amplifier.

Offset-Error
Offset error is a measure of the difference between VOUT (actual) and VOUT (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured when Code 32 is loaded into the DAC register.

Gain Error
Gain Error is specified in the linear region of the ouput range between Vout =10mV and Vout =AVdd-50mV. It is the deviation in slope of the DAC transfer characteristic from ideal and is expressed in % FSR.

DC Crosstalk

This is the DC change in the output level of one DAC at midscale in response to a fullscale code (all 0's to all 1's and vice versa) and output change of all other DACs. It is expressed in LSbs.

DC Output Impedance
This is the effective output source resistance. It is dominated by package lead resistance.

Output Voltage Settling Time
This is the amount of time it takes for the output of a DAC to settle to a specified level for a 1/4 to 3/4 full-scale input change and measured from BUSY rising edge.

Digital-to-Analog Glitch Energy
This is the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 1FFF Hex and 2000Hex.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is defined as the glitch impulse that appears at the output of one DAC output due to both the digital change and subsequent analog O/P change at another DAC. The victim channel is loaded with mid-scale and DAC-to-DAC crosstalk is specified in nV-s.

Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter is defined as the digital crosstalk and is specified in nV-s.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the V_{OUT} pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density
This is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per root Hertz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in $nV/(Hz)^{1/2}$ in a 1 Hz bandwidth at 10KHz.

AD539X PIN FUNCTION DESCRIPTIONS

Mnemonic	Function
VOUTX	Buffered analog outputs for channel X. Each analog output is driven by a rail to rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5k to ground. Typical output impedance is 0.5 ohms.
SIGNAL_GND(1&2)	Analog ground reference points for each group of 8 output channels. All signal_gnd pins are tied together internally and should be connected to AGND plane as close as possible to the AD539X.
DAC-GND (1&2)	Each group of 8 channels contains a DAC_GND pin. This is the ground reference point for the internal 14-bit DACs.These pins shound be connected to the AGND plane.
AGND (1&2)	Analog Ground reference point. Each group of 8 channels contains an AGND pin. All AGND pins should be connected externally to the AGND plane.
AVDD (1&2)	Analog Supply pins. Each group of 8 channels has a separate AVDD pin. These pins should be decoupled with 0.1uF ceramic capacitors and 10uF tantalum capacitors.Operating range is 5V +/-10%
DGND	Ground for all digital circuitry.
DVDD	Logic Power Supply; Guaranteed operating range is 2.7 V to 5.5 V. Recommended that these pins be decoupled with 0.1uF ceramic and 10uF tantalum capacitors to DGND.
REF-GND	Ground Reference point for the internal reference.
REFOUT/REFIN	The AD539X contains a common REFOUT/REF IN pin. When the internal reference is selected this pin is the reference output. If the application necessitates the use of an external reference, it can be applied to this pin and the internal reference disabled vis the control register. The default for this pin is a reference input.
MON_OUT	Analog Output Pin. When the monitor function is enabled this output acts as the output of a 16-to-1 channel multiplexer which can be programmed to multiplex one of channels 0 to 15 to the MON_OUT pin. The MON_OUT pins output impedance is typically 500 ohms and is intended to drive a high input impedance like that exhibited by SAR ADC inputs.
MON_IN	Monitor Input Pins. The AD539X contain two monitor input pins allowing the user to connect input signals within the maximum ratings of the device to these pins for monitoring purposes. Any of the signals applied to the MON_IN pins along with the output channels can be switched to the MON_OUT pin via software. An external ADC for example can be used to monitor these signals.
SYNC/AD0	This is the Frame Synchronisation input signal for the serial interface. When taken low the internal counter is enabled to count the required number of clocks before the addressed register is updated. I2C Mode: This pin acts as a hardware address pin used in conjunction with AD1 to determine the software address for the device on the I2C bus.
DCEN/AD1	Interface Control pin. Serial Interface: Daisy-Chain Select Input (level sensitive, active high). When high this signal is used to enable SPI serial interface daisy-chain mode. I2C Mode: This pin acts as a hardware address pin used in conjunction with AD0 to determine the software address for this device on the I2C bus.
SDOUT	Serial Data Output. Tristatable CMOS output. SDO can be used for daisy-chaining a number of devices together. Data is clocked out on SDO on the rising edge of SCLK and is valid on the falling edge of SCLK.
BUSY	Digital CMOS Output. *BUSY* goes low during internal calculations of x2. If LDAC is taken low while *BUSY* is low this event is stored. *BUSY* also goes low during power-on-reset or when the *RESET* pin is low. During this time the interface is disabled and any events on *LDAC* are ignored.
LDAC	Load DAC Logic Input (active low). *If LDAC* is taken low while *BUSY* is inactive (high) the contents of the input registers are transferred to the DAC registers and the DAC outputs are updated. If *LDAC* is taken low while *BUSY* is active and internal calculations are taking place, the *LDAC* event is stored and the DAC registers are updated when *BUSY* goes inactive. However any events on *LDAC* during power-on-reset or *RESET* are ignored.
CLR	Asynchronous Clear Input (level sensitive, active low). While *CLR* is low all LDA*C* pulses are ignored. When CLR is activated all channels are updated with the data contained in the

CLR code register. BUSY is low for a duration of 12us while all channels are being updated with the CLR code.

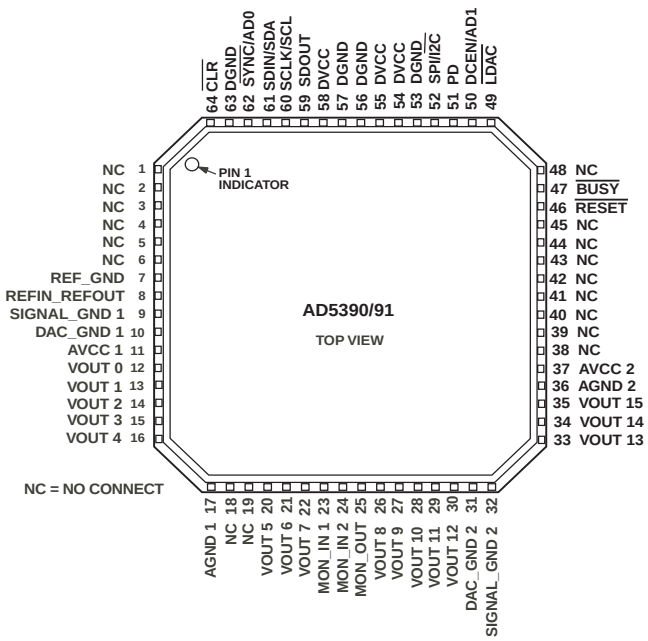
RESET Asynchronous Digital Reset Input (falling edge sensitive). The function of this pin is equivalent to that of the Power-On-Reset generator. When this pin is taken low, the state-machine initiates a reset sequence to digitally reset x1, m, c, and x2 registers to their default power-on values. This sequence takes 300us (typ). The falling edge *of RESET* initiates the RESET process and *BUSY* goes low for the duration returning high when *RESET is complete.* While BUSY is low all interfaces are disabled and all LDAC pulses are ignored. When BUSY returns high the part resumes normal operation and the status of the RESET pin is ignored till the next falling edge is detected.

PD Power Down (level sensitive active high). Used to place the device in low power mode where the device consumes less than 5uA. In power pown mode all internal analog circuitry is placed in low power mode, the analog output will be configured as high impedance outputs or will provide a 100k load to ground depending on how the power down mode is configured. The serial interface remains active during power down.

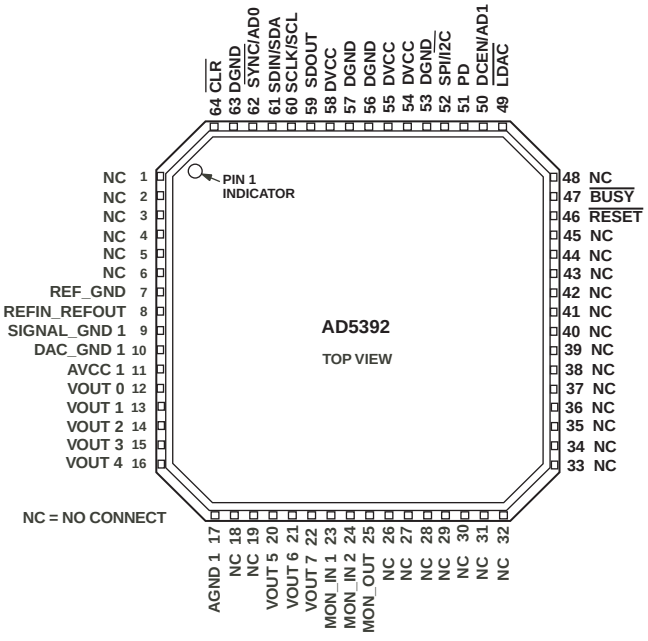
SPI/I2C Interface Select input pin. When this input is low I2C Mode is selected. When this input is high SPI Mode is selected.

SCLK/SCL Interface CLOCK input pin. In SPI compatible serial interface mode this pin acts as a serial clock input. This operates at clock speeds up to 50 MHz.
I2C Mode: In I2C mode this pin performs the SCL function, clocking data into the device. Data transfer rate in I2C mode is compatible with both 100kHz and 400kHz operating modes.

DIN/SDA Interface data input pin.
SPI/I2C =1: This pin acts as the serial data input. Data must be valid on the falling edge of SCLK.
SPI/I2C =0, I2C Mode: In I2C mode this pin is the serial data pin (SDA) operating as an open drain input/output.



AD5390/91 Pin Configuration



AD5392 Pin Configuration

FUNCTIONAL DESCRIPTION

DAC Architecture — General

The AD5390/91 are complete single supply, 16-channel, voltage output DACs offering resolution of 14 and 12 bits respectively. The AD5392 is a complete single supply, 8-channel, voltage output DAC offering 14-bit resolution. All devices are available in a 64-lead LFCSP package and feature serial interfaces. This family includes an internal 2.5V, 10ppm/°C reference that can be used to drive the buffered reference inputs, alternatively an external reference can be used to drive these inputs. All channels have an on-chip output amplifier with rail-to-rail output capable of driving a 5kΩ ohm in parallel with a 200pf load.

The architecture of a single DAC channel consists of a 12/14-bit resistor-string DAC followed by an output buffer amplifier operating at a gain of two. This resistor-string architecture guarantees DAC monotonicity. The 12/14-bit binary digital code loaded to the DAC register determines at what node on the string the voltage is tapped off before being fed to the output amplifier. Each channel on these devices contains independant offset and gain control registers allowing the user to digitally trim offset and gain. The inclusion of these registers allows the user the ability

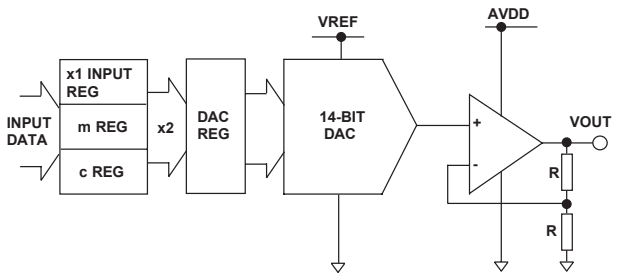


Figure 6. Single Channel Architecture

to calibrate out errors in the complete signal chain including the DAC using the internal M and C registers which hold the correction factors. All channels are double buffered allowing synchronous updating of all channels using the LDAC pin. Figure 6 shows a block diagram of a single channel on the AD5390/91/92.

The digital input transfer function for each DAC can be represented as:

$$x2 = [(m + 1)/2^n \times x1] + (c\text{-}2^{n-1})$$

x2 is the Dataword loaded to the resistor string DAC
x1 is the 12/14-bit Dataword written to the DAC input register
m is the 12/14-bit Gain Coefficient (default is all 3FFE Hex on the AD5390/92 and FFFEHex on the AD5391). The LSB of the gain coefficient must always be zero.

n=DAC resolution (n=14 for AD5390/92 and n=12 for AD5391)
c is the 12/14-bit Offset Coefficient (default is 2000Hex on the AD5390/92 and 800Hex on the AD5391)

The complete transfer function for these devices can be represented as:

$$VOUT = 2 \times V_{REF} \times x2/2^n$$

x2 is the Dataword loaded to the resistor string DAC
V_{REF} is the reference voltage applied to the DAC, 2.5V for specified performance.

Data Decoding

The AD5390/92 internally contain a 14-bit data bus. The input data is decoded depending on the data loaded to the REG1 and REG0 bits of the input serial register. This is outlined in Table 1. Data from the serial input register is loaded into the addressed DAC input register, Offset (c) register, or Gain (m) register. The format data, Offset (c) and gain (m) register contents are outlined in tables II to IV.

Table I. Register Selection

REG1	REG0	Register Selected
1	1	Input Data Register (x1)
1	0	Offset Register (c)
0	1	Gain Register (m)
0	0	Special Function Registers (SFRs)

Table II. DAC Data format (REG1 = 1, REG0 = 1)

DB13 to DB0	DAC Output
11 1111 1111 1111	$2 V_{REF} \times (16383/16384)$ V
11 1111 1111 1110	$2 V_{REF} \times (16382/16384)$V
10 0000 0000 0001	$2 V_{REF} \times (8193/16384)$ V
10 0000 0000 0000	$2 V_{REF} \times (8192/16384)$ V
01 1111 1111 1111	$2 V_{REF} \times (8191/16384)$ V
00 0000 0000 0001	$2 V_{REF} \times (1/16384)$ V
00 0000 0000 0000	0 V

Table III. Offset Data format (REG1 = 1, REG0 = 0)

DB13 to DB0	Offset
111111 1111 1111	+8192 LSB
111111 1111 1110	+8191 LSB
100000 0000 0001	+1 LSB
100000 0000 0000	+0 LSB
011111 1111 1111	-1 LSB
000000 0000 0001	-8191 LSB
000000 0000 0000	-8192 LSB

Table IV. Gain Data format (REG1 = 0, REG0 = 1)

DB13 to DB0	Gain Factor
11 1111 1111 1110	1
10 1111 1111 1110	0.75
01 1111 1111 1110	0.5
00 1111 1111 1110	0.25
00 0000 0000 0000	0

The AD5391 internally contains a 12-bit data bus. The input data is decoded depending on the value loaded to the REG1 and REG0 bits of the input serial register. The input data from the serial input register is loaded into the addressed DAC input register, Offset (c) register, or Gain (m) register. The format data, Offset (c) and gain (m) register contents are outlined in tables V to VII.

Table V. DAC Data format (REG1 = 1, REG0 = 1)

DB11 to DB0	DAC Output
1111 1111 1111	2 V_{REF} × (4095/4096) V
1111 1111 1110	2 V_{REF} × (4094/4096) V
1000 0000 0001	2 V_{REF} × (2049/4096) V
1000 0000 0000	2 V_{REF} × (2048/4096) V
0111 1111 1111	2 V_{REF} × (2047/4096) V
0000 0000 0001	2 V_{REF} × (1/4096) V
0000 0000 0000	0 V

Table VI. Offset Data format (REG1 = 1, REG0 = 0)

DB11 to DB0	Offset
1111 1111 1111	+2048 LSB
1111 1111 1110	+2047 LSB
1000 0000 0001	+1 LSB
1000 0000 0000	+0 LSB
0111 1111 1111	-1 LSB
0000 0000 0001	-2047 LSB
0000 0000 0000	-2048 LSB

Table VII. Gain Data format (REG1 = 0, REG0 = 1)

DB11 to DB0	Gain Factor
1111 1111 1110	1
1011 1111 1110	0.75
0111 1111 1110	0.5
0011 1111 1110	0.25
0000 0000 0000	0

INTERFACE

The AD5390/91/92 contain a serial interface. Furthermore, the serial interface can be programmed to be either DSP,SPI,MICROWIRE or I2C compatible. The SPI/I2C pin is used to select DSP,SPI,MICROWIRE or I2C interface mode.

To minimize both the power consumption of the device and on-chip digital noise, the interface only powers up fully when the device is being written to, i.e. on the falling edge of SYNC.

DSP, SPI, MICROWIRE Compatible Serial Interface

The serial interface can be operated with a minimum of 3-wires in stand alone mode or 5-wires in daisy chain mode. Daisy chaining allows many devices to be cascaded together to increase system channel count.The serial interface is control pins are as follows:

SYNC, DIN, SCLK - Standard 3-wire interface pins.

DCEN - Selects Stand-Alone Mode or Daisy-Chain Mode.

SDO - Data Out pin for Daisy-Chain Mode.

Figures 3 and 4 show the timing diagram for a serial write to the AD5390/91/92in both Stand-Alone and Daisy-Chain Mode.

The 24-bit data word format for the serial interface in shown in Figure 7 below.

MSB LSB

0 R/W 0 0 A3 A2 A1 A0 REG1 REG0 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

Figure 7a . AD5390, 16-Channel, 14-Bit DAC Serial Input Register Configuration

MSB LSB

0 R/W 0 0 A3 A2 A1 A0 REG1 REG0 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 X X

Figure 7b . AD5391, 16-Channel, 12-Bit DAC Serial Input Register Configuration

MSB LSB

0 R/W 0 0 0 A2 A1 A0 REG1 REG0 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

Figure 7c . AD5392, 8-Channel, 14-Bit DAC Serial Input Register Configuration

R/W is the Read or Write control bit.
A3-A0 are used to Address the input channels .
REG1 & REG0 Select the register to which data is written as outlined in Table 1.
DB13-DB0 Contain the input data word.
X is a dont care condition.

Stand-Alone Mode

By connecting DCEN (Daisy-Chain Enable) pin low, Stand-Alone Mode is enabled. The serial interface works with both a continuous and a noncontinuous serial clock. The first falling edge of SYNC starts the write cycle and resets a counter that counts the number of serial clocks to ensure that the correct number of bits are shifted into the serial shift register. Any further edges on SYNC except for a falling edge are ignored until 24 bits are clocked in. Once 24 bits have been shifted in, the SCLK is ignored. In order for another serial transfer to take place the counter must be reset by the falling edge of SYNC.

Daisy-Chain Mode

For systems which contain several devices the SDO pin may be used to daisy-chain several devices together. This daisy-chain mode can be useful in system diagnostics and reducing the number of serial interface lines.

By connecting DCEN (Daisy-Chain Enable) pin high, the Daisy-Chain Mode is enabled. The first falling edge of SYNC starts the write cycle. The SCLK is continuously applied to the input shift register when SYNC is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO of the first device to the DIN input on the next device in the chain, a multi-device interface is constructed. 24 clock pulses are required for each device in the system. Therefore, the total number of clock cycles must equal 24N where N is the total number of AD539X devices in the chain.

When the serial transfer to all devices is complete, SYNC is taken high. This latches the input data in each device in the daisy-chain and prevents any further data being clocked into the input shift register.

If the SYNC is taken high before 24 clocks are clocked into the part this is considered as a bad frame and the data is discarded.

The serial clock may be either a continuous or a gated clock. A continuous SCLK source can only be used if it can be arranged that SYNC is held low for the correct number of clock cycles. In gated clock mode a burst clock containing the exact number of clock cycles must be used and SYNC taken high after the final clock to latch the data.

I2C Serial Interface

The AD5390/91/92 feature an I2C compatible 2-wire interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between these DACs and the master at rates up to 400kHz. Figure 5 shows the 2-wire interface timing diagram.

In selecting the I2C operating mode firstly configure serial operating mode (SER/PAR=1) and then select I2C mode by configuring the SPI/I2C pin to a logic 1. The device is connected to this bus as slave devices (i.e., no clock is generated by the AD5390/91/92. The AD5390/AD5391/AD5392 have a 7-bit slave address 1010 1AD1AD0. The 5 MSBs are hard coded and the two LSBs are determined by the state of the AD1 AD0 pins.The facility to hardware configure AD1 and AD0 allows four of these devices to be configured on the bus.

I2C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals that configure START and STOP Conditions. Both SDA and SCL are pulled high by the external pull-up resistors when the I2C bus is not busy.

START and STOP Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. A START condition from the master signals the beginning of a transmission to the AD539X. The STOP condition frees the bus. If a repeated START condition (Sr) is generated instead of a STOP condition, the bus remains active.

Repeated START Conditions

A repeated START (Sr) condition may indicate a change of data direction on the bus. Sr may be used when the bus master is writing to several I2C devices and does not want to relinquish control of the bus.

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data word. ACK is always generated by the receiving device. The AD539X devices generate an ACK when receiving an address or data by pulling SDA low during the ninth clock period. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication.

AD539X Slave Addresses

A bus master initiates communication with a slavedevice by issuing a START condition followed by the 7-bit slave address. When idle, the AD5380 waits for a START condition followed by its slave address. The LSB of the address word is the Read/Write (R/W) bit. The AD539X devices are receive devices only and when communicating with these R/W = 0. After receiving the proper address 1010 1(AD1)(AD0) , the AD539X issues an ACK by pulling SDA low for one clock cycle.

The AD539X has four different user programmable addresses determined by the AD1 and AD0 bits.

WRITE OPERATION

There are three specific modes in which data can be written to the AD539X family of DACs.

4-Byte Mode.

When writing to the AD539X DACs, the user must begin with an address byte (R/W = 0) after which the DAC will acknowledge that it is prepared to receive data by pulling SDA low. The address byte is followed by the pointer byte, this addresses the specific channel in the DAC to be addressed and is also acknowledged by the DAC. Two bytes of data are then written to the DAC as shown in Figure 11. A STOP condition follows. This allows the user to update a single channel within the AD539X at any time and requires 4 bytes of data to be transferred from the master.

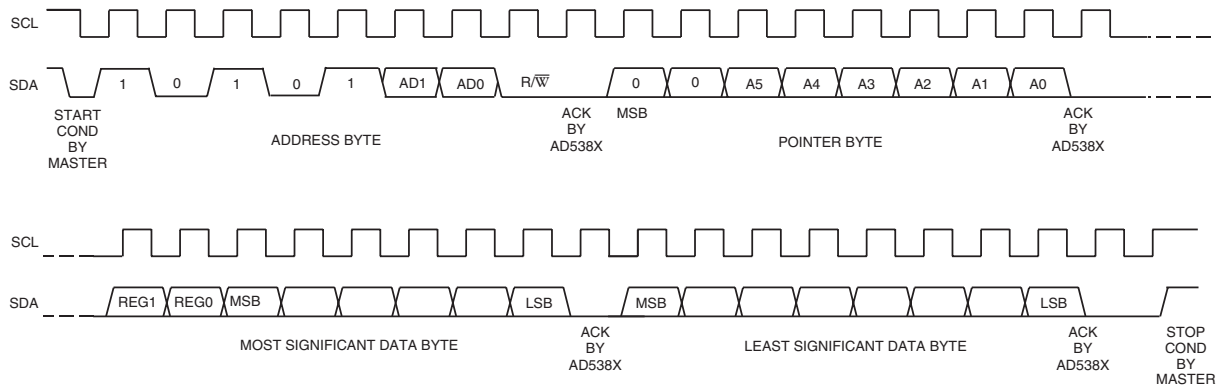


Figure 11 . 4-Byte AD5380, I2C Write Operation

3-Byte Mode

Three byte mode allows the user update more than one channel in a write sequence without having to write the device address byte each time. The device address byte is only required once and subsequent channel updates require the pointer byte and the data bytes. In three byte mode the user begins with an address byte (R/W = 0) after which the DAC will acknowledge that it is prepared to receive data by pulling SDA low. The address byte is followed by the pointer byte, this addresses the specific channel in the DAC to be addressed and is also acknowledged by the DAC. This is then followed by the two data bytes. REG1 and REG0 determine the register to be updated.

If a STOP condition is not sent following the data bytes another channel can be updated by sending a new pointer byte followed by the data bytes. This mode only requires 3-bytes to be sent to update any channel once the device has been initially addressed and reduces the software overhead in updating the AD539X channels. A STOP condition at any time exits this mode. Figure 12 shows a typical configuration.

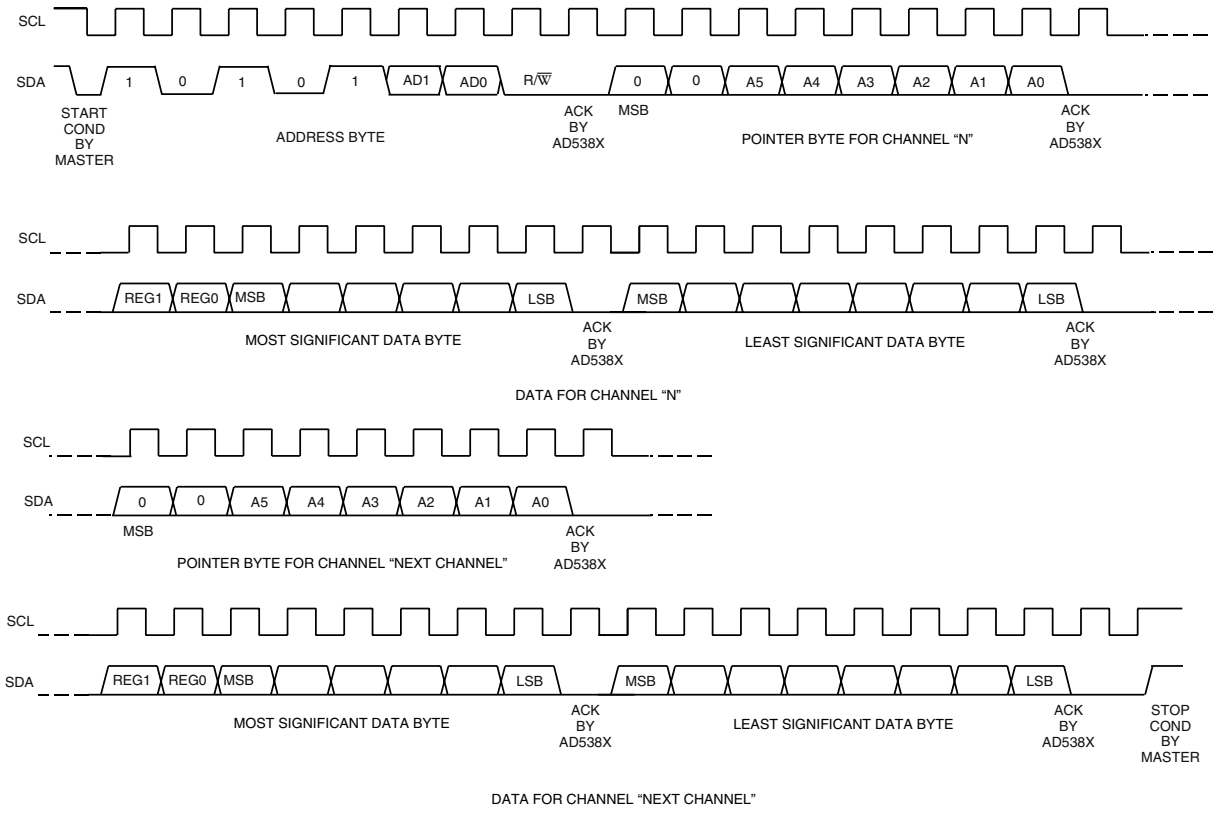


Figure 12 . 3-Byte AD538X, I2C Write Operation

2-Byte Mode

Two byte mode allows the user update channels sequentially following initialization of this mode. The device address byte is only required once and the pointer address pointer is configured for auto increment or burst mode.

The user must begin with an address byte (R/W = 0) after which the DAC will acknowledge that it is prepared to receive data by pulling SDA low. The address byte is followed by a specific pointer byte (3F Hex) which initiates the burst mode of operation. In this mode the address pointer initializes to channel zero and automatically increments to the next address on receiving the two data bytes for the present address. The REG0 and REG 1 bits in the data byte determine the register to be updated. In this mode, following the initialization only the 2-data bytes are required to update a channel, the channel address automatically increments from address 0. This allows transmission of data to all channels in one block and reduces the software overhead in configuring all channels. A STOP condition at any time exits this mode. Figure 13 shows a typical configuration.

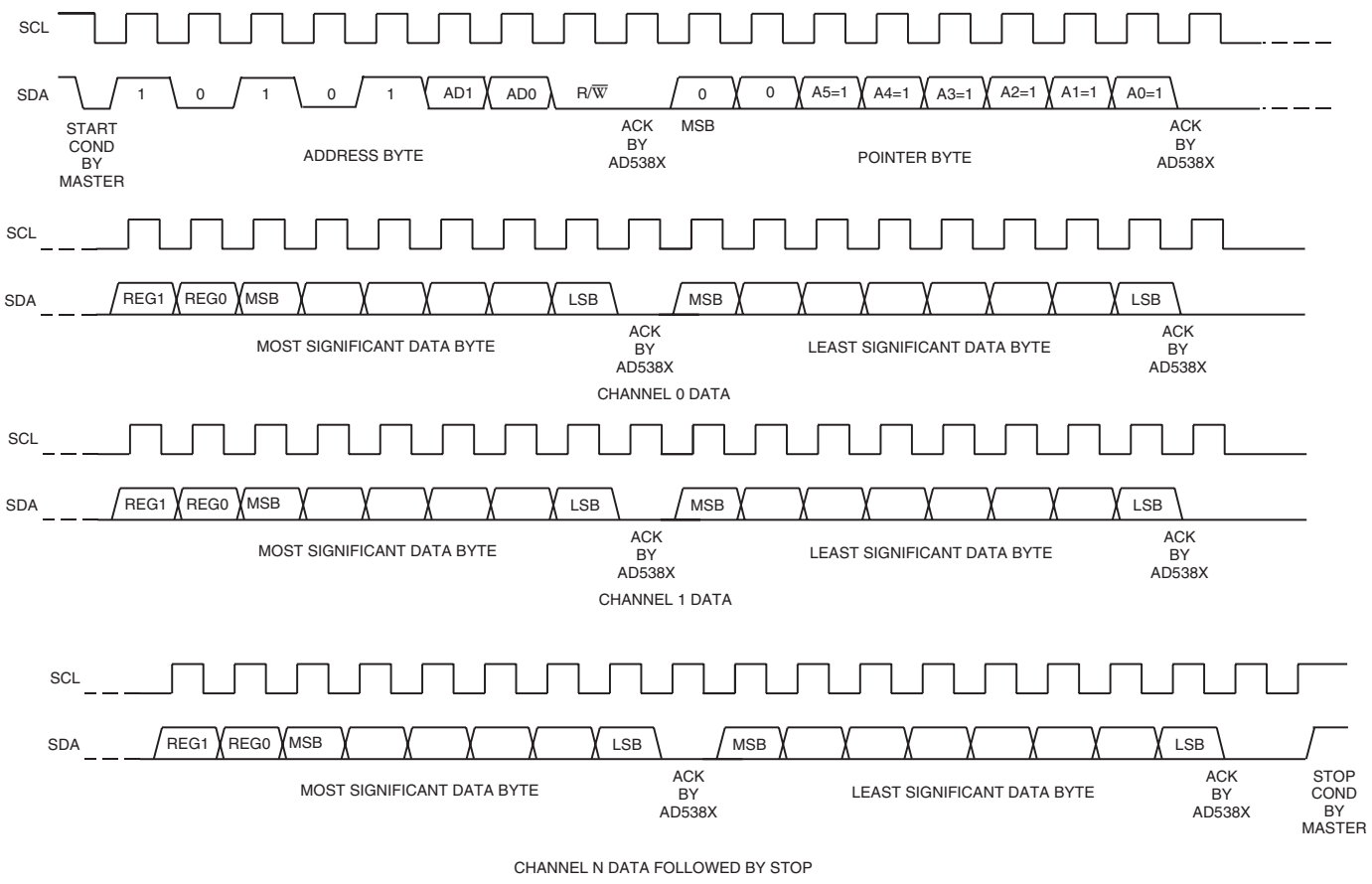


Figure 13 . 2-Byte AD539X, I2C Write Operation

AD539X On-chip Special Function Registers (SFR)
The AD539x family of parts contain a number of special function registers (SFRs)as outlined in table VIII. SFRs are addressed with REG1=REG0= 0 and are decoded using the Address bits A3 to A0.

Table VIII. SFR Register Functions (REG1 =0, REG0 = 0)

R / W	A3	A2	A1	A0	Function
X	0	0	0	0	NOP (No Operation)
0	0	0	0	1	Write ClR Code
0	0	0	1	0	Soft CLR
0	1	0	0	0	Soft Power Down
0	1	0	0	1	Soft Power Up
0	1	1	0	0	Control Register Write
1	1	1	0	0	Control Register Read
0	1	0	1	0	Monitor Channel
0	1	1	1	1	Soft Reset

SFR Commands

NOP (no operation)
REG1=REG0=0, A3-A0=0000

Perfoms no operation but is usefull in readback mode to clock out data on Dout for diagnostic purposes.

Write CLR Code
REG1=REG0=0, A3-A0=0001
DB13-DB0= Contain the CLR data.
Bringing the CLR line low or exercising the soft clear function will load the contents of the DAC registers with the data contained in the user configurable CLR register and sets VOUT0-VOUT15 accordingly. This can be very useful not only for setting up a specific output voltage in a clear condition but can also be used for calibration purposes where the user can load fullscale or zeroscale to the the clear code register and then issue a hardware or software clear to load this code to all DAC removing the need for individual writes to all DACs. Default on power up is all zeroes.

Soft CLR
REG1=REG0=0, A3-A0=0010
DB13-DB0= Dont Care.

Executing this instruction performs the CLR which is functionally the same as that provided by the external CLR pin. The DAC outputs are loaded with the data in the CLR code register. The time taken to fully execute the SOFT CLR is 16*400ns and is indicated by the BUSY low time.

Soft Power Down
REG1=REG0=0, A3-A0=1000
DB13-DB0= Dont Care.

Executing this instruction performs a global power-down feature that puts all channels into a low power mode reducing both analog and digital power consumption to 5uA. In power down mode the output amplifier can be configured as a high impedance output or provide a 100k load to ground. The contents of all internal registers are retained in power-down mode. Cannot write to any register while in power down.

Soft Power up
REG1=REG0=0, A3-A0=1001
DB13-DB0= Dont Care.

This instruction is used to power up the output amplifiers and internal reference. The time to exit power down is XXus. The hardware power down and software function are internally combined in a digital OR function.

Soft RESET
REG1=REG0=0, A5-A0=001111
DB13-DB0= Dont Care.

This instruction is used to implement a software reset. All internal registers are reset to their default values which corresponds to m at fullscale and c at zero. The contents of the DAC registers are cleared setting all analog outputs to zero volts. The soft rreset activation time is 150us (typ).

Monitor Channel
REG1=REG0=0, A3-A0=01010
DB13-DB8= Contain data to address the channel to be monitored.
A monitor function is provided on all devices. This feature consisting of a multiplexer addressed via the interface allows any channel output to be routed to this pin for monitoring using an external ADC. In channel monitor mode the monitored channel is routed to the MON_OUT pin. In addition to monitoring all output channels, two external inputs are also provided allowing the user to monitor signals external to the AD539X. The channel monitor function must be enabled in the control register before any channels are routed to the MON_OUT pin. On the AD5390 and AD5392, 14 bit parts, DB13 to DB8 contain the channel address for the monitored channel. On the AD5391, 12 bit part, DB11 to DB6 contain the channel address for the channel to be monitored. Selecting channel XX tri-states the MON_OUT pin.

The Channel Address decoding for the AD539X is as follows:

REG1	REG0	A3	A2	A1	A0	DB13	DB12	DB11	DB10	DB9	DB8	DB7 ->DB0	MON_OUT (AD5390)	MON_OUT (AD5392)
0	0	1	0	1	0	0	0	0	0	0	0	X	Vout 0	Vout 0
0	0	1	0	1	0	0	0	0	0	0	1	X	Vout 1	Vout 1
0	0	1	0	1	0	0	0	0	0	1	0	X	Vout 2	Vout 2
0	0	1	0	1	0	0	0	0	0	1	1	X	Vout 3	Vout 3
0	0	1	0	1	0	0	0	0	1	0	0	X	Vout 4	Vout 4
0	0	1	0	1	0	0	0	0	1	0	1	X	Vout 5	Vout 5
0	0	1	0	1	0	0	0	0	1	1	0	X	Vout 6	Vout 6
0	0	1	0	1	0	0	0	0	1	1	1	X	Vout 7	Vout 7
0	0	1	0	1	0	0	0	1	0	0	0	X	Vout 8	
0	0	1	0	1	0	0	0	1	0	0	1	X	Vout 9	
0	0	1	0	1	0	0	0	1	0	1	0	X	Vout 10	
0	0	1	0	1	0	0	0	1	0	1	1	X	Vout 11	
0	0	1	0	1	0	0	0	1	1	0	0	X	Vout 12	
0	0	1	0	1	0	0	0	1	1	0	1	X	Vout 13	
0	0	1	0	1	0	0	0	1	1	1	0	X	Vout 14	
0	0	1	0	1	0	0	0	1	1	1	1	X	Vout 15	
0	0	1	0	1	0	1	1	0	1	0	0	X	MON_IN1	
0	0	1	0	1	0	1	1	0	1	0	1	X	MON_IN2	

AD5390/AD5392 Channel Monitor Decoding

The Channel Address decoding for the AD5391 is as follows:

REG1	REG0	A3	A2	A1	A0	DB11	DB10	DB9	DB8	DB7	DB6	DB5 ->DB0	MON_OUT (AD5391)
0	0	1	0	1	0	0	0	0	0	0	0	X	Vout 0
0	0	1	0	1	0	0	0	0	0	0	1	X	Vout 1
0	0	1	0	1	0	0	0	0	0	1	0	X	Vout 2
0	0	1	0	1	0	0	0	0	0	1	1	X	Vout 3
0	0	1	0	1	0	0	0	0	1	0	0	X	Vout 4
0	0	1	0	1	0	0	0	0	1	0	1	X	Vout 5
0	0	1	0	1	0	0	0	0	1	1	0	X	Vout 6
0	0	1	0	1	0	0	0	0	1	1	1	X	Vout 7
0	0	1	0	1	0	0	0	1	0	0	0	X	Vout 8
0	0	1	0	1	0	0	0	1	0	0	1	X	Vout 9
0	0	1	0	1	0	0	0	1	0	1	0	X	Vout 10
0	0	1	0	1	0	0	0	1	0	1	1	X	Vout 11
0	0	1	0	1	0	0	0	1	1	0	0	X	Vout 12
0	0	1	0	1	0	0	0	1	1	0	1	X	Vout 13
0	0	1	0	1	0	0	0	1	1	1	0	X	Vout 14
0	0	1	0	1	0	0	0	1	1	1	1	X	Vout 15
0	0	1	0	1	0	1	1	0	1	0	0	X	MON_IN1
0	0	1	0	1	0	1	1	0	1	0	1	X	MON_IN2
0	0	1	0	1	0	1	1	0	1	1	0	X	Undefined
0	0	1	0	1	0	1	1	1	X	X	X	X	Undefined
0	0	1	0	1	0	1	1	1	1	1	1	X	Tristate

AD5391 Channel Monitor Decoding

Control Register Write
REG1=REG0=0, A3-A0=1100
DB13-DB0 contains the control register data.

AD5390 and AD5392 Control Register Contents

MSB												LSB
CR13	**CR12**	**CR11**	**CR10**	**CR9**	**CR8**	**CR7**	**CR6**	**CR5**	**CR4**	**CR3**	**CR1**	**CR0**

Table VIII AD5390 and AD5392 Control Register Contents

CR13: Power Down Status. This bit is used to configure the output amplifier state in power down.
CR13=1 amplifier output is high impedance .
CR13=0 amplifier output is 100k to ground (default on power up).

CR12: 3V/5V power supply operating mode. This bit conditions the DAC when operating at 3V or 5 V. CR12 is programmed as follows:

CR12=1: 5V condition, internal reference is 2.5V (default on power-up).
CR12=0: 3V condition, internal reference is 1.25V.

CR11: Current Boost Control. This bit is used to boost the current in the output amplifier therby altering its settling time. This bit is configured as follows:

CR11=1: Boost mode on. This maximizes the bias current in the output amplifier giving the fastest settling time (3us typ) but increasing the power dissipation.
CR11=0: Boost mode off (default on power up). This reduces the bias current in the output amplifier and reduces the overall power consumption but increases the settling time to 10us.

CR10: Internal/External Reference. This bits determines if the DAC uses its internal reference or an externally applied reference.

CR10=1: Internal Reference enabled. 1.25V with 3V supplies and 2.5V with 5V supplies.

CR10=0: External Reference selected (default on power up)

CR9: Voltage Output Monitor Enable

CR9=1: Monitor Enabled. This enables the channel monitor function. Following a write to the monitor channel in the SFR register the selected channel output is routed to the MON_OUT pin.

CR9=0: Monitor Disabled (default on power-up). When monitor is disabled the MON_OUT pin is tristated.

CR8: Thermal Monitor Function. This function is used to monitor the internal die temperature of the AD539X devices when enabled. The thermal monitor puts the device into soft power down when the temperature exceeds 130 degree C. This function can be used to protect the device in cases where the power dissipation of the devoice may be exceeded if a number of output channels are simultaneously short circuited.

CR8=1: Monitor enabled.

CR8=0 Monitor disabled (default on power-up).

CR7-CR0: These are dont care conditions.

AD5391 Control Register Contents

MSB										LSB
CR11	**CR10**	**CR9**	**CR8**	**CR7**	**CR6**	**CR5**	**CR4**	**CR3**	**CR1**	**CR0**

Table IX AD5391 Control Register

CR11: Power Down Status. This bit is used to configure the output amplifier state in power down.
CR11=1 amplifier output is high impedance (default on power up).
CR11=0 amplifier output is 100k to ground.

CR10: 3V/5V power supply operating mode. This bit conditions the DAC when operating at 3V or 5 V. With 3V supplies the internal reference is 1.25V. With 5V supplies the internal reference is 2.5V. CR12 is programmed as follows:

CR10=1: 5V condition, internal reference is 2.5V (default on power-up).
CR10=0: 3V condition, internal reference is 1.25V.

CR9: Current Boost Control. This bit is used to boost the current in the output amplifier therby altering its settling time. This bit is configured as follows:

CR9=1: Boost mode on. This maximizes the bias current in the output amplifier giving the fastest settling time (3us typ) but increasing the power dissipation.
CR9=0: Boost mode off (default on power up). This reduces the bias current in the output amplifier and reduces the overall power consumption but increases the settling time to 10us.

CR8: Internal/External Reference. This bits determines if the DAC uses its internal reference or an externally applied reference.

CR8=1: Internal Reference enabled. 1.25V with 3V supplies and 2.5V with 5V supplies.

CR8=0: External Reference selected (default on power up)

CR7: Voltage Output Monitor Enable

CR7=1: Monitor Enabled. This enables the channel monitor function. Following a write to the monitor channel in the SFR register the selected channel output is routed to the MON_OUT pin.

CR7=0: Monitor Disabled (default on power-up). When monitor is disabled the MON_OUT pin is tristated.

CR6: Thermal Monitor Function. This function is used to monitor the internal die temperature of the AD539X devices when enabled. The thermal monitor puts the device into soft power down when the temperature exceeds 130 degree C. This function can be used to protect the device in cases where the power dissipation of the devoice may be exceeded if a number of output channels are simultaneously short circuited.

CR6=1: Monitor enabled

CR6=0 Monitor disabled (default on power-up).

CR5-CR0: These are dont care conditions.

Hardware Functions

Reset Function

Bringing the RESET line low resets the contents of all internal registers to their power-on-reset state. Reset is a negative edge sensitive input. The default corresponds to m at fullscale and c at zero. The contents of all DAC registers are cleared setting the outputs to zero volts. This sequence takes 300us (typ). The falling edge *of RESET* initiates the reset process and *BUSY* goes low for the duration returning high when *RESET* is complete. While BUSY is low all interfaces are disabled and all LDAC pulses are ignored. When BUSY returns high the part resumes normal operation and the status of the RESET pin is ignored till the next falling edge is detected.

Asynchronous Clear Function

Bringing the CLR line low clears the contents of the DAC registers to the data contained in the user configurable CLR register and sets the analog outputs accordingly. This function can be used in system calibration to load zeroscale and fullscale to all channels together.The execution time for a CLR is 32us.

BUSY and LDAC Functions

BUSY is a digital cmos output indicating the status of the AD539X devices. BUSY goes low during internal calculations of x2 data. During this time the user can continue writing new data to further x1, c and m registers in parallel interface mode and these are stored in a FIFO but no updates to the DAC registers and DAC outputs will take place. If LDAC is taken low while *BUSY* is low this event is stored.

BUSY also goes low during power-on-reset and on a falling edge is detected on the *RESET* pin . During this time all interfaces are disabled and any events on *LDAC* are ignored.

The AD539X contain an extra feature whereby a DAC register is not updated unless it's x2 register has been written to since the last time LDAC was brought low. Normally, when LDAC is brought low, the DAC registers are filled with the contents of the x2 registers. However these devices will only update the DAC register if the x2 data has changed, thereby removing unnecessary digital crosstalk.

Power-On-Reset

The AD539X contain a power-on-reset generator and state-machine. The power-on-reset resets all registers to a predefined state and the analog outputs are configured with a 100k impedance to ground. The BUSY pin goes low during the power-on-reset sequencing preventing data writes to the device.

Power-Down

The AD539X contain a global power-down feature that puts all channels into a low power mode reducing both analog and digital power consumption to 5uA. In power down mode the output amplifier can be configured as a high impedance output or provide a 100k load to ground. The contents of all internal registers are retained in power-down mode. When exiting power down the settling time of the amplifier will elapse before the outputs settle to their correct value.

AD539X to MC68HC11

The Serial Peripheral Interface (SPI) on the MC68HC11 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 0 and the Clock Phase Bit (CPHA) = 1. The SPI is configured by writing to the SPI Control Register (SPCR)—see 68HC11 User Manual. SCK of the 68HC11 drives the SCLK of the AD5380, the MOSI output drives the serial data line (D_{IN}) of the AD539X and the MISO input is driven from D_{OUT}. The SYNC signal is derived from a port line (PC7). When data is being transmitted to the AD539X, the SYNC line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle.

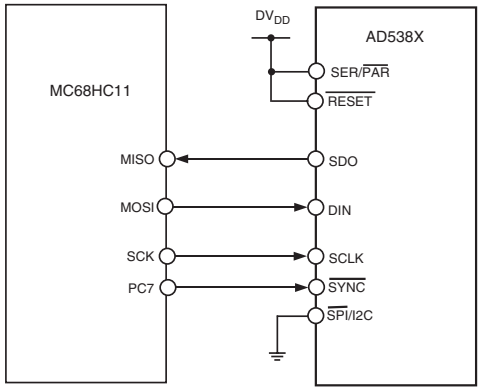


Figure 15 . AD539X -MC68HC11 Interface

AD539X to PIC16C6x/7x

The PIC16C6x/7x Synchronous Serial Port (SSP) is configured as an SPI Master with the Clock Polarity bit = 0. This is done by writing to the Synchronous Serial Port Control Register(SSPCON). See user PIC16/17 Microcontroller User Manual. In this example I/O port RA1 is being used to pulse SYNC and enable the serial port of the AD539X. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, three consecutive read/write operations are needed depending on the mode. Figure 16 shows the connection diagram.

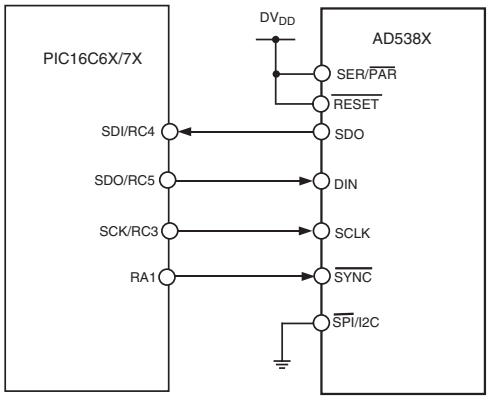


Figure 15 . AD539X -PIC16C6X/7X Interface

AD539X to 8051

The AD539X requires a clock synchronized to the serial data. The 8051 serial interface must therefore be operated in Mode 0. In this mode serial data enters and exits through RxD and a shift clock is output on TxD. Figure 17 shows how the 8051 is connected to the AD539X. Because the AD5380 shifts data out on the rising edge of the shift clock and latches data in on the falling edge, the shift clock must be inverted. The AD539X requires its data with the MSB first. Since the 8051 outputs the LSB first, the transmit routine must take this into account.

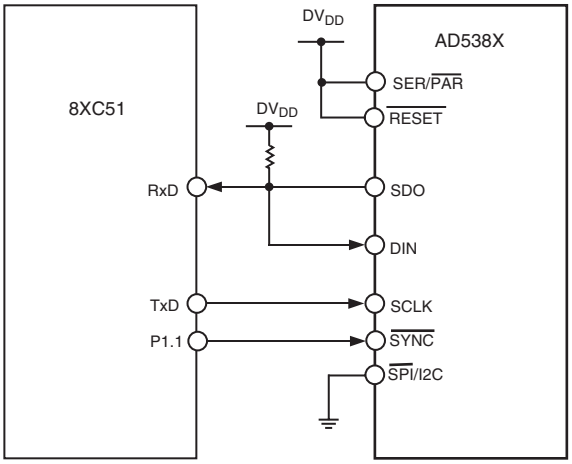


Figure 17 . AD539X - 8051 Interface

AD539X to ADSP2101/2103

Figure 18 shows a serial interface between the AD539X and the ADSP-2101/ADSP-2103. The ADSP-2101/ ADSP-2103 should be set up to operate in the SPORT Transmit Alternate Framing Mode. The ADSP-2101/ ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: Internal Clock Operation, Active Low Framing, 16-Bit Word Length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

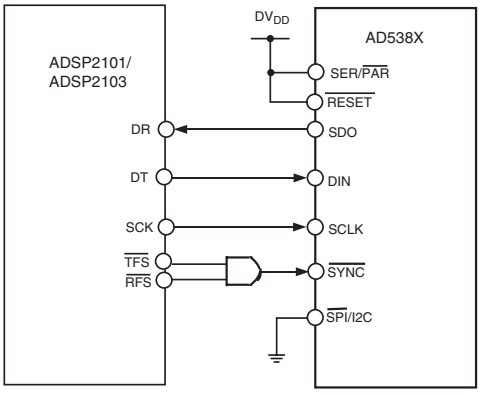


Figure 18 . AD539X - ADSP2101/03 Interface

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD539X is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the AD539X is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. For supplies with multiple pins (AV_{DD}, AV_{CC}) it is recommended to tie those pins together. The AD539X should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

The power supply lines of the AD539X should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the D_{IN} and SCLK lines will help reduce crosstalk between them (not required on a multilayer board as there will be a separate ground plane, but separating the lines will help). It is essential to minimize noise on V_{IN} and REFIN lines.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.