BURR-BROWN®

ADS852

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

SpeedPlus™ 14-Bit, 65MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **HIGH DYNAMIC RANGE:**
  High SFDR: 100dB at 20MHz f_{IN}
  High SNR: 75dB at 20MHz f_{IN}
- **PREMIUM TRACK/HOLD:**
  High Bandwidth: 1GHz
  Low Jitter: 0.25pS rms
  Differential or Single-Ended Inputs
  Selectable Full-Scale Input Range
- **FLEXIBLE CLOCKING:**
  Differential or Single-Ended
  Accepts Sine or Square Wave Clocking Down to 0.5Vp-p
  Variable Threshold Level

APPLICATIONS

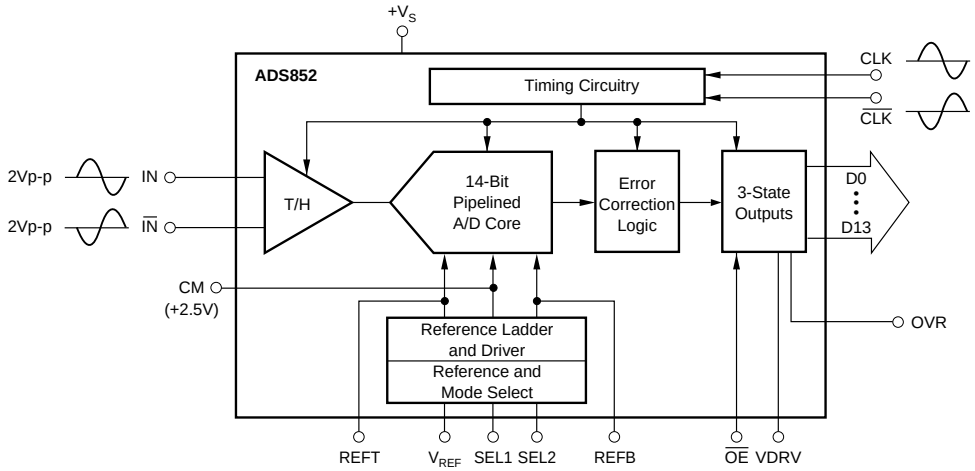
- **BASESTATION WIDEBAND RADIOS: CDMA, GSM, TDMA, 3G, AMPS, NMT**
- **TEST INSTRUMENTATION**
- **CCD IMAGING**

DESCRIPTION

The ADS852 is a high-dynamic range 14-bit, 65MHz pipelined analog-to-digital converter. It includes a high-bandwidth linear track/hold that gives excellent spurious performance up to and beyond the Nyquist rate. This high-bandwidth track/hold also has a low jitter of only 0.25pS rms, leading to excellent SNR performance. The clock input can accept a low level differential sine wave or square wave signal down to 0.5Vp-p, further improving the SNR performance. It also accepts a single-ended clock signal and has flexible threshold levels.

The ADS852 has a 4Vp-p differential input range (2Vp-p x 2 inputs, +16dBm) for optimum signal-to-noise ratio. The differential operation gives the lowest even-order harmonic components. A lower input voltage of 3Vp-p or 2Vp-p can also be selected using the internal references, further optimizing SFDR. Alternatively, a single-ended input range can be used by tying the IN input to the common-mode voltage if desired.

The ADS852 also provides an over-range flag that indicates when the input signal has exceeded the converter's full-scale range. This flag can also be used to reduce the gain of the front end signal conditioning circuitry. It also employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. The ADS852 is available in a small 48-lead TQFP package.



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SPECIFICATIONS

At T_A = full specified temperature range, differential input range = 1.5V to 3.5V, sampling rate = 65MHz, and external reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS852Y MIN	ADS852Y TYP	ADS852Y MAX	UNITS
RESOLUTION			14 Guaranteed		Bits
SPECIFIED TEMPERATURE RANGE	Ambient Air		–40 to +85		°C
ANALOG INPUT					
Standard Differential Input Range	(2Vp-p x 2, +16dBm)	1.5		3.5	V
Optional Single-Ended Input Range	4Vp-p	0.5		4.5	V
Common-Mode Voltage			2.5		V
Optional Input Ranges	Selectable		2Vp-p (+10dBm) or 3Vp-p (+13dBm)		V
Analog Input Bias Current			1		µA
Track-Mode Input Bandwidth	–3dBFS		1		GHz
Input Impedance			1.25 || 9		MΩ || pF
CONVERSION CHARACTERISTICS					
Sample Rate		1M		65M	Samples/s
Data Latency			7		Clk Cyc
DYNAMIC CHARACTERISTICS					
Differential Linearity Error (largest code error)					
f = 2.2MHz			±0.5	±1.0	LSB
f = 20MHz			±0.5		LSB
No Missing Codes			Guaranteed		
Integral Nonlinearity Error, f = 1MHz			±0.5	±2.0	LSBs
Spurious Free Dynamic Range[1]					
f = 2.2MHz			105		dBFS[2]
f = 20MHz			100		dBFS
f = 31MHz			100		dBFS
Two-Tone Intermodulation Distortion[3]					
f = 4.5MHz and 5.5MHz (–7dB each tone)			–95		dBc
Signal-to-Noise Ratio (SNR)					
f = 2.2MHz			75		dBFS
f = 20MHz			75		dBFS
f = 31MHz			75		dBFS
Signal-to-(Noise + Distortion) (SINAD)					
f = 2.2MHz			75		dB
f = 20MHz			75		dB
f = 31MHz			74		dBFS
Output Noise	Input Grounded		TBD		LSBs rms
Aperture Delay Time			3		ns
Aperture Jitter			0.25		ps rms
Overvoltage Recovery Time			2		ns
Full-Scale Step Acquisition Time			5		ns
DIGITAL INPUTS					
Convert Command (Start Conversion)	Rising Edge of Convert Clock	+0.5		$+V_S$	Vp-p
Logic Family (Other Clock Inputs)			+3V/+5V Logic Compatible CMOS		
High Level Input Current[4] (V_{IN} = 5V)				100	µA
Low Level Input Current (V_{IN} = 0V)				10	µA
High Level Input Voltage		+2.0			V
Low Level Input Voltage				+1.0	V
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Logic Family			+3V/+5V Logic Compatible CMOS		
Logic Coding			Straight Offset Binary		
Low Output Voltage (I_{OL} = 50µA to 1.6mA)	VDRV = 3V			+0.2	V
High Output Voltage, (I_{OH} = 50µA to 0.5mA)		+2.5			V
Low Output Voltage, (I_{OL} = 50µA to 1.6mA)	VDRV = 5V			+0.2	V
High Output Voltage, (I_{OH} = 50µA to 1.6mA)		+2.5			V
3-State Enable Time	$\overline{OE}$ = L		20	40	ns
3-State Disable Time	$\overline{OE}$ = H		2	10	ns
Output Capacitance			5		pF
ACCURACY (Internal Reference, = 2V, Unless Otherwise Noted)					
Zero Error (Referred to –FS)	at 25°C		0.5	3.0	%FS
Zero Error Drift (Referred to –FS)			12		ppm/°C
Gain Error[5]	at 25°C		±1.5	±2.5	%FS
Gain Error Drift[5]			38		ppm/°C
Gain Error[6]	at 25°C		±0.75	±1.5	%FS
Gain Error Drift[6]			20		ppm/°C
Power Supply Rejection of Gain	ΔV_S = ±5%		68		dB
Internal REF Tolerance	Deviation from Ideal		±10	±50	mV
External REF Voltage Range		0.9	2	2.025	V
Reference Input Resistance			1.0		kΩ

SPECIFICATIONS (CONT)

At T_A = full specified temperature range, differential input range = 1.5V to 3.5V, sampling rate = 65MHz, and external reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS852Y			UNITS
		MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS					
Supply Voltage: $+V_S$	Operating	+4.75	+5.0	+5.25	V
Supply Current: $+I_S$	Operating		120		mA
Output Driver Supply Current (VDRV)			12		mA
Power Dissipation: VDRV = 5V			670	740	mW
VDRV = 3V			650	720	mW
Power Down	Operating		20		mW
Thermal Resistance, θ_{JA}					
48-Lead TQFP					°C/W

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full Scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) A 50kΩ pull-down resistor is inserted internally. (5) Includes internal reference. (6) Excludes internal reference.

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	(–0.3V) to ($+V_S$ +0.3V)
Logic Input	(–0.3V) to ($+V_S$ +0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
ADS852Y	48-Lead TQFP	xxx	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

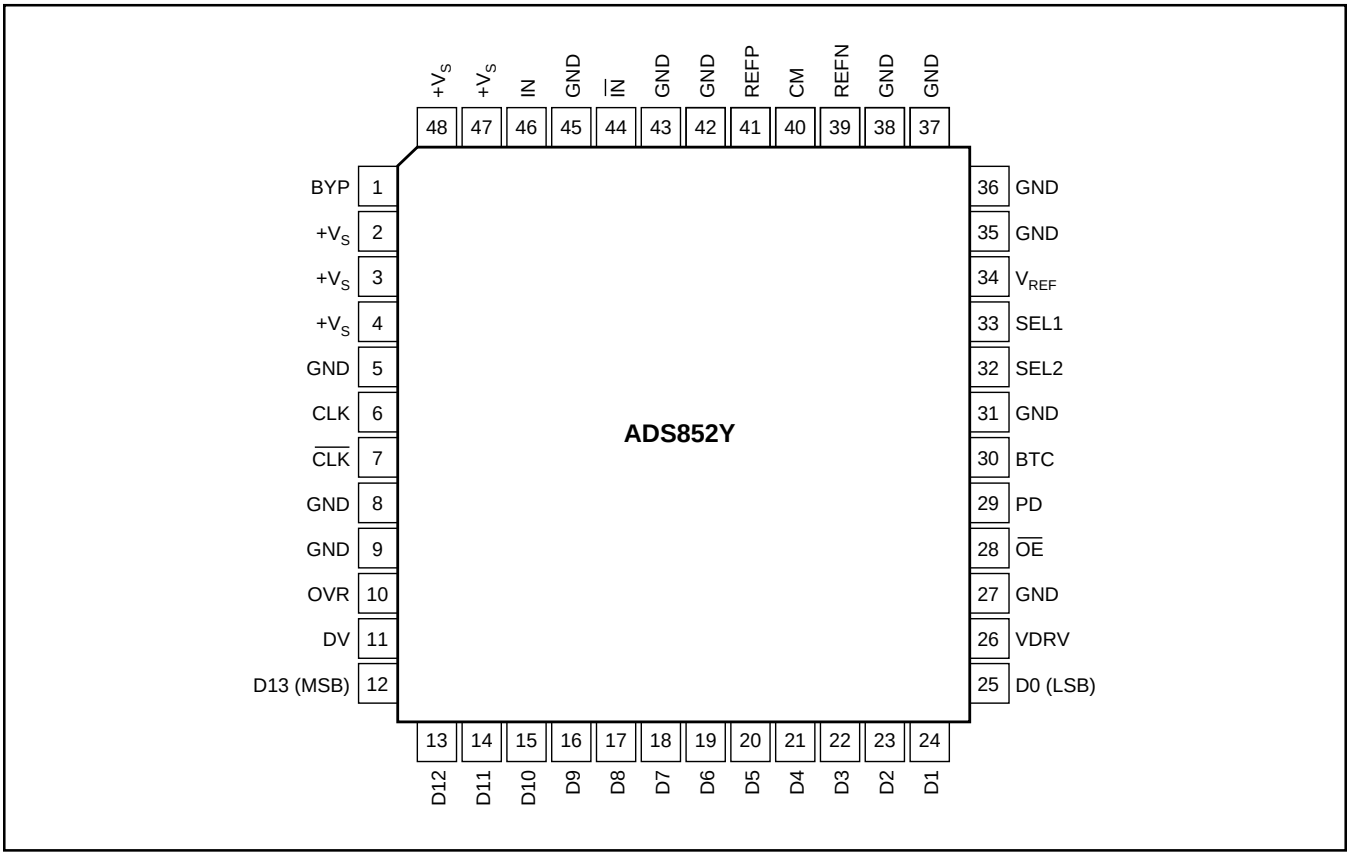
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

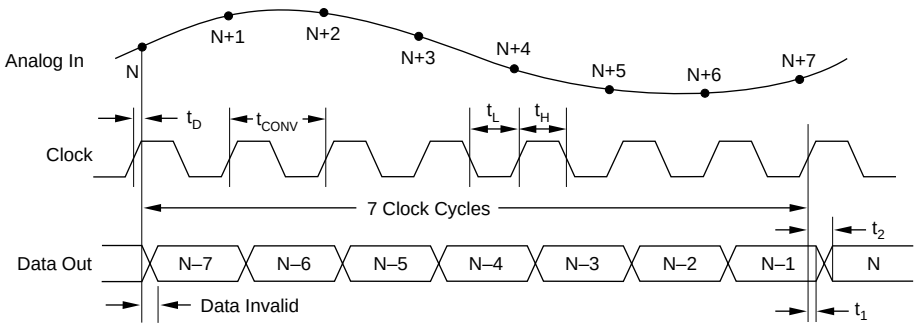
PIN DESCRIPTIONS

PIN	I/O	DESIGNATOR	DESCRIPTION	PIN	I/O	DESIGNATOR	DESCRIPTION
1		BYP	Bypass Point	26		VDRV	Output Bit Driver Voltage Supply
2		$+V_S$	Supply Voltage	27		GND	Ground
3		$+V_S$	Supply Voltage	28		$\overline{OE}$	Output Enable: HI = High Impedance;
4		$+V_S$	Supply Voltage				LO or Floating: Normal Operation
5		GND	Ground	29	I	PD	Power Down: HI = Power Down; LO = Normal
6	I	CLK	Clock Input	30	I	BTC	HI = Binary Two's Complement;
7	I	$\overline{CLK}$	Complementary Clock Input				LO = Straight Binary
8		GND	Ground	31		GND	Ground
9		GND	Ground	32		SEL2	Reference Select 2: See Table
10	O	OVR	Overrange Indicator	33		SEL1	Reference Select 1: See Table
11	O	DV	Data Valid Pulse: HI = Data Vaild	34		V_{REF}	Internal Reference Voltage
12	O	D13	Most Significant Bit (MSB)	35		GND	Ground
13	O	D12	Data Bit 12	36		GND	Ground
14	O	D11	Data Bit 11	37		GND	Ground
15	O	D10	Data Bit 10	38		GND	Ground
16	O	D9	Data Bit 9	39		REFN	Bottom Reference Voltage Bypass
17	O	D8	Data Bit 8	40		CM	Common-Mode Voltage (mid-scale)
18	O	D7	Data Bit 7	41		REFP	Top Reference Voltage Bypass
19	O	D6	Data Bit 6	42		GND	Ground
20	O	D5	Data Bit 5	43		GND	Ground
21	O	D4	Data Bit 4	44	I	$\overline{IN}$	Complementary Analog Input
22	O	D3	Data Bit 3	45		GND	Ground
23	O	D2	Data Bit 2	46	I	IN	Analog Input
24	O	D1	Data Bit 1	47		$+V_S$	Supply Voltage
25	O	D0	Least Significant Bit (LSB)	48		$+V_S$	Supply Voltage

PIN DIAGRAM



TIMING DIAGRAM



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	15.4		1µs	ns
t_L	Clock Pulse Low	7.6	$t_{CONV}/2$		ns
t_H	Clock Pulse High	7.6	$t_{CONV}/2$		ns
t_D	Aperture Delay		3		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12	ns

TABLE, REFERENCE/FULL SCALE RANGE SELECT

DESIRED FULL SCALE RANGE	SEL1	SEL2	INTERNAL V_{REF}
4Vp-p (2Vp-p x 2, +16dBm)	GND	GND	2V
3Vp-p (1.5Vp-p x 2, +13dBm)	GND	$+V_S$	1.5V
2Vp-p (1Vp-p x 2, +10dBm)	V_{REF}	GND	1V

For External Reference Operation, tie V_{REF} to $+V_S$, the full scale range will be 2X the reference value. For instance, selecting a 2V External Reference will set the full scale values of 1.5V to 3.5V for both IN and $\overline{IN}$ inputs.