CMOS
165 MHz, Triple 8-Bit Video RAM-DAC

ADV458

FEATURES
165 MHz Pseudo-Color Operation
Triple 8-Bit D/A Converters
***Triple* 256 × 8 (256 × 24) Color Palette RAM**
Triple 4 × 8 (4 × 24) Overlay Registers
Compatible to Brooktree BT458
RS-343A/RS-170 Compatible Analog Outputs
TTL Compatible Digital Inputs
Bit Plane Read and Blink Masks
Standard 8-Bit MPU I/O Interface:
Multiplexed Pixel Input Ports; 4:1 or 5:1
+5 V CMOS Monolithic Construction
84-Pin PLCC Package

AVAILABLE CLOCK RATES
165 MHz
135 MHz
110 MHz
80 MHz

APPLICATIONS
High Resolution Color Graphics
Video Reconstruction

GENERAL DESCRIPTION

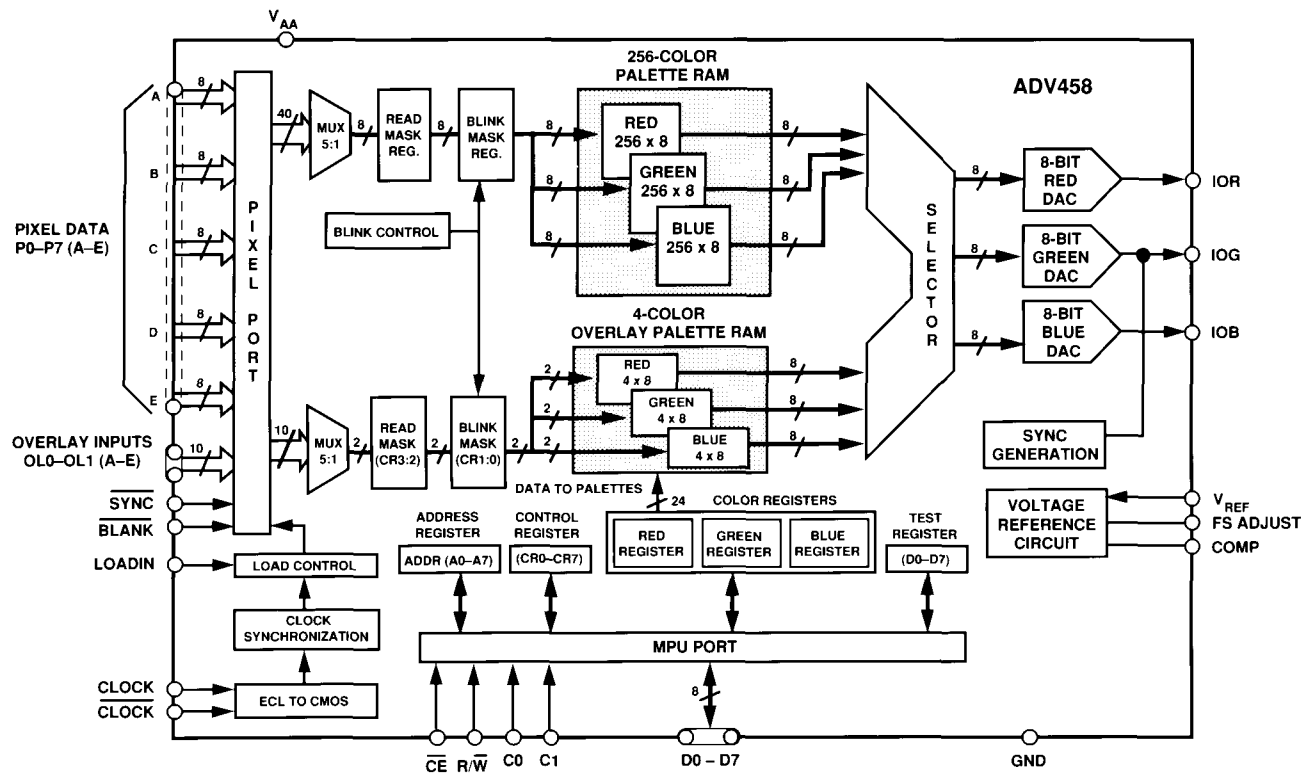
The ADV458 is a complete analog output, video RAM-DAC on a single CMOS monolithic chip. The part is specifically designed for use in the graphics systems of high performance, color graphics workstations. The ADV458 integrates a number of graphic functions onto one device allowing 8-bit Pseudo-Color operation with an additional 2 bits of overlay information at the maximum screen update rate of 165 MHz.

The device consists of three, high speed, 8 bit, video D/A converters (RGB), three 256 × 8 (one 256 × 24) look-up tables, a pixel input data multiplexer/serializer and three 4 × 8 (one 4 × 24) overlay registers. The ADV458 is capable of 4:1 or 5:1 multiplexing. The part is controlled through the MPU port by the on-board command register. The part also contains an on-board test register, associated with self diagnostic testing of the device.

Pseudo-Color image rendition, at speeds of up to 165 MHz, is achieved through the use of the on-board data multiplexer/serializer. The pixel input port's flexibility allows for direct interface to most standard frame buffer memory configurations, including general purpose DRAM and VRAM designs.

(Continued on Page 4)

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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ADV458—SPECIFICATIONS (V_{AA}[1] = +5 V; V_{REF} = +1.235 V; R_L = 37.5 Ω; C_L = 10 pF; R_{SET} = 523 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted).

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	
Coding		Binary	
DIGITAL INPUTS (excluding CLOCK, $\overline{CLOCK}$)			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	10	pF max	
CLOCK INPUTS (CLOCK, $\overline{CLOCK}$)			
Differential Input Voltage, ΔV_{IN}	0.6	V min	
	6	V max	
Input Current, I_{IN}	±1	μA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	10	pF max	
DIGITAL OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	
Output Low Voltage, V_{OL}	0.4	V max	
Floating-State Leakage Current	10	μA max	
Floating-State Output Capacitance	10	pF typ	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05 mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44 mA
	1.90	mA max	
Blank Level on IOR, IOG	0	μA min	Typically 5 μA
	50	μA max	
Blank Level on IOG or I_{OUT}	6.29	mA min	Typically 7.62 mA
	8.96	mA max	
Sync Level on IOG or I_{OUT}	0	μA min	Typically 5 μA
	50	μA max	
LSB size	17.22	μA typ	
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	−0.5	V min	
	+1.2	V max	
Output Impedance, R_{OUT}	50	kΩ typ	
Output Capacitance, C_{OUT}	20	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.20 /1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	10	μA typ	
POWER REQUIREMENTS			
V_{AA}	5	V nom	
I_{AA}[3]	370	mA max	165 MHz Parts, Typically 300 mA
I_{AA}	340	mA max	135 MHz Parts, Typically 230 mA
I_{AA}	315	mA max	110 MHz Parts, Typically 200 mA
I_{AA}	285	mA max	80 MHz Parts, Typically 180 mA
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%: f = 1 kHz, COMP = 0.1 μF
DYNAMIC PERFORMANCE			
Clock and Data Feedthrough[4]	−30	dB typ	
Glitch Impulse	50	pV secs typ	
DAC-to-DAC Crosstalk[5]	−23	dB typ	

NOTES

[1]±5% for all versions.

[2]Temperature Range (T_{MIN} to T_{MAX}); 0°C to +70°C; T_J (Silicon Junction Temperature) ≤ 105°C.

[3]Pixel Port is continuously clocked with data corresponding to a linear ramp.

[4]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough. TTL input values are 0 to 3 volts, with input rise/fall times ≤4 ns, measured the 10% and 90% points. Timing reference points at 50% for inputs and outputs.

[5]DAC-to-DAC Crosstalk is measured by holding one DAC high while the other two are making low to high and high to low transitions.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{AA}[2] = +5 V; V_{REF} = +1.235 V; R_L = 37.5 Ω; C_L = 10 pF; R_{SET} = 523 Ω. All specifications T_{MIN} to T_{MAX}[3] unless otherwise noted.)

MPU PORT[4, 5]

Parameter	165 MHz Version	135 MHz Version	110 MHz Version	80 MHz Version	Units	Conditions/Comments
t_1	0	0	0	0	ns min	R/$\overline{W}$, C0, C1 to $\overline{CE}$ Setup Time
t_2	15	15	15	15	ns min	R/$\overline{W}$, C0, C1 to $\overline{CE}$ Hold Time
t_3	45	45	45	45	ns min	$\overline{CE}$ Low Time
t_4	25	25	25	25	ns min	$\overline{CE}$ High Time
t_5	7	7	7	7	ns min	$\overline{CE}$ Asserted to Databus Driven[4]
t_6	45	45	45	45	ns max	$\overline{CE}$ Asserted to Data Valid[4]
t_7	15	15	15	15	ns max	$\overline{CE}$ Disabled to Databus Three-Stated[5]
	5	5	5	5	ns typ	
t_8	35	35	35	35	ns min	Write Data (D0–D7) Setup Time
t_9	3	3	3	3	ns min	Write Data (D0–D7) Hold Time

CLOCK CONTROL & PIXEL PORT[6]

Parameter	165 MHz Version	135 MHz Version	110 MHz Version	80 MHz Version	Units	Condition/Comments
f_{CLOCK}	165	135	110	80	MHz max	Pixel CLOCK Rate
f_{LD}	41.25	33.75	27.5	20	MHz max	LD Clock Rate
t_{10}	24.24	29.63	36.36	50	ns min	LD Cycle Time
t_{11}	10	12	15	20	ns min	LD Pulse High Time
t_{12}	10	12	15	20	ns min	LD Pulse Low Time
t_{13}	3	3	3	4	ns min	Pixel Data Setup Time
t_{14}	2	2	2	2	ns min	Pixel Data Hold Time
t_{15}	6.06	7.4	9.09	12.5	ns min	Pixel CLOCK Cycle Time
t_{16}	2.6	3	4	5	ns min	Pixel CLOCK High Time
t_{17}	2.6	3	4	5	ns min	Pixel CLOCK Low Time

ANALOG OUTPUTS[7]

Parameter	165 MHz Version	135 MHz Version	110 MHz Version	80 MHz Version	Units	Conditions/Comments
t_{18}	12	12	12	12	ns typ	Analog Output Delay
t_{19}	2	2	2	2	ns typ	Analog Output Rise/Fall Time
t_{20}	8	8	8	8	ns max	Analog Output Settling Time
t_{SK}	0	0	0	0	ns typ	Analog Output Skew
	2	2	2	2	ns max	

NOTES

[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL inputs (CLOCK, $\overline{CLOCK}$) are V_{AA} − 0.8 V to V_{AA} − 1.8 V, with input rise/fall times ≤ 2 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF. Databus (D0–D7) loaded as shown in Figure 1.

[2]+5% for all versions.

[3]Temperature Range (T_{MIN} to T_{MAX}); 0°C to +70°C, T_J (Silicon Junction Temperature) ≤ 105°C.

[4]t_5 and t_6 are defined as the time required for an output to cross 0.4 V or 2.4 V.

[5]t_7 is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging the 100 pF capacitor. This means that the time, t_7, quoted in the Timing Characteristics is the true value for the device and as such is independent of external databus loading capacitances.

[6]Pixel Port consists of the following inputs:

Pixel Inputs:	P0-P7 [A, B, C, D, E]
Overlay Control:	OL0-OL1 [A, B, C, D, E]
Pixel Controls:	$\overline{SYNC}$, $\overline{BLANK}$
Clock Inputs:	CLOCK, $\overline{CLOCK}$, $\overline{LD}$

[7]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition. Output rise/fall time measured between the 10% and 90% points of full-scale transition. Settling time measured from the 50% point of full-scale transition to the output remaining within ± 1 LSB (Settling time does not include clock and data feedthrough).

Specifications subject to change without notice.

(Continued from Page 1)

The ADV458 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

Test diagnostic circuitry has been included to complement the users system level debugging.

Other features include programmable blink rates, bit plane masking and bit plane blinking.

The ADV458 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation.

The ADV458 is packaged in an 84-pin plastic leaded chip carrier package (PLCC).

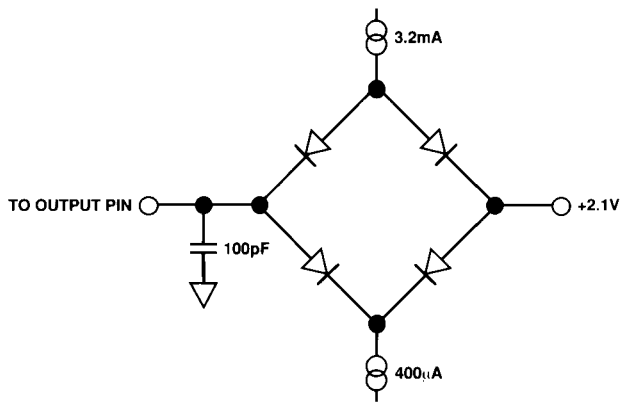


Figure 1. Load Circuit for Databus Access and Relinquish Times

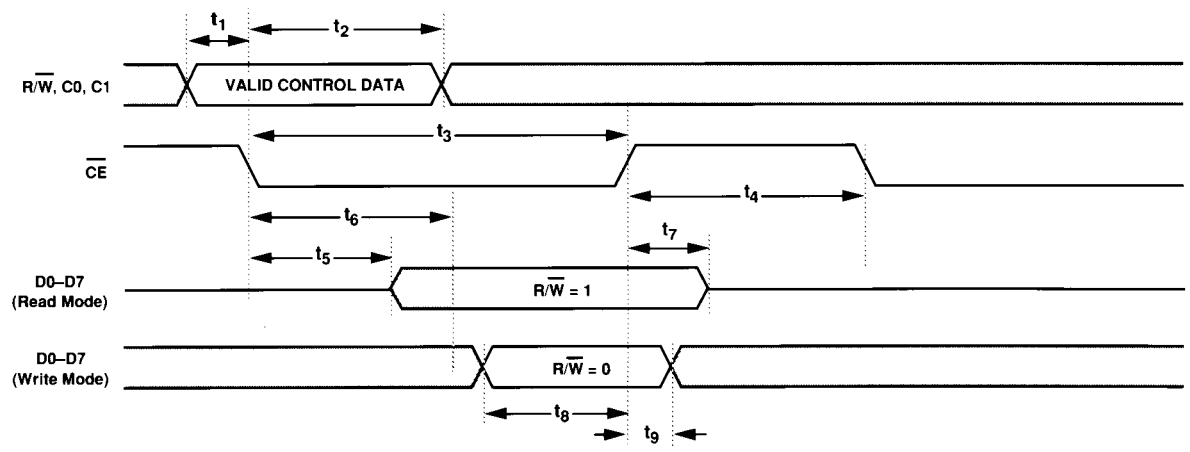


Figure 2. Microprocessor Port (MPU) Interface Timing

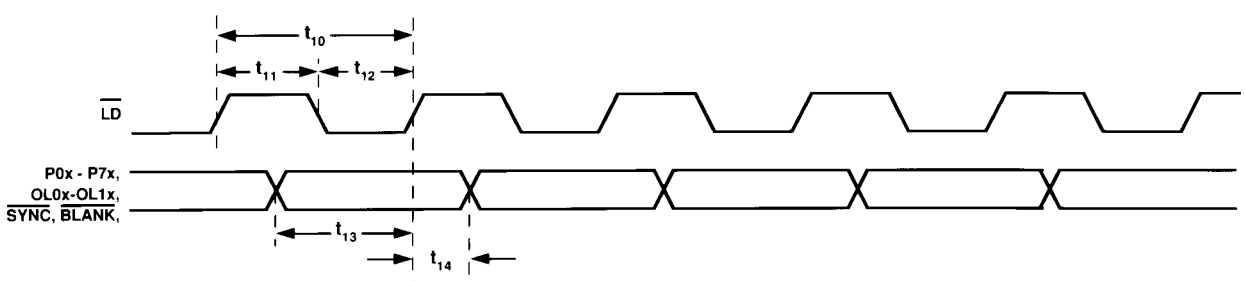
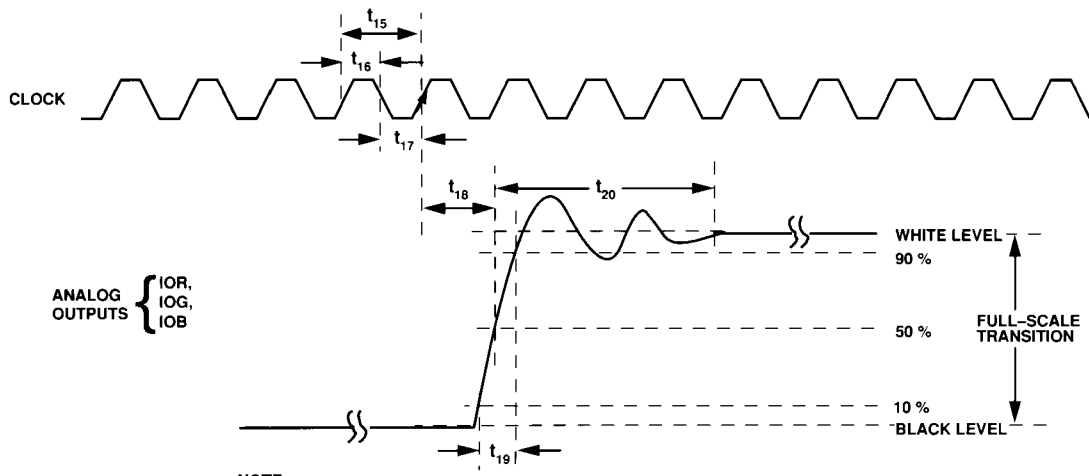


Figure 3. Pixel Data vs. $\overline{LD}$ Timing



NOTE:
THIS DIAGRAM IS NOT TO SCALE. FOR THE PURPOSES OF CLARITY,THE ANALOG OUTPUT WAVEFORM IS MAGNIFIED IN TIME AND AMPLITUDE W.R.T. THE CLOCK WAVEFORM.

Figure 4. Analog Output Response vs. CLOCK

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temp	T_A	0		+70	°C
Reference Voltage	V_{REF}	1.20	1.235	1.26	Volts
Output Load	R_L		37.5		Ω

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV458 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . . 7 V
Voltage on any Digital Pin . . . GND − 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) . . . . . −55°C to +125°C
Storage Temperature (T_S) . . . . . −65°C to +150°C
Junction Temperature (T_J) . . . . . +150°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C
Vapor Phase Soldering (1 minute) . . . . . +220°C
Analog Outputs to GND[2] . . . . . GND − 0.5 to V_{AA}

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING GUIDE[1, 2]

SPEED			
165 MHz	135 MHz	110 MHz	80 MHz
ADV458KP165	ADV458KP135	ADV458KP110	ADV458KP80

NOTES
[1]ADV458 is packaged in an 84-pin plastic leaded chip carrier, PLCC.
[2]All devices are specified for 0°C to +70°C operation.

PIN FUNCTION DESCRIPTION

P0A...P0E–P7A..P7E	Pixel Port (TTL Compatible Inputs): There are 40 pixel inputs which are multiplexed at a 4:1 or a 5:1 rate. Each group of eight inputs, P0x–P7x, constitutes one pixel. These entries address the RAM Look Up Table which provides the color information for the DACs. They are latched on the rising edge of $\overline{LD}$. Unused inputs should be connected to GND. The A pixel is displayed first, followed by the B pixel, etc., until all four or five pixels have been output, at which point the cycle repeats.
OL0A...OL1A–OL0E...OL1E	Overlay Select (TTL Compatible Inputs): These control inputs are used in conjunction with Bit 6 of the command register to specify which color palette is to be used to provide color information for the DACs. They are latched on the rising edge of $\overline{LD}$. Each group of two inputs OL0x–OL1x constitutes one overlay pixel. Unused inputs should be connected to GND. When accessing the overlay palette the P0x–P7x pixel inputs are ignored. The Palette color used is determined as per Table I:

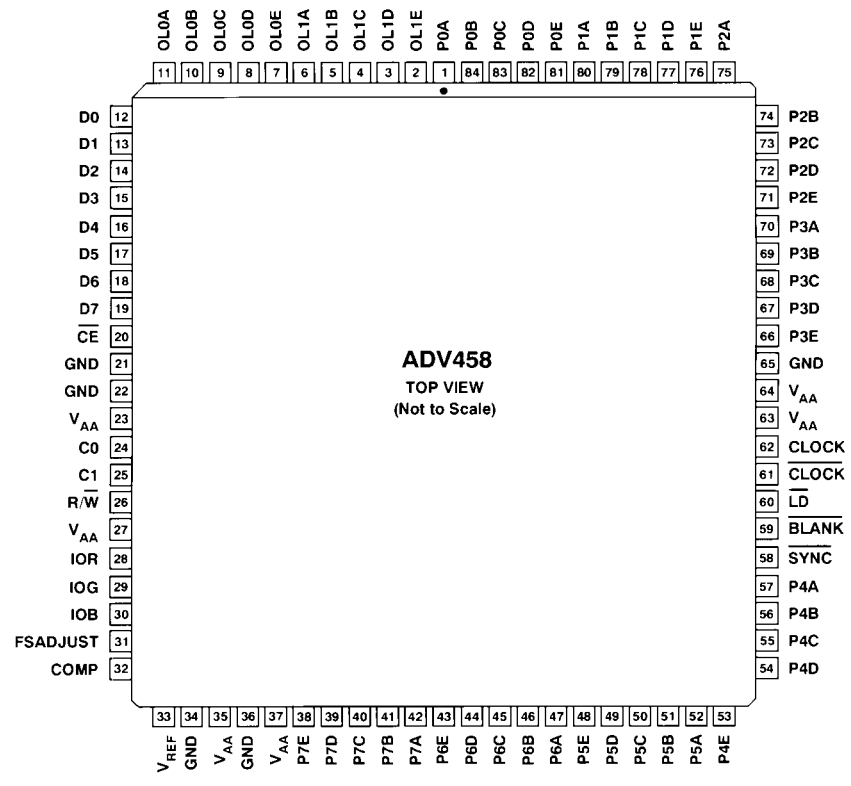
Table I. Palette and Overlay Select Truth Table

OL1	OL0	CR6 = 1	CR6 = 0
0	0	Color Palette RAM	Overlay Color 0
0	1	Overlay Color 1	Overlay Color 1
1	0	Overlay Color 2	Overlay Color 2
1	1	Overlay Color 3	Overlay Color 3

$\overline{LD}$	Pixel Data Load Input (TTL Compatible Input): This input latches the serialized pixel data, including $\overline{SYNC}$, $\overline{BLANK}$ and OL0x–OL1x into the device. $\overline{LD}$ runs at either one quarter or one fifth the frequency of CLK.
CLOCK, $\overline{CLOCK}$	Clock Inputs (ECL Compatible Inputs): These differential clock inputs are designed to be driven by ECL logic levels configured for single supply (+5 V) operation. The clock rate is normally the pixel clock rate of the system.
$\overline{BLANK}$	Composite Blank (TTL Compatible Input): This video control signal drives the analog outputs to the blanking level. It is latched on the rising edge of $\overline{LD}$. When $\overline{BLANK}$ is a logical zero, the pixel and overlay inputs are ignored.
$\overline{SYNC}$	Composite-Sync (TTL Compatible Input): This video control signal drives the IOG analog output to the sync level by switching off a 40 IRE current source on the output when $\overline{SYNC}$ is at a logical zero. As $\overline{SYNC}$ does not override any other control or data input, it should only be asserted during the blanking period. It is latched on the rising edge of $\overline{LD}$. If sync information is not to be generated on the IOG output then $\overline{SYNC}$ should be connected to GND.
D0–D7	Databus (TTL Compatible Input/Output Bus): Data, including color palette values and device control information is written to and read from the device over this 8-bit, bidirectional databus. D0 is the least significant bit.
$\overline{CE}$	Chip Enable (TTL Compatible Input): This input must be at logic "0" when writing to or reading from the device over the databus (D0–D7). Internally, data is latched on the rising edge of $\overline{CE}$ during write operations. Care should be taken to avoid glitches on this input.
R/$\overline{W}$	Read/Write Control (TTL Compatible Input): This input determines whether data is written to or read from the device's registers and color palette RAM. R/$\overline{W}$ and $\overline{CE}$ must be at logic "0" to write data to the part. R/$\overline{W}$ must be at logic "1" and $\overline{CE}$ at logic "0" to read from the device. R/$\overline{W}$ is latched on the falling edge of $\overline{CE}$.
C0, C1	Command Controls (TTL Compatible Inputs): These inputs determine the type of read or write operation being performed on the device over the databus. (See Interface Truth Table.) Data on these inputs is latched on the falling edge of $\overline{CE}$.
IOR, IOG, IOB	Red, Green & Blue Current Outputs (High Impedance Current Sources): These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into doubly terminated 75 Ω loads.
V_{REF}	Voltage Reference Input (Analog Input): An external 1.235 V (typical) voltage reference is required to drive this input. The use of an AD589 (2-terminal voltage reference) is recommended. This pin should be decoupled to V_{AA} with a 0.1 μF capacitor. If V_{AA} is excessively noisy, then better performance may be obtained by decoupling this pin to GND. The decoupling capacitor must be kept as close to the device as possible to keep lead lengths to an absolute minimum. (Note: It is not recommended to use a resistor network to generate the voltage reference.)

FS ADJUST	Output Full-Scale Adjust Control (Analog Input): A resistor connected between this pin and analog ground controls the absolute amplitude of the output video signal. Note that IRE relationships are maintained, regardless of the full-scale output current. To maintain RS-343A video output levels into a doubly terminated 75 Ω load, R_{SET} = 523 Ω. The relationship between R_{SET} and the full scale output current on IOG is: $R_{SET}\,(\Omega) = 11{,}294 \times V_{REF}\,(V) / IOG\,(mA)$ The full-scale output current on IOR and IOB for a given R_{SET} is: $IOR,\ IOB\,(mA) = 8{,}067 \times V_{REF}\,(V) / R_{SET}\,(\Omega)$
COMP	Compensation Pin: A 0.1 μF capacitor should be connected between this pin and V_{AA}. The capacitor should be mounted as close as possible to the device to minimize lead length and hence, stray inductance. This pin provides compensation for the internal reference amplifier.
V_{AA}	Power Supply (+5 V ± 5%). The part contains multiple power supply pins, all should be connected together to one common +5 V filtered analog power supply.
GND	Analog Ground. The part contains multiple ground pins, all should be connected together to the system's ground plane.

PIN CONFIGURATION



CIRCUIT DETAILS AND OPERATION

As illustrated in the functional block diagram, the ADV458 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual port color palette RAM and dual port overlay registers allow color updating without contention with the display refresh process.

As illustrated in Table II, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register, color palette RAM entry, or overlay register will be accessed by the MPU.

The 8-bit address register (ADDR0-7) is used to address to internal RAM and registers. ADDR0 corresponds to D0 and is the least significant bit.

Table II. Address Register (ADDR) Operation

ADDR0-7	C1	C0	Addressed by MPU
xxH	0	0	Address Register
00H-FFH	0	1	Color Palette RAM
00H	1	1	Overlay Color 0
01H	1	1	Overlay Color 1
02H	1	1	Overlay Color 2
03H	1	1	Overlay Color 3
04H	1	0	Read Mask Register
05H	1	0	Blink Mask Register
06H	1	0	Command Register
07H	1	0	Control/Test Register

Reading/Writing Color Data

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (eight bits each of red, green and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word. This color value is then written to the location pointed at by the address register. The address register then increments to the next location. The MPU may modify this location by writing another sequence of red, green and blue data, without accessing the address register.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles to read red, green and blue data, using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location. The MPU may now read the next set of red, green and blue data.

When accessing the color palette RAM, the address register resets to 00H after a blue read or write cycle to location FFH. When accessing the overlay registers, the address register increments to 04H after a blue read or write cycle to overlay register 3. To keep track of the red, green and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to zero after the MPU reads or writes to the address register. The MPU does not have access to these two bits. The other eight bits (ADDR0–ADDR7) are accessible to the MPU.

Additional Information

Although the color palette RAM and overlay registers are dual ported, it is possible for one or more of the pixels on the display screen to be disturbed if the pixel or overlay data is accessing the same palette entry being written to by the MPU during the write cycle. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

The control registers are accessed through the address register in conjunction with the C0 and C1 inputs. The control registers can be written to and read from over the MPU interface at any time. Read or write cycles to the control registers do not increment the address register at any time. This allows read-modify-write operations on the control registers.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Pixel Interface

The ADV458 enables pixel data to be transferred from the frame buffer to the DACs at TTL data rates, by incorporating internal multiplexers and latches. Data is latched into the part on the rising edge of $\overline{LD}$ (see Figure 3). The data consists of either four or five sets of 8-bit pixel data and 2-bit overlay data and $\overline{SYNC}$ and $\overline{BLANK}$ information. With this configuration $\overline{BLANK}$ and $\overline{SYNC}$ can only be controlled to four or five pixel resolution. The $\overline{LD}$ signal is typically used to clock external circuitry to generate basic video timing.

Each clock cycle, the ADV458 outputs color information based on the [A] inputs, followed by the [B] inputs and so on until four or five pixels have been displayed. The cycle then repeats itself.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character or cursor generation logic.

To simplify the frame buffer interface timing, $\overline{LD}$ may be phase shifted by any amount with respect to CLOCK. This enables $\overline{LD}$ to be derived by externally dividing CLOCK by four or five, independent of the propagation delays of the $\overline{LD}$ generation logic. As a result, the pixel and overlay data are latched on the rising edge of $\overline{LD}$, independent of the clock phase.

A LOAD signal that is synchronous to CLOCK is maintained by internal logic and is guaranteed to follow the $\overline{LD}$ signal by at least one and not more than four clock cycles. This LOAD signal transfers the latched data into a second set of latches which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, then only one rising edge of $\overline{LD}$ should occur every four clock cycles. If 5:1 multiplexing is specified, then only one rising edge of $\overline{LD}$ should occur every five clock cycles. Otherwise the internal LOAD generation circuitry assumes it is not locked onto the $\overline{LD}$ signal and will continuously attempt to resynchronize itself to $\overline{LD}$.

Color Selection

Each clock cycle, 8 bits of color information (P0–P7) and 2 bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask and command registers. Through the use of the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e., in the middle of the screen), the ADV458 monitors the $\overline{\text{BLANK}}$ input to determine vertical retrace intervals. A vertical retrace interval is recognized as an interval during which $\overline{\text{BLANK}}$ has been low for at least 256 $\overline{\text{LD}}$ cycles.

The processed pixel data is then used to select which color palette entry of overlay register is to provide color information. Note that P0 is the LSB when accessing the color palette RAM. Table III illustrates the truth table used for color selection.

Table III. Palette and Overlay Select Truth Table

CR6	OL1	OL0	P0-P7	Addressed by Frame Buffer
1	0	0	00H	Color Palette Entry 00H
1	0	0	01H	Color Palette Entry 01H
:	:	:	:	:
1	0	0	FFH	Color Palette Entry FFH
0	0	0	xxH	Overlay Color 0
x	0	1	xxH	Overlay Color 1
x	1	0	xxH	Overlay Color 2
x	1	1	xxH	Overlay Color 3

Video Generation

Every clock cycle, the selected color information from the color palette RAM or overlay registers is presented to the D/A converters.

The $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications.

The varying output current from each of the D/A converters produces a corresponding voltage level across the termination resistors which is used to drive the color CRT monitor. Note that only the green output (IOG) contains $\overline{\text{SYNC}}$ information. Table IV details how the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs modify the output levels.

The D/A converters on the ADV458 use a segmented architecture in which bit currents are routed to either the current output of GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on and off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An additional on-chip operational amplifier stabilizes the D/A converter's full-scale output current against temperature and power supply variations.

INTERNAL REGISTERS

Command Register

The command register may be written to or read from at any time and is not initialized at power on. CR0 corresponds to databus bit D0.

CR7 Multiplex Select

This bit specifies the multiplexing rate used by pixel and overlay inputs of the ADV458. If 4:1 multiplexing is specified, then the (E) pixel and overlay inputs should be connected to GND and the $\overline{\text{LD}}$ input should be one quarter the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used and the $\overline{\text{LD}}$ input should be one fifth the CLOCK rate.

CR6 RAM Enable

When the overlay inputs are 00 this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.

CR5, CR4 Blink Rate Selection

These bits control the blink rate cycle time and duty cycle and are specified as the number of vertical retrace intervals.

CR3 OL1 Blink Enable

If a logical one, then this bit forces the OL1 (A-E) inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL1 (A-E) inputs. In order for overlay 1 bit plane to blink, bit CR1 must be set to a logical one.

CR2 OL0 Blink Enable

If a logical one, then this bit forces the OL0 (A-E) inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL0 (A-E) inputs. In order for overlay 0 bit plane to blink, bit CR0 must be set to a logical one.

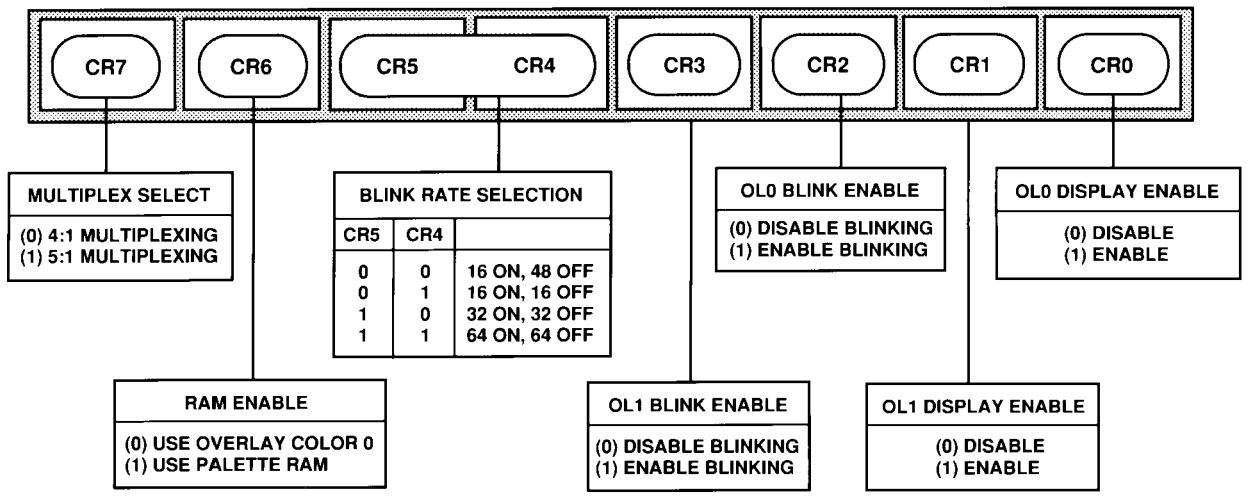


Figure 5. Command Register Definitions

CR1 OL1 Display Enable
If a logical zero, this bit forces the OL1 (A-E) inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL1 (A-E) inputs.

CR0 OL0 Display Enable
If a logical zero, this bit forces the OL0 (A-E) inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL0 (A-E) inputs.

Read Mask Register
The read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. D0 corresponds to bit plane 0 (P0 (A-E)) and Bit 7 corresponds to Bit Plane 7 (P7 (A-E)). Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized at power on.

Blink Mask Register
The blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by the command register. D0 corresponds to Bit Plane 0 (P0 (A-E)) and D7 corresponds to Bit Plane 7 (P7 (A-E)). In order for a bit plane to blink, the corresponding bit in the read mask register must be a logical one.. This register may be written to or read by the MPU at any time and is not initialized at power on.

Test Register
The test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read from by the MPU at any time and is not initialized at power up. When writing to the register, the upper four bits (D7–D4) are ignored.

The contents of the test register are as follows:

D7–D4	Color Information (4 Bits of Red, Green or Blue)
D3	Low (Logical One) or High (Logical Zero) Nibble
D2	Blue Enable
D1	Green Enable
D0	Red Enable

To use this test register, the host MPU writes to it, setting one, and one only, of the red, green or blue enable bits. These bits specify which four bits of color information the MPU wishes to read (R7–R4, G7–G4, B7–B4, R3–R0, G3–G0, or B3–B0). When the MPU reads the test register, the four bits of color information from the DAC inputs are contained in the upper four bits, and the lower four bits contain the red, green, blue and nibble information previously written. Note that either the CLOCK must be slowed down to the MPU cycle time or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper four bits of red color information being presented to the D/A converters, the MPU writes to the test register, setting only the red enable bit (D0). The nibble bit (D3) is set to a logical zero to ensure that the high nibble of the red data is accessed. The MPU then proceeds to read the test register, keeping the pixel data stable. This results in D7–D4 containing R7–R4 color bits and D3–D0 containing red, green, blue and low or high nibble enable information, illustrated as follows:

D7	D6	D5	D4	D3	D2	D1	D0
R7	R6	R5	R4	0	0	0	1

DIGITAL TO ANALOG CONVERTERS (DACs) & VIDEO OUTPUTS

The ADV458 contains three high speed video DACs. The DAC outputs are represented as the three primary analog color signals IOR (red video), IOG (green video) and IOB (blue video). Other analog signals on the part include FS_{ADJUST} and V_{REF}.

DACs & Analog Outputs
The part contains three matched 8-bit digital to analog converters. The DACs are designed using an advanced, high speed, segmented architecture. The bit currents corresponding to each digital input are routed to either IOR, IOG, IOB (bit = "1") or GND (bit = "0").

The analog video outputs are high impedance current sources. Each of the these three RGB current outputs are specified to directly drive a 37.5 Ω load (doubly terminated 75 Ω).

Reference Input and FS_{ADJUST}
An external 1.235 V voltage reference is required to drive the analog outputs of the ADV458. The reference voltage is connected to the V_{REF} input.

A resistor R_{SET} is connected between the FS_{ADJUST} input of the part and ground. For specified performance, R_{SET} has a value of 523 Ω. This corresponds to the generation of RS-343A video levels (with $\overline{SYNC}$ on IOG and Pedestal = 7.5 IRE) into a doubly terminated 75 Ω load. Figure 7 illustrates the resulting video waveform and the Video Output Truth Table shows the corresponding control input stimuli.

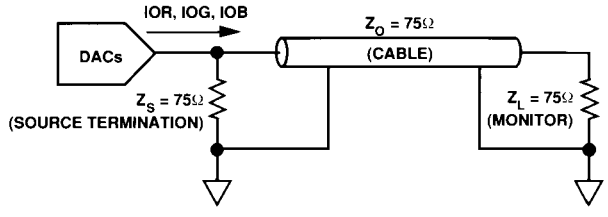


Figure 6. DAC Output Termination (Doubly Terminated 75 Ω Load)

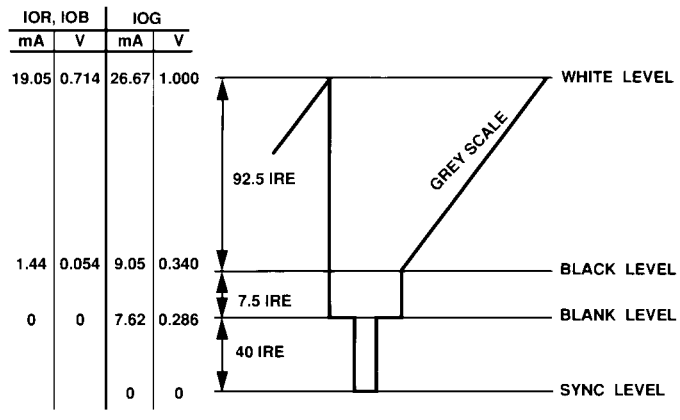


Figure 7. Composite Video Waveform SYNC Decoded on IOG; Pedestal = 7.5 IRE; R_{SET} = 523 Ω

Table IV. Video Output Truth Table

Description	IOG (mA)	IOR, IOB (mA)	$\overline{\text{SYNC}}$	DAC $\overline{\text{BLANK}}$	Input Data
WHITE LEVEL	26.67	19.05	1	1	FFH
VIDEO	video + 9.05	video + 1.44	1	1	data
VIDEO to BLANK	video + 1.44	video + 1.44	0	1	data
BLACK LEVEL	9.05	1.44	1	1	00H
BLACK to BLANK	1.44	1.44	0	1	00H
BLANK LEVEL	7.62	0	1	0	xxH
SYNC LEVEL	0	0	0	0	xxH

ADV458 INITIALIZATION

After power has been supplied, the ADV458 must be initialized. To reset the pipeline delay to a fixed delay of eight clock cycles using the CLOCK/$\overline{\text{LD}}$ sequence control, the reset sequence must be performed before the initialization. The command register must be reinitialized when the multiplex selection is changed.

Device: *ADV458*
Multiplexing: *4:1*
Overlay *No*
Blinking *No*

Control Register Initialization	C1	C0	R/$\overline{\text{W}}$	Comment
Write 04H to Address Register (ADDR)	0	0	0	Select Read Mask Reg
Write FFH to Read Mask Register (RMR)	1	0	0	Enable Color Palette RAM
Write 05H to Address Register (ADDR)	0	0	0	Select Blink Mask Reg
Write 00H to Blink Mask Register (BMR)	1	0	0	Disable Blinking
Write 06H to Address Register (ADDR)	1	0	0	Select Command Reg
Write 40H to Command Register (CR)	1	0	0	4:1 Muxing, Disable Overlays
Write 07H to Address Register (ADDR)	1	0	0	Select Test Register
Write 00H to Test Register (TSTR)	0	0	0	Disable Test Reg
Color Palette Ram Initialization				
Write 00H to Address Register (ADDR)	0	0	0	Select Address Register
Write Red Data to RAM (Location 00H)	0	1	0	Write to Color Palette RAM
Write Green Data to RAM (Location 00H)	0	1	0	Write to Color Palette RAM
Write Blue Data to RAM (Location 00H)	0	1	0	Write to Color Palette RAM
Write Red Data to RAM (Location 01H)	0	1	0	Write to Color Palette RAM
Write Green Data to RAM (Location 01H)	0	1	0	Write to Color Palette RAM
Write Blue Data to RAM (Location 01H)	0	1	0	Write to Color Palette RAM
.				
.				
Write Red Data to RAM (Location FFH)	0	1	0	Write to Color Palette RAM
Write Green Data to RAM (Location FFH)	0	1	0	Write to Color Palette RAM
Write Blue Data to RAM (Location FFH)	0	1	0	Write to Color Palette RAM
Overlay Color Palette Initialization				
Write 00H to Address Register (ADDR)	0	0	0	Select Address Register
Write Red Data to Overlay (Location 00H)	1	1	0	Write to Overlay Color 0
Write Green Data to Overlay (Location 00H)	1	1	0	Write to Overlay Color 0
Write Blue Data to Overlay (Location 00H)	1	1	0	Write to Overlay Color 0
Write Red Data to Overlay (Location 01H)	1	1	0	Write to Overlay Color 1
Write Green Data to Overlay (Location 01H)	1	1	0	Write to Overlay Color 1
Write Blue Data to Overlay (Location 01H)	1	1	0	Write to Overlay Color 1
.				
.				
Write Red Data to Overlay (Location 03H)	1	1	0	Write to Overlay Color 3
Write Green Data to Overlay (Location 03H)	1	1	0	Write to Overlay Color 3
Write Blue Data to Overlay (Location 03H)	1	1	0	Write to Overlay Color 3

Clock Interfacing
The ADV458 accepts differential clock signals CLOCK and $\overline{\text{CLOCK}}$ due to the high operating clock rates. A PLL Clock Generator Chip, such as the ICS1562, can be used to generate the CLOCK, CLOCK and $\overline{\text{LD}}$ ECL logic signals is shown in Figure 8 below. The termination resisters should be located as close as possible to the clock driver. Differential signals only must be used for the CLOCK and $\overline{\text{CLOCK}}$ inputs and should be greater than 0.6 V peak to peak.

Depending on whether 4:1 or 5:1 multiplexing is being used CLOCK is divided by 4 or 5 generating $\overline{\text{LD}}$. This signal is phase shifted relative to CLOCK. Therefore the $\overline{\text{LD}}$ signal propagation delay need not be considered. This $\overline{\text{LD}}$ signal can be used to generate the fundamental video timing of the system ($\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$) and can also be used as the shift clock for video DRAMs.

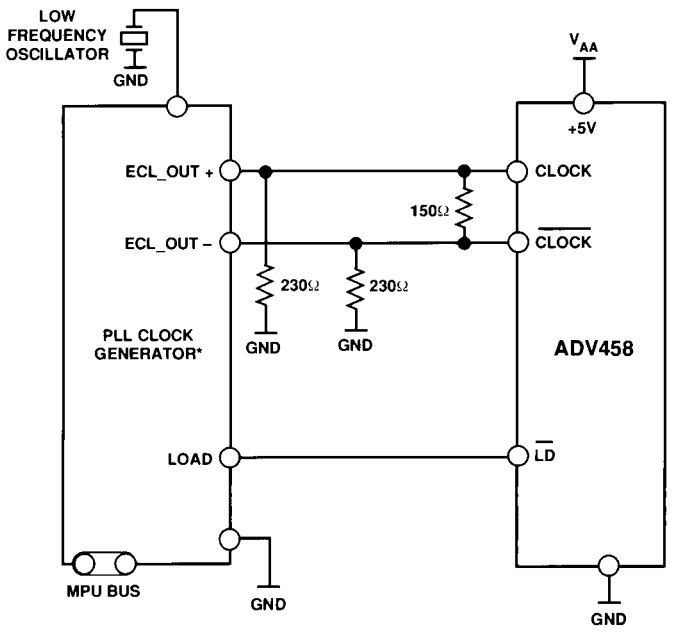


Figure 8. Generating Clock Signals Using a PLL Clock Chip

Pipeline Delay
The ADV458 pipeline delay after power up is a fixed number from six to ten cycles. However the pipeline delay on the ADV458 can be reset at a fixed eight clock cycles. In this mode the blink counter circuitry is not reset. If multiple ADV458s are to be used in parallel, the on-chip blink counters may not be synchronized. Therefore the blink mask register then should be set to 00H and the overlay blink enable bits set to logical zero. In the instance where the pipeline delay is reset to a fixed eight clock cycles, each time the input multiplexing changes, the ADV458 must be reset to a fixed pipeline delay. In standard operation the on-chip blink circuitry may be used as the device is reset following a power up or reset condition.

To reset the ADV458, the device must be powered up with CLOCK, $\overline{\text{CLOCK}}$ and $\overline{\text{LD}}$ running. Then CLOCK held high and $\overline{\text{CLOCK}}$ held low for at least 3 rising edges of $\overline{\text{LD}}$. They can be held for an unlimited time. CLOCK and $\overline{\text{CLOCK}}$ should be restarted as close as possible to the rising edge of $\overline{\text{LD}}$. The falling edge of CLOCK should lead by no more than 1 clock cycle and lag by no more than 1.5 clock cycles.

BOARD DESIGN AND LAYOUT CONSIDERATIONS

The ADV458 is a highly integrated circuit containing both precision analog and high speed digital circuitry. It has been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system level design such that high speed, accurate performance is achieved. The "Recommended Analog Circuit Layout" shows the analog interface between the device and monitor.

The layout should be optimized for lowest noise on the ADV458 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes
The ground plane should encompass all ADV458 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV458, the analog output traces, and all the digital signal traces leading up to the ADV458. The ground plane is the graphics board's common ground plane.

Power Planes
The ADV458 and any associated analog circuitry should have its own power plane, referred to as the analog power plane (V_{AA}). This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV458.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV458 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling
For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 μF ceramic capacitor decoupling. Each group of V_{AA} pins on the ADV458 must have at least one 0.1 μF decoupling capacitor to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV458 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high-frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect
The digital inputs to the ADV458 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV458 should be avoided to reduce noise pick-up.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect
The ADV458 should be located as close as possible to the output connectors to minimize noise pick-up and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

Digital inputs, especially Pixel Data Inputs, Overlay Inputs and clocking signals (CLOCK and $\overline{LD}$, etc.) should never overlay any of the analog signal circuitry and should be kept as far away as possible.

For best performance, the analog outputs (IOR, IOG, IOB) should each have a 75 Ω load resistor connected to GND. These resistors should be placed as close as possible to the ADV458 so as to minimize reflections.

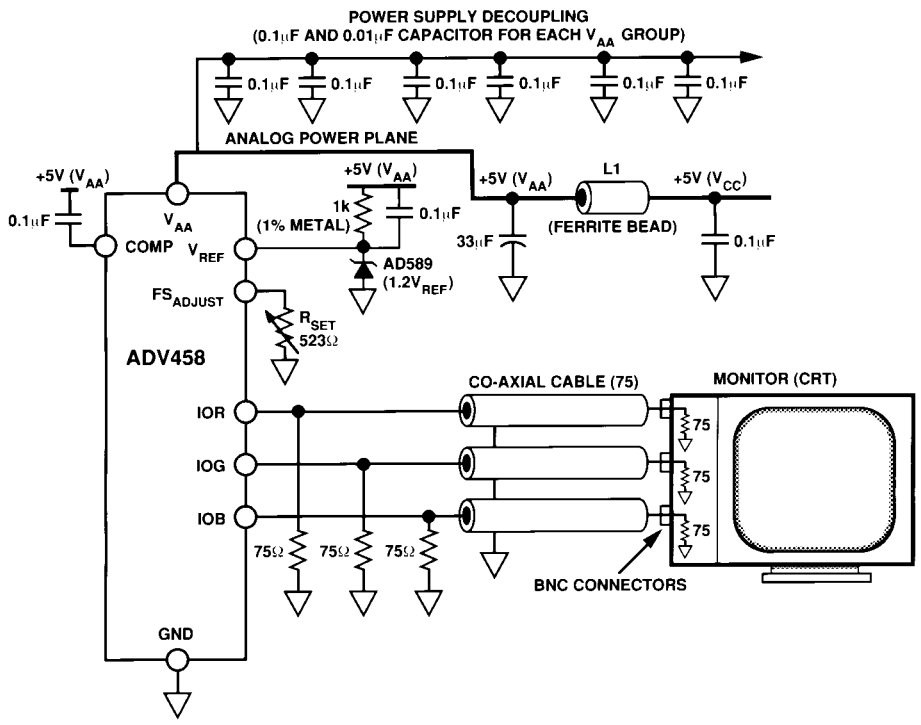
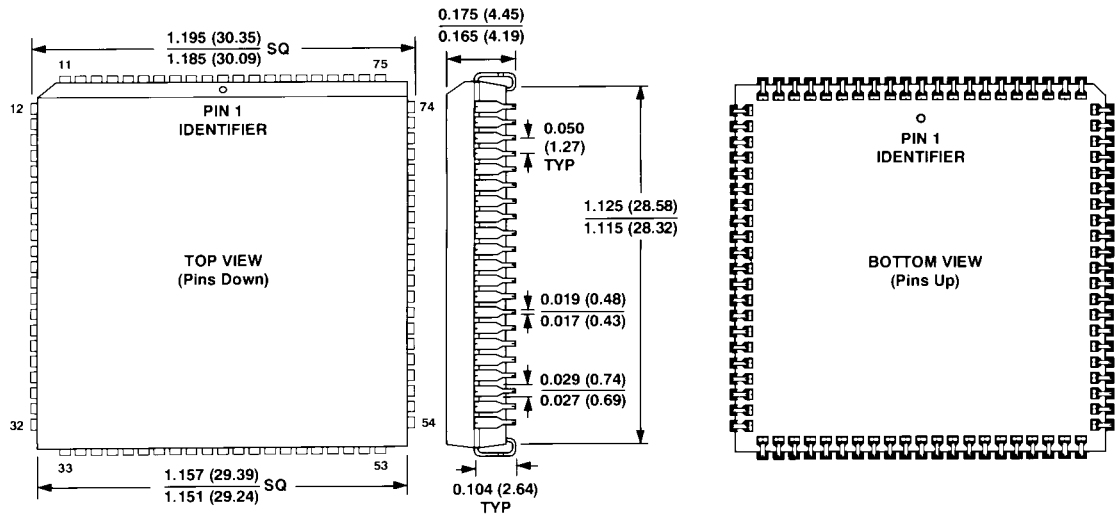


Figure 9.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

84-Pin Plastic Leaded Chip Carrier (PLCC)



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