Using the SA5752 and SA5753 for low voltage designs AN1742

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INTRODUCTION

The SA5752 and the SA5753 are two audio processor chips that can be used in designs that require 3 volt operation. This chip set, known as the APROC II (SA5752 and SA5753), is functionally similar to the APROC I (SA5750 and SA5751), but with a number of enhancements which allow more design flexibility for the designer. Additionally, the APROC II offers the same high performance as the APROC I. The SA5752 is the low voltage version of the SA5750, and the SA5753 is the low voltage version of the SA5751. Figures 1 and 2 show the block diagrams of the APROC II and APROC I, respectively. Notice that the differences are subtle and pertain primarily to the amplifier section.

If a designer is not familiar with the APROC I chip set, he/she can refer to AN1741 which discusses the basics of audio processing and the key functions used to meet the strict requirements for cellular specifications. Additionally, it describes how to design with the chip set and how to measure attack and release times for the compandor section.

This application note should be used in conjunction with AN1741 to fully understand audio processing. Experience with the APROC I will help aid the designer in learning the APROC II, but this is not a necessity. This application note will focus on the main differences between the APROCs and highlight key areas of the APROC II.

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- Comparing the SA5751 and SA5753
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I. KEY DIFFERENCES BETWEEN APROC I AND APROC II

Table 2 shows the main differences between the APROC I and II. One noticeable difference is the power consumption and power down currents. Moreover, the SA5753 has three power down modes which will be discussed in detail in the Power Down Mode section of this application note.

Comparing the SA5750 and SA5752

The SA5750 and SA5752 differ in the following ways:

Packaging

There are minimal differences between the SA5750 and the SA5752. Instead of a 24 pin package, the SA5752 is offered in a 20 pin package. This change allows the SA5752 to come in the SSOP package. The SSOP package is smaller in dimension than the standard SO package which saves space.

External Amplifiers

Since many APROC I customers use their own external speaker and ear amplifiers, the SA5752 was designed without them (see Figures 1 and 2). However, the other key blocks are present, like the preamp, VOX, compressor, expandor, and noise canceller circuit.

Since the SA5752 does not supply the ear and speaker amplifiers internally, an external one can be used. The Philips TDA7050T is the recommended choice because of its low voltage operation and high performance capabilities.

Power Consumption

The current consumption and power down mode has been improved in the SA5752. For normal operation, the SA5752 only draws an I_{CC} of 3.1mA for a 3 volt supply compared to the SA5750, where I_{CC} = 8.4mA for V_{CC} = 5V. Additionally, in the power down mode, the SA5752 only draws 0.2mA of current, compared to 1.8mA for the SA5750. Recall that the power down mode is implemented when the chip is not being used to conserve battery life. The power down feature is preferred instead of completely turning off the power to the chip because the turn on time to normal operation is faster.

Comparing the SA5751 and SA5753

The SA5751 and SA5753 differ in the following ways:

Packaging

The SA5751 is available in a 24 pin DIP package or a 28 pin SO package.

Similar to the SA5752, the SA5753 is also offered in the 20 pin SSOP package. The combination of these packages allows all the audio processing functions to be done in a minimal amount of board space.

Power Consumption

The current and voltage specification has also improved for the SA5753. This chip draws 2.1mA at 3V compared to 2.7mA at 5V for the SA5751. There is also additional current economy from the three different power-down modes, PWDN, DENA and IDLE (see Power-Down section). These power-down currents are 0.2mA, 0.6mA and 0.7mA compared to 0.9 for the SA5751.

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Programmable gain attenuators

The SA5753 has the same key block functions as the SA5751, but there are additional features. The SA5753 has nine programmable gain attenuators throughout the transmit and receive path. This allows the designer the flexibility to tailor the signal level at different ports. The SA5751 has only one programmable gain attenuator in the receive path which can be used as the volume control. Table 3 shows the programmable gain attenuators' range for the SA5753.

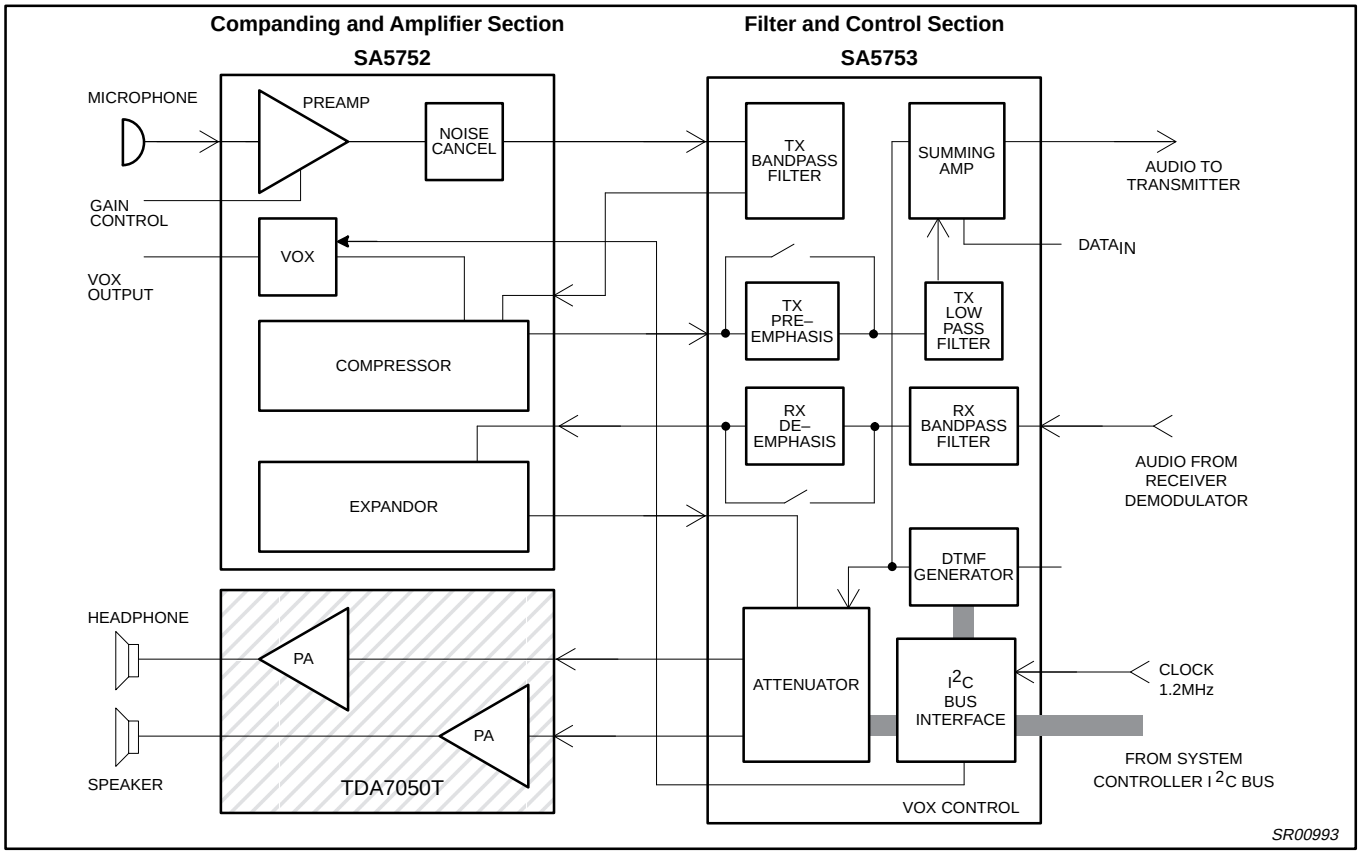


Figure 1. Block Diagram of Audio Processor (APROC II) System Chip Set

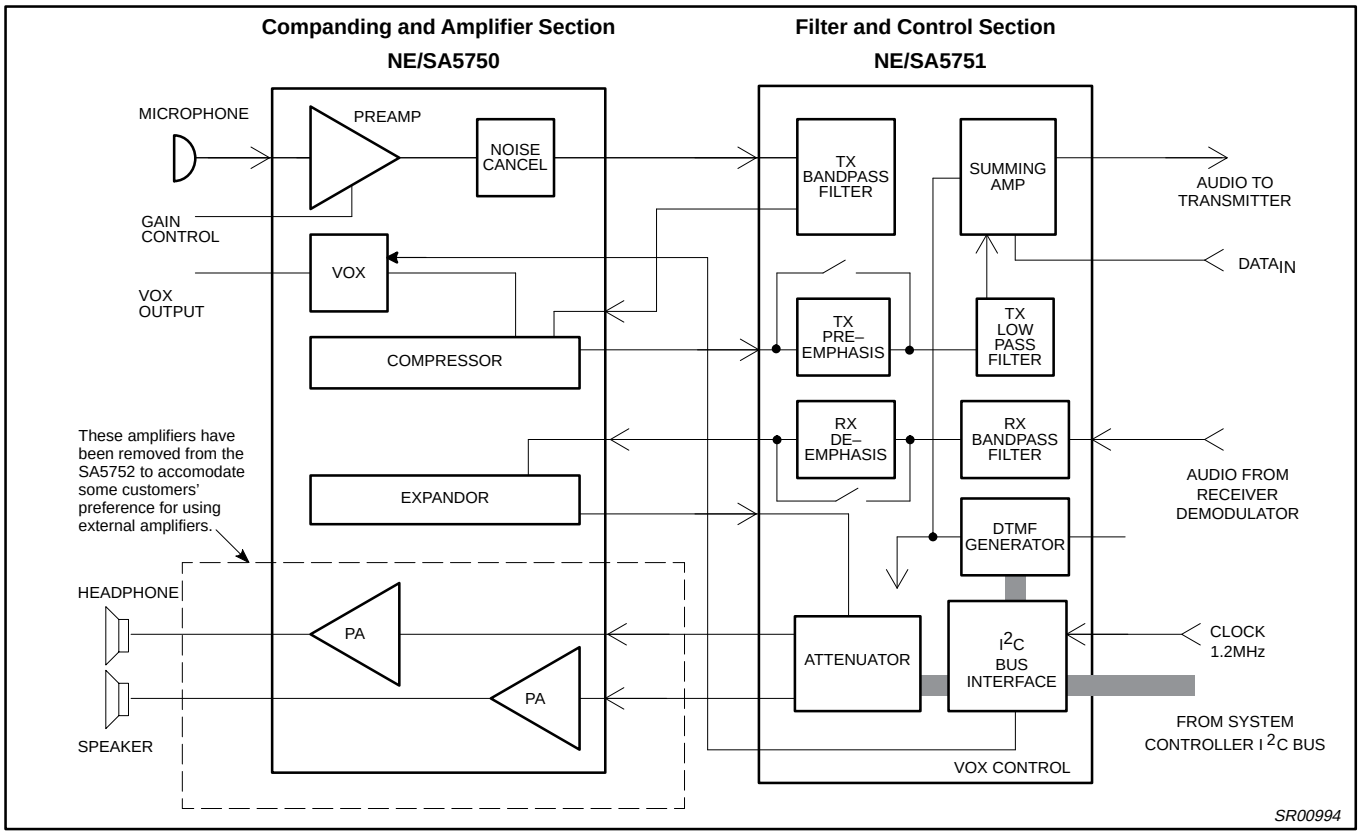


Figure 2. Block Diagram of Audio Processor (APROC I) System Chip Set

Table 2. Key Differences Between APROC I and APROC II (All values are Typical)

	APROC I		APROC II	
	SA5750	**SA5751**	**SA5752**	**SA5753**
V_{CC} (V)	4.5 – 5.5	4.5 – 5.5	2.7 – 5.5	2.7 – 5.5
I_{CC} (mA)	8.4 @ 5V	2.7 @ 5V	3.1 @ 3V	2.1 @ 3V
Total I_{CC} (mA)	11.10		5.4	
Power Down Modes	PWDN		PWDN, IDLE and DENA	
Power Down I_{CC} (mA)	1.8	0.9	0.2	PWDN 0.2 IDLE 0.6 DENA 0.7
Packages:				
NE: 0 to +70°C	NE5750N NE5750D	NE5751N NE5751D		
SA: –40 to +85°C	SA5750N SA5750D	SA5751N SA5751D	SA5752D SA5752DK	SA5753D SA5753DK
No. of Pins	24	24 or 28	20	20
Programmable Gain Attenuators	0	1	0	9
I^2C Protocol	Not required	Required	Not Required	Optional*

Package Codes:
N: Plastic Dual In-Line Package (DIP)
D: Plastic Small Outline (SO)
FE: Ceramic Dual In-Line Package
DK: Shrink Small Outline Package (SSOP)

*Operating the SA5753 without the I^2C protocol means DTMF generator and gain attenuators are no longer functional. See SA5753 section for more details.

Table 3. Attenuator Gain Blocks (SA5753)

SYMBOL	Bits	TYPICAL STEP (dB)	TYPICAL GAIN (dB)	
			MIN	MAX
A1	4	-0.8	–12.0	0
A2a	5	±0.25	–3.75	+3.75
A2b	2	–6, (–12 on first)	–24.0	0
A3	4	–1.0	–17.0	–2
A4	4	±0.5	–3.5	+3.5
A6	4	–2.0	–30	0
A7	4	0.5	–3.5	+3.5
NAMPS	1		+1.9 in A2b –7.6 in A4	
VCO	1		+6.0 in A4	
For A2a, A4 and A7:		MSB sets the sign of the gain MSB = 0 for gain MSB = 1 for attenuation		
For all Gain Blocks:		All bits set to 0 = 0dB gain All bits set to 1 = maximum gain or attenuation		

Table 4. Power-Down Modes (SA5753)

PWDN	IDLE1	IDLE0	
1	X	X	(PWDN) Complete power down except I^2C, I/Os high impedance.
0	1	0	(DENA) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} enabled.
0	1	1	(IDLE) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} disabled.
0	0	0	Normal operation.
0	0	1	$DATA_{IN}$ to TX_{OUT} disabled.
X = don't care			

The benefit of having signal amplitude control throughout the signal path is that a designer will no longer have to add an external amplifier to boost signals. Additionally, external resistors are no longer needed to attenuate the signal. The SA5753 programmable gain attenuators make a design more flexible which saves cost and board space from external components.

Power Down

The SA5753 has three different power down modes compared to only one for the SA5751. The three power down modes are PWDN, IDLE, and DENA (see Table 4). All three power down modes have different current consumptions and provide different options to the designer.

In the PWDN mode, the voice and data channels are powered down. This allows for maximum power conservation. In the IDLE mode, both the voice and data channels are also powered down, but are glitch free when going from power down to power up.

The IDLE mode trades a higher standby current against glitch-free power-up. Hence, the IDLE mode is used for power conservation, whereas PWDN mode is mainly used for absolute maximum power conservation.

For the DENA mode, the voice channels are powered down, but the data channel is still fully active. This allows the chip set to transmit on reverse control channel without powering up the whole APROC II.

In the PWDN mode, the SA5753 transmit path from the Tx bandpass filter in to the Tx filter out pin has only 6dB of attenuation. This means that, if a signal is present and a designer does not want this signal through, he/she should use the IDLE (or DENA) mode.

Programmable Transmit and Receive Mute Polarity Function

The SA5753 also has programmable transmit and receive mute polarity functions (TxP and RxP). A designer can mute the transmit or receive path with a logic '1' or '0' on the TxMute or RxMute pin depending on how the SA5753 is programmed by I^2C.

The benefit of having programmable transmit and receive mute polarity functions is that it eliminates the need for an inverter chip which saves on costs, power, and space. If the microcontroller or data processor (DPROC) can only provide a logic '1' to mute the Tx and Rx signal path, then to mute the chip-set the standard way, an inverter gate is needed because the logic '1' needs to be converted to a logic '0'. This logic '0' is then applied to the TxMute and RxMute pin. But with the SA5753, a logic '1' applied to the TxMute and RxMute pins will mute the Tx and Rx path if the SA5753 is programmed to mute for a logic '1'.

Figure 3 shows a diagram of how the inverter gate chip is eliminated. Additionally, a logic '0' applied to the TxMute or RxMute pin can mute the signal path if the SA5753 is programmed to mute when a logic '0' is applied to the TxMute and RxMute pins. Because of this feature the APROC II can now interface directly with the Philips Semiconductors UMA1000 DPROC.

Since the TxMute and RxMute pins are separate, the Tx and Rx path can also be muted separately. For example, if a user wants to mute his/her side of the conversation (such that the other party cannot hear), but still wants to hear the other party, the Tx path needs to be muted while the Rx path is left on. Therefore, a

designer can provide a mute button on the keypad to provide this function to the user.

Since there are separate pins to mute the Tx and Rx paths, a designer is also given full flexibility in programming these pins separately. He/she can define a logic '1' to have the Tx path mute while programming a logic '0' to have the Rx path mute, or vice versa (see Figure 4). However, in most designs a logic '0' is programmed to have the Tx and Rx path muted.

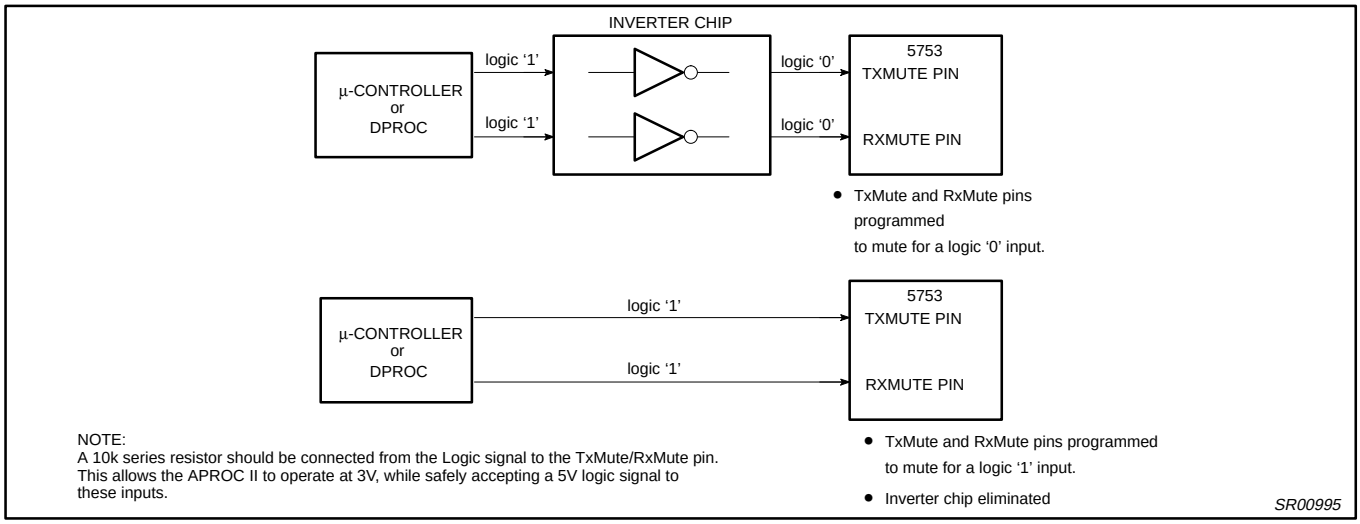


Figure 3. Benefit of Having Programmable Transmit and Receive Mute Pins

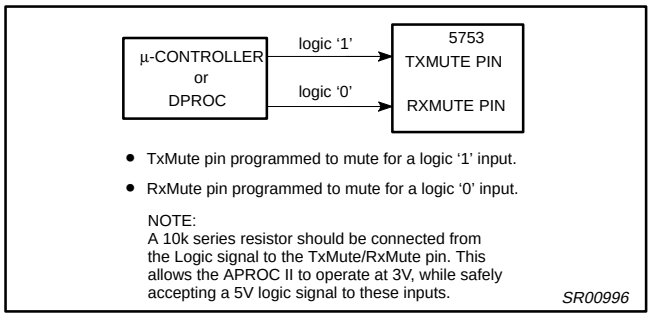


Figure 4. Muting the Tx and Rx Path for Separate Programmable Inputs

Non–I²C Operation (Default Mode)

The SA5753 can also be used without the I²C protocol by pulling the DFT (default pin) and HPDN pin HIGH. This non-I²C operation does not give the designer the flexibility to tailor the signal or use the internal DTMF generator. However, if the SA5753 is loaded serially, the SA5753 can be programmed. More information can be found in any I²C documentation. See the SA5753 section for more detailed information.

Cordless Application

Unlike the SA5751, the SA5753 can be implemented more readily for cordless phone applications. The data path can be routed through the transmit path while inhibiting the voice channel. In the receive path, the EAR_{OUT} and $SPKR_{OUT}$ can be disabled when the data is detected at the $DEMP_{OUT}$ pin.

To allow design flexibility, a designer can attenuate the data signal internally before it is passed through the TX_{OUT} pin. This eliminates the need for external components and allows programmable attenuation steps

such that different data amplitude inputs can be tailored in real-time.

VCO Mode

If the VCO bit on the SA5753 is programmed correctly, the TX_{OUT} provides an extra 6dB of gain through Attenuator 4. Therefore, the new range is 2.5dB to 9.5dB. Normally the TX_{OUT} signal is connected to a VCO (Voltage Controlled Oscillator) with a slope of 10kHz/V. The designer can implement the VCO bit to get a stronger output from the SA5753 to match 5kHz/V VCOs.

NAMPS Mode

Another key difference between the SA5753 and the SA5751 is that the SA5753 can be programmed for NAMPS mode by tailoring the gain attenuator settings.

There are two attenuators that receive the modified gain adjustments. Attenuator 4 is reduced by –7.6dB and Attenuator 2B is boosted by 1.9dB. Therefore, the new ranges are –11.1dB to –4.1dB for Attenuator 4 and –22.1dB to 1.9dB for Attenuator 2B.

The reason the gain settings are reduced is because the signal amplitude needs to be reduced before going to the transmitter. Recall that for the NAMPS mode the frequency deviation is less, so less amplitude is required.

II. SA5752

Figure 5 shows the main blocks of the SA5752: preamp, noise canceller, VOX, compressor, and expandor. This part does not require any programming blocks and therefore, no I²C is needed to operate this part. However, the SA5752 can be powered down via the SA5753 HPDN bit, which is under I²C control.

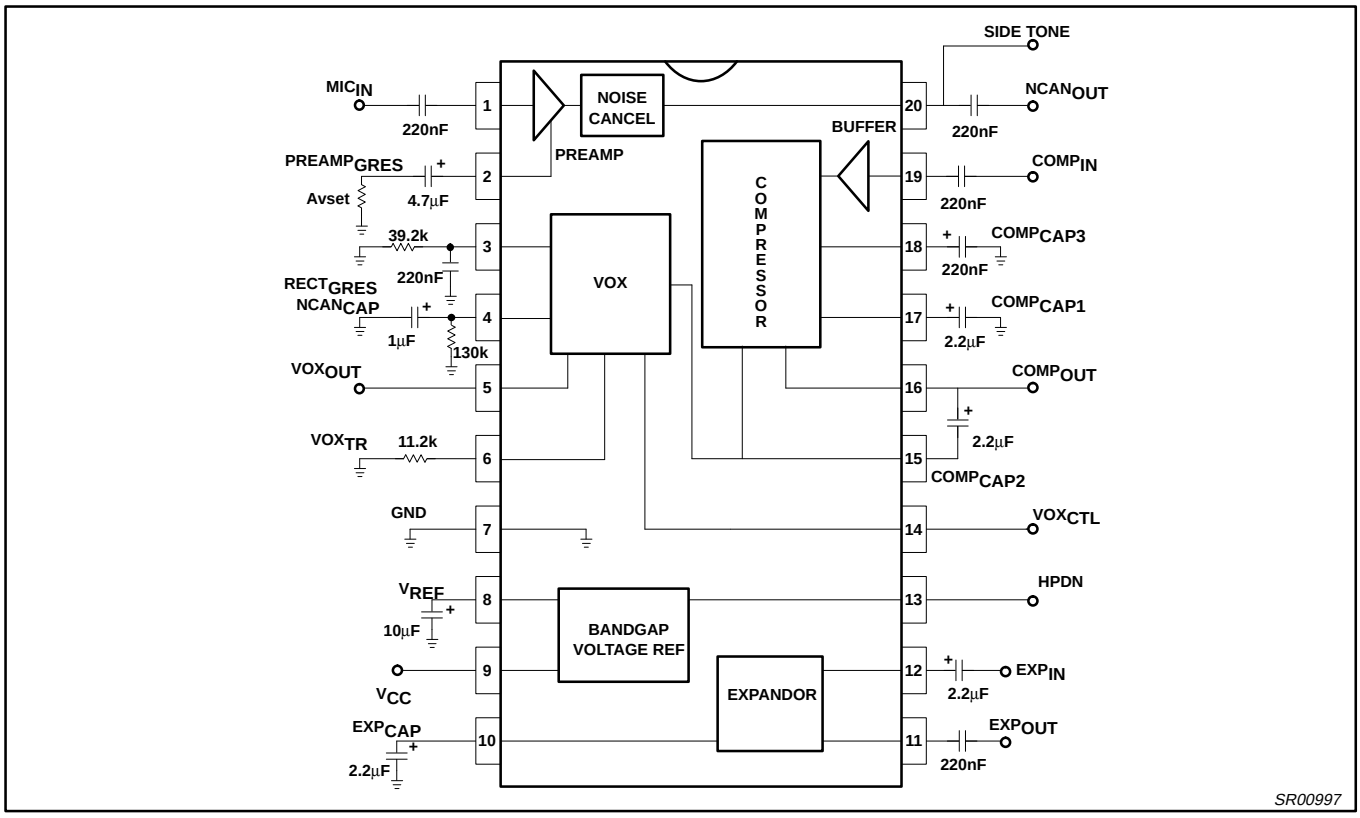


Figure 5. SA5752 Block Diagram

Preamp

The SA5752 provides a preamp which has an adjustable gain range from 0 to 40dB. The gain may be adjusted with an external resistor which connects to Pin 2 (see Equation 1, below). Table 5 shows the resistor values needed to get the appropriate gain. If a designer wants to calculate for a different value, the equation below shows how to do so.

When a designer sets the preamp gain, be sure that the output signal does not clip due to the power supply rails. To prevent this, apply the predicted strongest signal to the preamp input and observe the output while setting the gain.

Additionally, if the VOX is implemented, be sure that the extra 10dB of gain is on from the noise canceller circuit (see VOX section for more details).

$$R1 = \left[\frac{50,000}{10^{\left(\frac{X(dB)}{20}\right)} - 1}\right] - 500 \qquad (1)$$

"X" in dB

where 0 < XdB < 40dB

The preamp input impedance is 50kΩ. The output of the preamp is connected to a noise canceller which can drive a minimum load impedance of 50kΩ.

Table 5. Calculated R1 Values for Different Preamp Gains

X (dB)	R1
0	Leave Pin 2 open (∞)
5	64k
10	22k
15	10k
20	5.1k
25	2.5k
30	1.1k
35	405
40	Pin 2 AC grounded

When measuring the SA5752 preamp gain, be sure to measure the signal from Pin 20 to Pin 1. If the signal is measured from the SA5752 preamp input to the TX_{OUT} of the SA5753, the signal's amplitude will not be the expected value due to the compressor,

pre-emphasis, and attenuator settings. Therefore, remember to measure the preamp gain from the SA5752 preamp out to in.

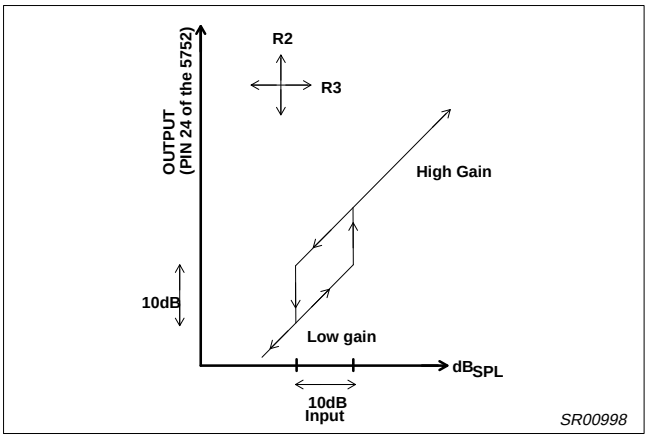


Figure 6. VOX Threshold Points

VOX

The SA5752 VOX circuitry operates like the SA5750 in that it works in conjunction with the noise canceller circuit. With the VOX activated, the noise canceller circuit will provide 10dB of gain when the input signal surpasses the ”on” threshold point. When the input signal drops below the ”off” threshold point, the noise canceller provides 0dB of gain. Figure 6 illustrates this function.

The VOX circuitry is useful for hands-free operation. This function is normally used in mobile conversation. Because there is road noise present in a moving vehicle, it is desirable to be able to prevent this noise from being heard. If the VOX threshold is set correctly, the noise canceller will provide 10dB of gain when the user speaks and a gain of 0dB when the user stops speaking. The other party will not hear the road noise in the background as loudly. Another feature of the VOX circuitry is that it can be used to save power. The transmitter can be switched off during non-speech periods if voice discontinuous mode (AMP) is enabled.

The VOX_{OUT} and VOX_{CTRL}, Pins 5 and 14 respectively, can be used to determine the status of the noise canceller. Since the VOX_{OUT} pin is an open collector output, a designer should connect a 10k pull up resistor to V_{CC}. This allows the output to read a high or low reading to determine the status of the noise canceller. Table 6 shows how Pins 5 and 14 can be used.

Having a logic ’0’ on Pin 14 (VOX_{CTRL}) is sufficient in most applications. When the voice is present, the noise canceller kicks on while the VOX_{OUT} pin supplies a logic ‘1’. When voice is not present, VOX_{OUT} pin supplies a logic ‘0’.

Supplying a logic ‘1’ on Pin 14 would cause the VOX_{OUT} pin to stay as a logic ‘1’ regardless of any signal input to the preamp

Table 6. VOX Truth Table

Inputs		Outputs	
Voice (Pin 1)	**VOX_{CTRL} (Pin 14 of NE5752)**	**Noise Canceller Gain**	**VOX_{OUT} (Pin 5 of NE5752)**
Not Present	logic ‘0’	0dB	logic ‘0’
Present	logic ‘0’	10dB	logic ‘1’
Not Present	logic ‘1’	0dB	logic ‘1’
Present	logic ‘1’	10dB	logic ‘1’

NOTE: If the NE5752 is used alone, be sure that the output of the noise canceller is AC coupled to the input of the compressor. Also, make sure that all of the components for the compressor are connected.

(Pin 1 of SA5752). However, the functionality of the noise canceller will still be signal dependent.

Pins 3, 4, 5, 6, and 14 all deal with the VOX’s performance. Resistor R2 and capacitor C3 are connected to Pin 3. These components set the gain of the VOX. The values chosen here are for internal use only and should not be altered.

The following steps are the procedure for setting the VOX threshold. Remember that this setting can be set externally by the user using an external potentiometer or by a microprocessor which can sample the sound in the car and electronically set the “automatic environment VOX function” threshold. This can be done by implementing different resistor settings for different threshold points.

Step 1: Make sure:

a. Pin 6 is left open
b. The VOX attack and recovery components are in place at Pin 4.
c. R2 and C3 are connected to Pin 3.
d. If using the SA5752 alone, be sure to connect the preamp output (Pin 20) to the compressor input (Pin 19) with a DC blocking capacitor.
e. The preamp gain is already set (in this instance the preamp gain is 0dB)
f. Make sure that the compressor’s components are also connected; compressor’s attack time has to be functional.

Step 2. Apply a constant 1kHz sinewave signal to Pin 1 through a DC blocking cap (if the Philips evaluation board is used, apply the signal to the MIC input pin) with the desired threshold. In this case, $30mV_{P-P}$.

Step 3. Measure the DC voltage on Pin 4: V4=275mV

Step 4. Calculate R5:

$$R5 = \frac{V4(V)}{25\mu A} = \frac{275mV}{25\mu A} = 11k \quad (2)$$

Step 5. Connect R5 to Pin 6 and verify that VOX kicks on at the desired threshold. This set-up has the VOX kicking on at $30mV_{P-P}$ and kicking off at $11mV_{P-P}$ (for better accuracy use a 1% resistor value for R5).

Referring to the above example, if a preamp gain of 10dB was chosen before setting the threshold, the threshold will also change. So it is vital that the preamp gain be set before setting the VOX threshold.

Noise Canceller

The output of the preamp is connected to the input of the noise canceller circuit which is internal to the device. The function of the

noise canceller is to automatically provide a set gain of either 0dB or 10dB when a voice is present or not present. The gain setting can be set by implementing the VOX functions.

Although the noise canceller circuit is really designed to be used with the VOX circuitry, it can be implemented without it. The noise canceller circuit can be set up to provide either 0dB or 10dB of gain at all times, regardless of the presence of a signal. Table 7 shows how to achieve either gain settings when the VOX function is bypassed.

Table 7. Setting Up the Gain of the Noise Canceller

Pin No.	Gain of Noise Canceller	
	0dB	10dB
3	Ground	Ground
4	Ground	V_{CC}
6	10k to GND	Ground

The output of the noise canceller is accessible to the designer at Pin 20.

Compressor
The SA5752 compandor operates with a unity gain level (0dB level) of 77.5mV$_{RMS}$. It operates like the rest of the Philips Compandor family where any signal above the 0dB level in the compressor mode is half in dB, and any signal below the 0dB level is multiplied by 2 (assuming the unit is in dB)

As for the Expandor, the levels above and below the 0dB level are modified by the opposite of what the compressor does. This allows the signal to be restored to its original level with reduction of noise.

To determine the amplitude, the following formula is used.

$$XdB = 20\log\left(\frac{\text{AC level mV}_{RMS}}{77.5\text{mV}_{RMS}}\right) \quad (3)$$

Example:
Determine the compressor's AC voltage output if a 200mV$_{RMS}$ signal is applied to the compressor's input.

1. Convert 200mV$_{RMS}$ to dB as in Equation 3

$$XdB = 20\log\left(\frac{200\text{mV}_{RMS}}{77.5\text{mV}_{RMS}}\right) = 8.23\text{dB}$$

2. Because 8.23dB is above the 0dB level, by definition of the compressor the signal is halved to 4.12dB
3. Now converting back to voltage using Equation 3 the output is 124.5mV$_{RMS}$.

Figure 7 shows the diagram with other numbers for practice.

Power Down
The HPDN (Hardware Power Down) pin on the SA5752 can be left open or connected to V_{CC} for normal operation. For power down, a designer needs to ground this pin.

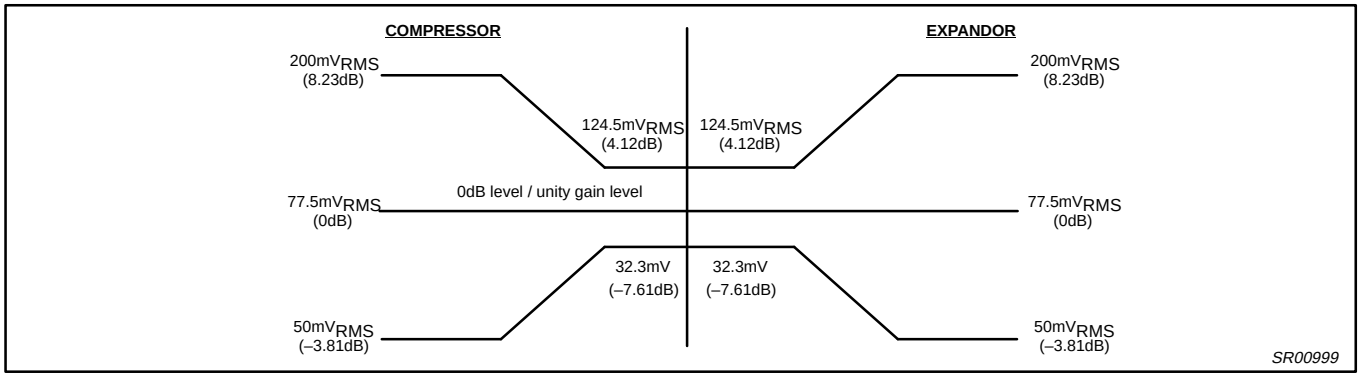


Figure 7. Determining the AC Signal Level Through a Compandor

Table 8. Programmable Divide Ratio Number

Decimal Value	Binary Value	Hi DTMF Frequency	Lo DTMF Frequency
2	0000 0010	OFF	OFF
3	0000 0011	66.66kHz	28.57kHz
4	0000 0100	50kHz	21.43kHz
5	0000 0101	40kHz	17.14kHz
• • •	• • •	• • •	• • •
254	1111 1110	787.40Hz	337.46Hz
555	1111 1111	784.31Hz	336.13Hz
256	0000 0000	781.25Hz	334.82Hz
257	0000 0001	778.21Hz	333.52Hz

III. SA5753

Figure 8 shows the main blocks of the SA5753; the Transmit and Receive Bandpass filters, the Transmit Low Pass Filter, Pre-emphasis and De-emphasis, DTMF generator, attenuators and I^{2}C controls.

Non-I^{2}C Operation (Default Mode)
The SA5753 can be used without the I^{2}C protocol. To implement this feature, the DFT pin (default, Pin 13) and HPDN (Pin 6) must be connected to V_{CC}. In the default mode, a designer has less flexibility in programming the SA5753. The only way to program the SA5753 without the I2C protocol is to load the register serially (see next section).

If a designer decides not to program the SA5753 registers, they can no longer bypass key functions or attenuate/gain the signal. Additionally, they can no longer make use of the DTMF generator.

The TxMute and RxMute pins are also no longer programmable, but are controllable externally.

A designer does not have a choice of programming the mute polarity pins. Muting the transmit and receive path now requires a

designer to supply V_{CC} to the TxMute pin (Pin 18) and RxMute pin (Pin 12). To unmute the paths, a ground connection on these pins is required.

Pin 6 must be grounded for powering down the SA5753 in the default mode. For normal operations without the I^2C protocol, Pin 6 must be connected to V_{CC}. Although the SA5753 might be functional with Pin 6 left open, this is not advisable. This pin should either have V_{CC} or ground connected for a defined state. See the SA5753 data sheet for more information on non-I^2C operation.

The following is a list of features when the Default Mode is implemented:

1. All previous settings in the registers are ignored except for R8B7 (VOX_{CTL}).
2. VOX_{CTL} = the setting in R8B7 before DFT goes high.
3. All attenuators are set to 0dB.
4. HPDN is now an input, LOW=PWDN Mode.
5. DTMF = OFF
6. DEEMPH = ON
7. PREEMPH = ON
8. AMPS mode
9. Closed = S9, S10, S13
10. Open = S1, S2, S3, S4, S5, S6, S7, S8, S11, S12
11. RX is muted when RXMUTE = HI
12. TX is muted when TXMUTE = HI

NOTE: When the SA5753 is changed from DFT=HIGH (Default Mode) to DFT=LOW, the register settings will have an indeterminate value and all registers will need to be reloaded to avoid undefined states.

Programming Without the I^2C Protocol

In the default mode, with DFT (Pin 13) and HPDN (Pin 6) pulled HIGH, the registers in the control register bit map are chained together so that bit 0 of a register is connected to bit 7 of the preceding register with R0B6, R0B7, R1B6 and R1B7 bypassed, i.e., R0B5 is connected to R1B0, R1B5 is connected to R2B0, R2B7 is connected to R3B0, etc. Bits can then be loaded as a serial stream through the SDA pin of the I^2C bus by the negative edge of a shifting clock applied at the SCL pin of the I^2C bus. When a bit is loaded at SDA it will load first into R0B0 and then will be shifted to R8B7 after 68 clock edges.

A total of 68 clock pulses (applied at SCL) are, therefore, required to completely load the registers.

In this mode of operation the contents of the register map are also shifted out from the VOX_{CTL} pin since it takes the same value as R8B7. After power up there is no reset within the registers so the first 68 bits clock out at the VOX_{CTL} pin will have an indeterminate value. Once the registers are loaded, the DFT pin can be pulled low to enable the interface between the control registers and the program functions.

Summary: To use this capability, the DFT pin and the HPDN pin must be pulled HIGH, the serial bit stream loaded through SCL synchronous with the negative clock edge applied at SCL for 68 clock pulses, and then the DFT pin pulled LOW.

DTMF

The DTMF generator generates its tones by using the 1.2MHz I^2C clock and dividing it down to the desired frequency. There are high and low DTMF tones, so different divide ratios are used. To tailor the exact frequency, a programmable divide ratio number is provided to the designer. Figure 9 shows the basic scheme and the formulas to calculate the desired DTMF frequency.

The programmable divide ratio number ranges from 3 to 257 for both the high and low DTMF functions. This means that the high DTMF frequency range is from 778.21Hz to 66.66kHz. The low DTMF frequency range is from 333.52Hz to 28.57kHz.

The only caution in using the DTMF generator is when the programmable divide ratio decimal number is 256 or 257. For the SA5753, decimal values 256 and 257 are defined as a binary ‘0’ and ‘1’, respectively (see Table 8). The reason the decimal values 256 and 257 were defined this way is because of the actual length of their binary numbers.

Decimal 256 is binary 1 0000 0000 and decimal 257 is binary 1 0000 0001. These binary numbers exceed the 8-bit register, so 256 and 257 were replaced with a decimal ‘0’ and ‘1’ since these values were not previously used.

Other decimal divide ratio numbers can be converted directly to a binary number which is then loaded into the 8-bit register. To turn off the high or low DTMF generator, a decimal 2, converted to a binary 0000 0010, needs to be loaded into the register.

Below are two examples of loading the DTMF generator.

Step 1: Determine what frequency is desired for the High and Low frequencies.

Step 2: Use formulas in Figure 9 to calculate the programmable ‘divide ratio number’ for both High and Low tones.

Step 3: Convert the calculated ‘divide ratio number’ to a binary number and load into the proper register. NOTE: If the ‘divide ratio number’ is 256 or 257, load a binary 0000 0000 or 0000 0001, respectively. To turn off the high or low

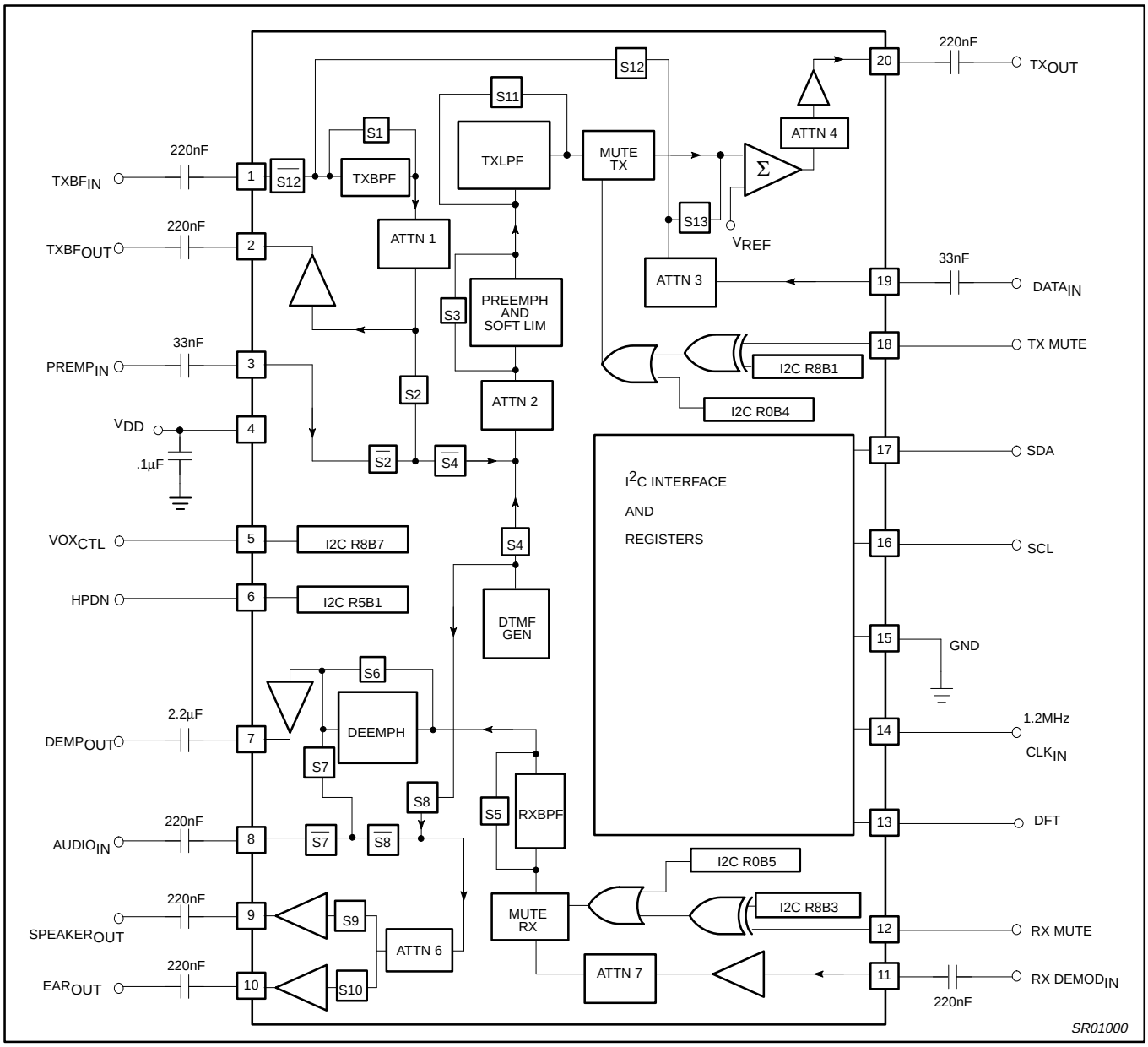


Figure 8. NE/SA5753 Test and Application Circuit

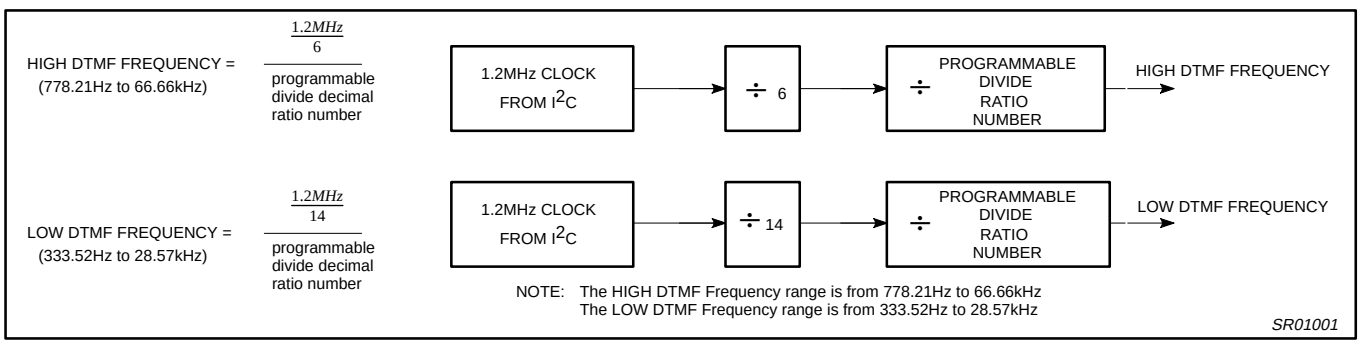


Figure 9. DTMF Formula

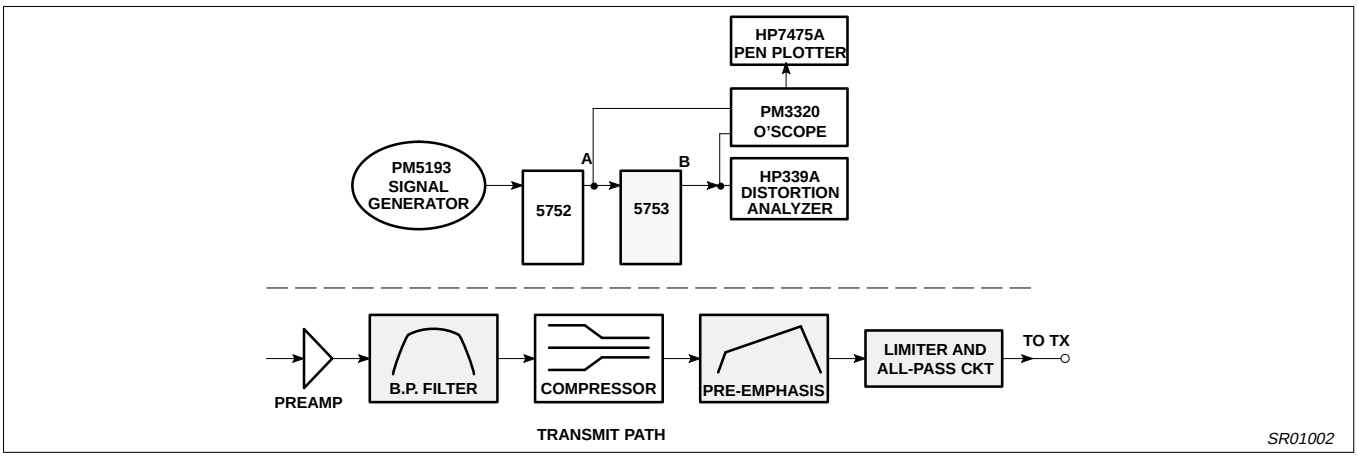


Figure 10. . Test Set-up and Tx Path of Signal

tone DTMF generator, load a binary 2 or 0000 0010 to the register.

Example 1

Program the SA5753 DTMF generator such that High DTMF = 4000Hz and Low DTMF = 3061.22Hz.

1. Using the formula in Figure 9,
   High DTMF 'divide ratio number' = 50
   Low DTMF 'divide ratio number' = 28
2. Convert 'divide ratio number' into a binary number
   High DTMF binary 'divide ratio number' = 0011 0010
   Low DTMF binary 'divide ratio number' = 0001 1100.
3. Load binary numbers into proper registers and observe on a spectrum analyzer.

Example 2

Program the SA5753 DTMF generator such that High DTMF = 778.21Hz and Low DTMF = OFF.

1. Calculate 'divide ratio number' using the formula in Figure 9,
   High DTMF 'divide ratio number' = 257
   Low DTMF 'divide ratio number' = 2, by definition for OFF see Table 8.
2. Converting 'divide ratio numbers'
   High DTMF binary 'divide ratio number' = 0000 0001 (remember the special case that applies here)
   Low DTMF binary 'divide ratio number' = 0000 0010.
3. Load binary numbers into proper registers and observe on a spectrum analyzer.

Programmable Transmit and Receive Mute Polarity Function

If a designer wants to operate the SA5753 at 3V and wants to mute the TxMute and RxMute pins with a 5V logic '1' signal, a series 10k resistor should be used. If the 10k resistor is not used, the SA5753 will draw more current. To eliminate the 10k resistor the designer should make sure that the logic '1' signal never exceeds V_{CC}.

The Limiter and All-Pass Circuit

An important aspect of the AMPS specification is concerned with the 12kHz maximum frequency deviation. The output of the APROC TX_{OUT} should be limited at a level which causes a maximum frequency deviation of 12kHz for the transmitter, regardless of the amplitude of the input signal. Figure 10 shows the equipment used for the test measurements and how the signal was processed. A 1kHz signal was applied to the input of the demo-board until a 5% distorted signal was measured at the limiter output. This waveform's peak-to-peak voltage was recorded as a reference. Then, at various chosen frequencies, the input of the demo-board was overdriven so we could record the distorted peak-to-peak waveform. (See Figure 11)

Formula 4 was used to calculate maximum frequency deviation from the waveforms shown in Figure 11.

$$\text{Max Freq Dev with All-Pass Ckt} = \left(\frac{BW_F}{BW_R}\right) 8\text{kHz} \quad (4)$$

where

BW_F = the bottom waveform's peak-to-peak voltage from one of the observed figures.

BW_R = the bottom waveform's peak-to-peak voltage from the reference Figure 11.

Table 9. Maximum Frequency Deviation Results for the 12kHz Test

Frequency (Hz)	With All-Pass (kHz)
300	3.58
500	5.61
800	10.13
1000	10.01
1200	9.21
2000	10.01
3000	9.61

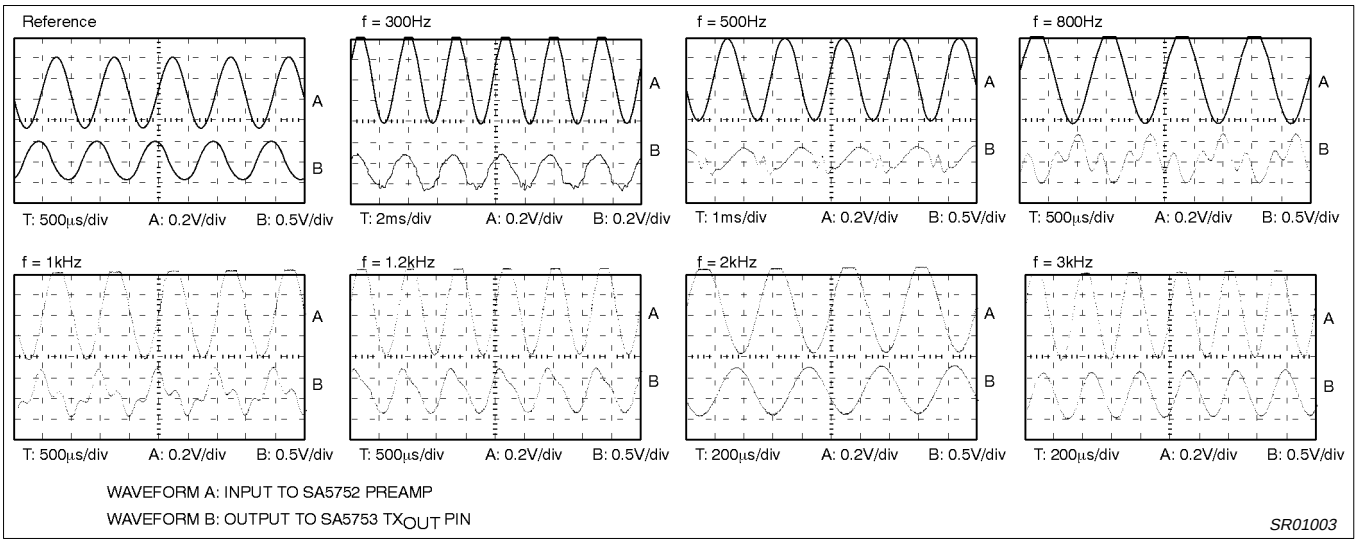


Figure 11. Results from the AMPS 12kHz Maximum Frequency Deviation Test

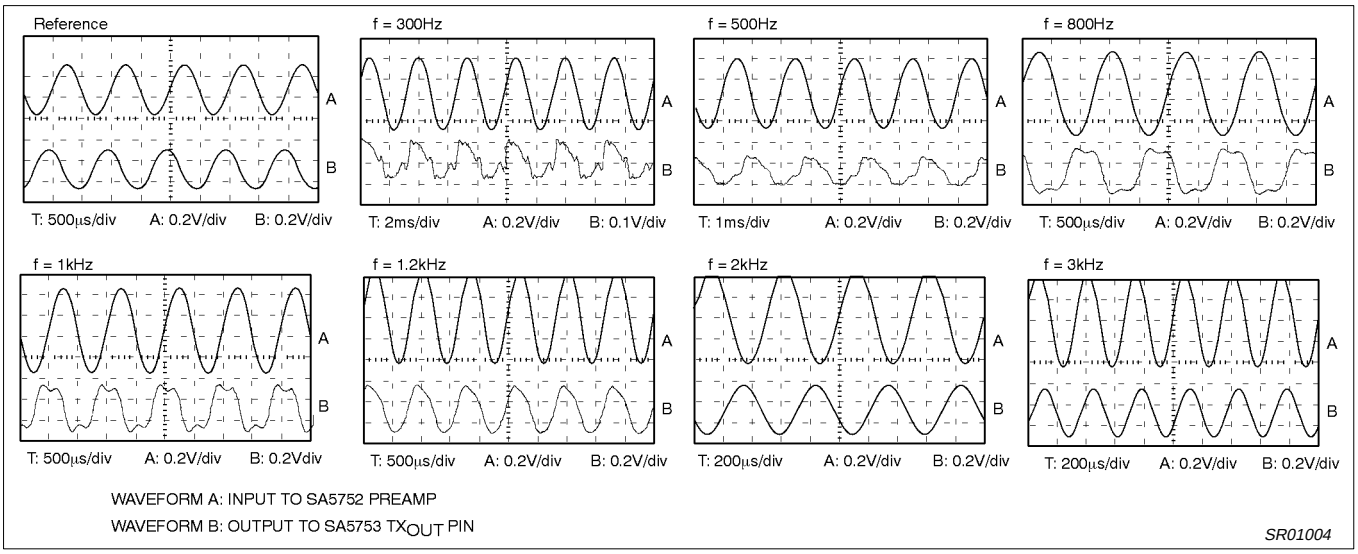


Figure 12. Results from the NAMPS 5kHz Maximum Frequency Deviation Test

Table 9 reveals the calculated results for maximum frequency deviation over the voice band. The test results show that the NE5752 and NE5753 will meet the 12kHz AMPS specification.

The same test set-up was used for the NAMPS measurements, however, the maximum frequency deviation formula changes. The following formula shows how to calculate the maximum frequency deviation for NAMPS:

$$\text{Max Freq Dev with All-Pass Ckt} = \left(\frac{BW_F}{BW_R}\right) 2.9\text{kHz} \quad (5)$$

where

BW_F = the bottom waveform's peak-to-peak voltage from one of the observed figures.

BW_R = the bottom waveform's peak-to-peak voltage from the reference Figure 12.

Table 10. Maximum Frequency Deviation Results for the 5kHz Test

Frequency (Hz)	With All-Pass (kHz)
300	1.48
500	2.11
800	3.27
1000	3.46
1200	3.42
2000	3.65
3000	3.56

Formula 5 was used to calculate the maximum frequency deviation in Table 10 from the waveforms shown in Figure 12. These test results show that the APROC II will meet the 5kHz maximum frequency deviation for NAMPS.

IV. EVALUATION SOFTWARE AND DEMOBOARD

The APROC II demoboard and evaluation software are for evaluation purposes only. It can help a designer understand the hardware and software functionality. The APROC II schematic and layout can be seen in Figures 13 and 14, respectively. The function of each external component is briefly shown in Figure 13.

In this software package, the screen (see Figure 15) only shows the signal path for the SA5753. Recall that for the audio processing chip, the signal is routed between the SA5752 and SA5753. The appropriate pin numbers are labeled to show where the signal enters and leaves the SA5753.

The upper half of the screen is the Tx path and the lower half of the window is the Rx path. To complete the signal path, a designer can use the computer's arrow keys to get to the area of interest. The space bar is used to toggle on and off path switches and key functions (like NAMPS, VCO, HPDN, VOX_{CTRL} etc).

The 'greater than' (>) or 'less than' (<) symbol keys on the key board are used to vary the value of the gain attenuator blocks. The way the gain attenuator blocks are programmed does not follow the logical way where the 'greater than' symbol key means going up in gain and the 'less than' symbol means decreases gain. Instead, the set up is programmed logically by the bits. So a user should use the 'greater than' and 'less than' symbol keys to vary the value, but continue to use the keys until the values stop changing. (See Table 11.)

To power down the chip set the following steps should be taken:

1. To power down the SA5752, move the marker to HPDN and hit the space bar to implement this function.

2. To implement one of the SA5753 three power down modes move the marker to the Power = 000 Bin and program the appropriate mode.

- For PWDN, set Power=1xx Bin; X=don't care
- For IDLE, set Power = 011 Bin
- For the DENA mode, set Power= 010 Bin
- For normal operation, set Power= 000 Bin
- For $DATA_{IN}$ to TX_{OUT} disabled, set Power= 001 Bin. This can be used for cordless applications

To power up the chip set, a designer needs to set the Power=000 Bin (for the SA5753) and toggle the HPDN section (for the SA5752).

DTMF

To implement the DTMF tones, a user can program the high and low tones by typing in the frequencies or programming the I^2C bits.

The high decimal value is from 2 to 257 where the frequency range is from off to 778.21Hz–66.66kHz. The low decimal value is from 2 to 257 where the frequency range is from off to 333.52Hz up to 28.57kHz.

The difference between the SA5753 DTMF generator and the SA5751 is that when the cycle is completed, the DC voltage goes back to 0V, whereas the SA5751 might not return to 0V. Therefore, upon switching back to the Tx voice path, a glitch may be heard from the SA5751, but not from the SA5753.

V. QUESTIONS AND ANSWERS SECTION

Q: I connected your evaluation board and software program but I do not see any output signal on the Transmit path. My input signal is connected to the Mic input of the SA5752. What is the problem?

A: There are several issues to look at. Make sure that the TxMute and RxMute pins are defined. If the registers are programmed such that the TxMute and/or RxMute pins need to be grounded for a signal to flow, please be sure that those pins are grounded.

If the registers are defined such that the TxMute and RxMute pins need V_{CC} connected to them for a completed signal path, please connect V_{CC} to the pins. Although leaving these pins open may work, it defines an open state and is, therefore, not guaranteed.

Q: When I program a DTMF tone, it only stays on for 96ms. How can I make it stay on longer?

A: The DTMF generator is designed to stay on for only 96ms. If a longer tone is desired, the DTMF registers must be re-loaded before the 96ms expires or set DTC = 1. For the evaluation program, the DTMF register can be loaded up automatically to observe the DTMF tone. Just toggle the space bar on the "DTMF frequency DTC" section.

Q: On the evaluation program, there are ADD field and REG values. What are these?

A: These are the registers (ADD = Address field and REG = the register) that must be programmed when using the SA5753 in the I^2C mode. The address field defines which portion of the chip is being accessed (See SA5753 data sheet for a detail look). The register bits control the functions of the block.

If a designer toggles in/out functions, they can see the registers which control that function. The Evaluation software is meant as a learning tool to aid the designer in getting up to speed.

Q: The SA5753 seems to be consuming more current than usual. Is this part damaged?

A: One area to look at is the I^2C clock. If the I^2C clock goes below ground, the SA5753 will draw more current. Therefore, be sure

that the I^2C clock is set at 1.2MHz square wave and it is from ground to V_{CC}.

Q: I have a Philips APROC II demoboard and a 5V I^2C interface board. At the present moment, I use two supplies to run the APROC II board at 3V and the interface board at 5V. Is there a 3V chip available that can be used for the interfacing between the computer's printer port to the I^2C section of the chip?

A: Yes, there is a 3V interface chip; the Philips PC74HC4049T. When a customer purchases an APROC II demoboard, he/she should receive an interface board. Most likely it will be the 3V version.

Q: The APROC II seems to draw more current than usual when I mute the TxMute and RxMute pins with a 5V logic '1' signal. The APROC II is operating at 3V. Is this normal, and if not, what can I do?

A: If you are going to operate the APROC II at 3V and apply 5V to the RxMute and TxMute pins, a series 10k resistor should be used to allow for this configuration.

If the logic '1' input is 3V and the APROC II is operating at 3V, the 10k resistor is not required. In general, it is safe to say that the logic '1' input should be no higher than V_{CC} if the 10k resistor is not used.

Q: I am evaluating your DTMF generator using the Philips evaluation program and demoboard. The frequency calculated and the frequency measured is correct but The evaluation screen, however, sometimes shows a different number, but the number shown is not too far off. Is there a bug in the program?

A: Yes, the program display is not correct. What you calculate and measure is fine. The program is incorrect at this time.

Q: I am evaluating the current consumption of the APROC II demoboard. I read a higher current than what is spec'd in the data sheet. What am I doing wrong?

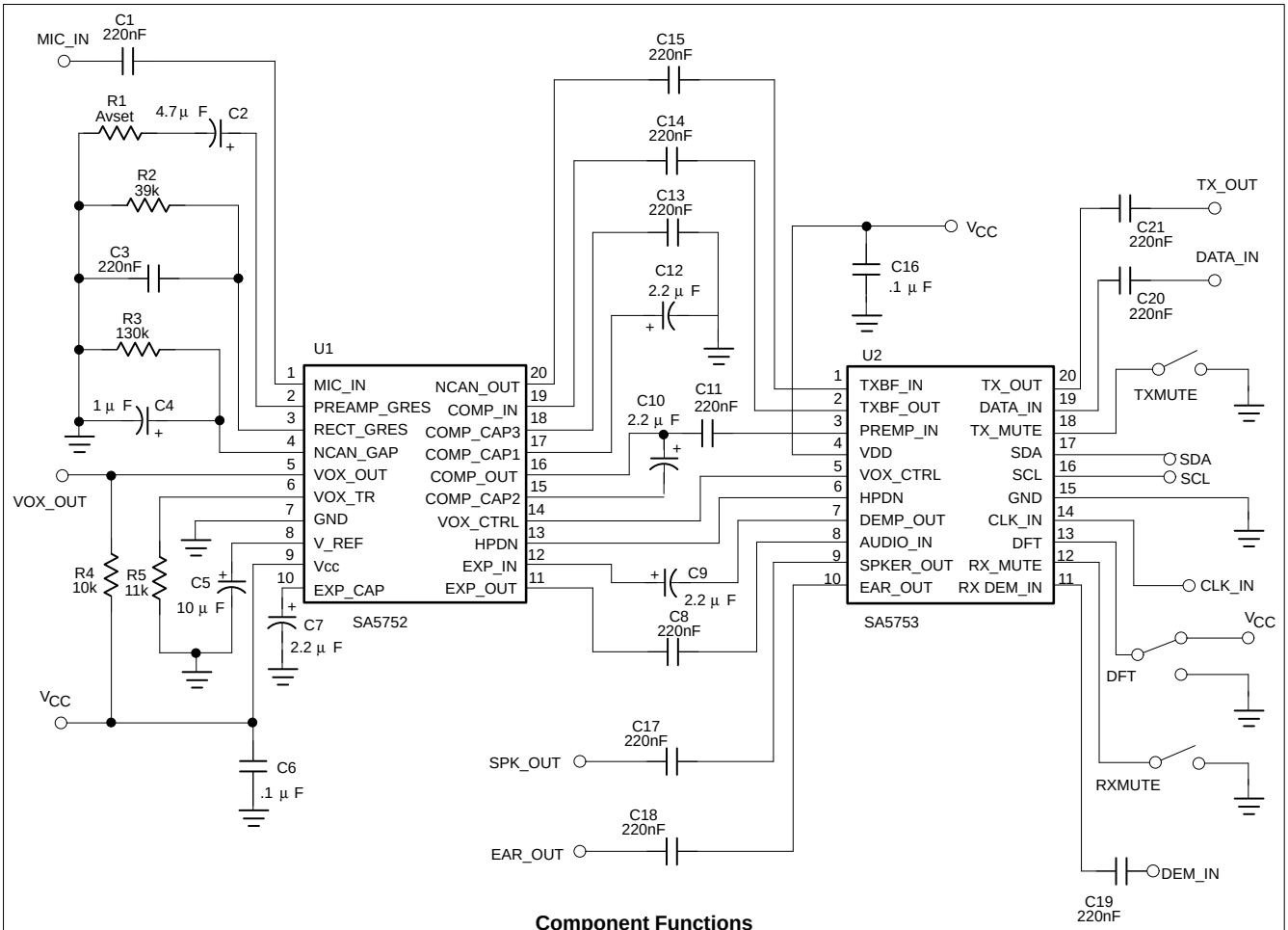
A: Remember that the I^2C interface card will draw some current away from the APROC II board (if it's connected that way). To avoid this problem, operate the I^2C interface card with a separate power supply and then measure the APROC II current.

Q: I have your APROC II evaluation demoboard. I am applying an input signal of 1kHz at $100mV_{RMS}$ to the MIC input and I am not getting any signal output on the TX_{OUT} pin. Any suggestions?

A: Your transmit path is probably open. To close the path you can do one of two things: either ground the TxP Mute pin (Pin 18) or redefine TxP to mute for a different input. You should also make sure that the SA5752 and SA5753 are in the power up state.

Q: I have a very unique situation using the SA5753. I would like to use the Default mode and I^2C mode in different situations. I know that the HPDN pin becomes an output when I^2C mode is implemented; and I know that the HPDN pin becomes an input when the Default mode is implemented. In my application I do not care about current consumption, therefore, the HPDN pin is not important to me. What can I do so that I don't leave the HPDN undefined, but at the same time, I allow myself to switch back and forth between the two modes?

A: For ease of use in the Default Mode without worrying about the function of the HPDN pin, the user can add an external pull-up resistor of 100kΩ between HPDN (Pin 6) and V_{DD}. This will put the SA5753 in Normal (active) Default operation when DFT (Pin 13) is pulled HIGH. For Power Down Mode the user will need to pull the HPDN pin LOW.



Component Functions

C1	DC blocking capacitor for MIC IN pin
C2	DC blocking capacitor for Preamp gain
C3	Used for filtering, internal use only
C4	Used to set attack and release time of VOX
C5	V_{REF} filter capacitor
C6	V_{CC} bypass capacitor
C7	Sets attack and release time of expandor
C8	DC blocking cap for Expandor out
C9	DC blocking cap for De-emphasis out
C10	AC bypassing for compressor
C11	DC blocking cap for Pre-emphasis in
C12	Sets attack and release time for compressor
C13	Passes AC to GND
C14	DC blocking cap for compressor in
C15	DC blocking cap for TXBF in
C16	V_{CC} bypass cap
C17	DC blocking cap for SPKR OUT
C18	DC blocking cap for EAR OUT
C19	DC blocking for Demodulation in pin
C20	DC blocking for Data in pin
C21	DC blocking cap for Tx OUT
R1	Sets microphone preamp gain
R2	Sets gain of VOX, but for internal use only. Effects voltage on Pin 4.
R3	Used to set the release time of VOX
R4	Pull-up resistor to get logic level out
R5	Sets threshold level of VOX

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Figure 13. APROC II Evaluation Board Schematic

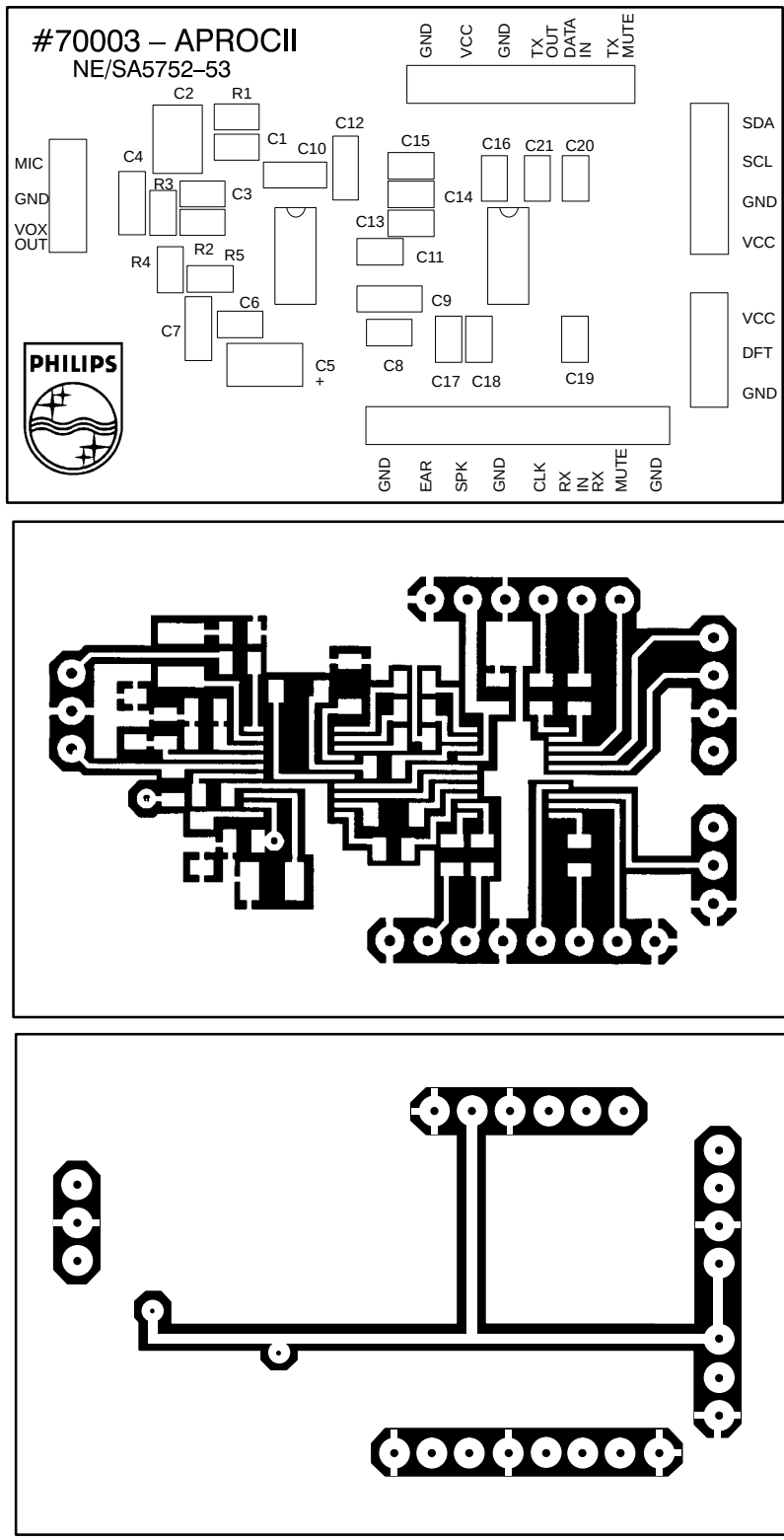

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Figure 14. APROC II Evaluation Board Layouts

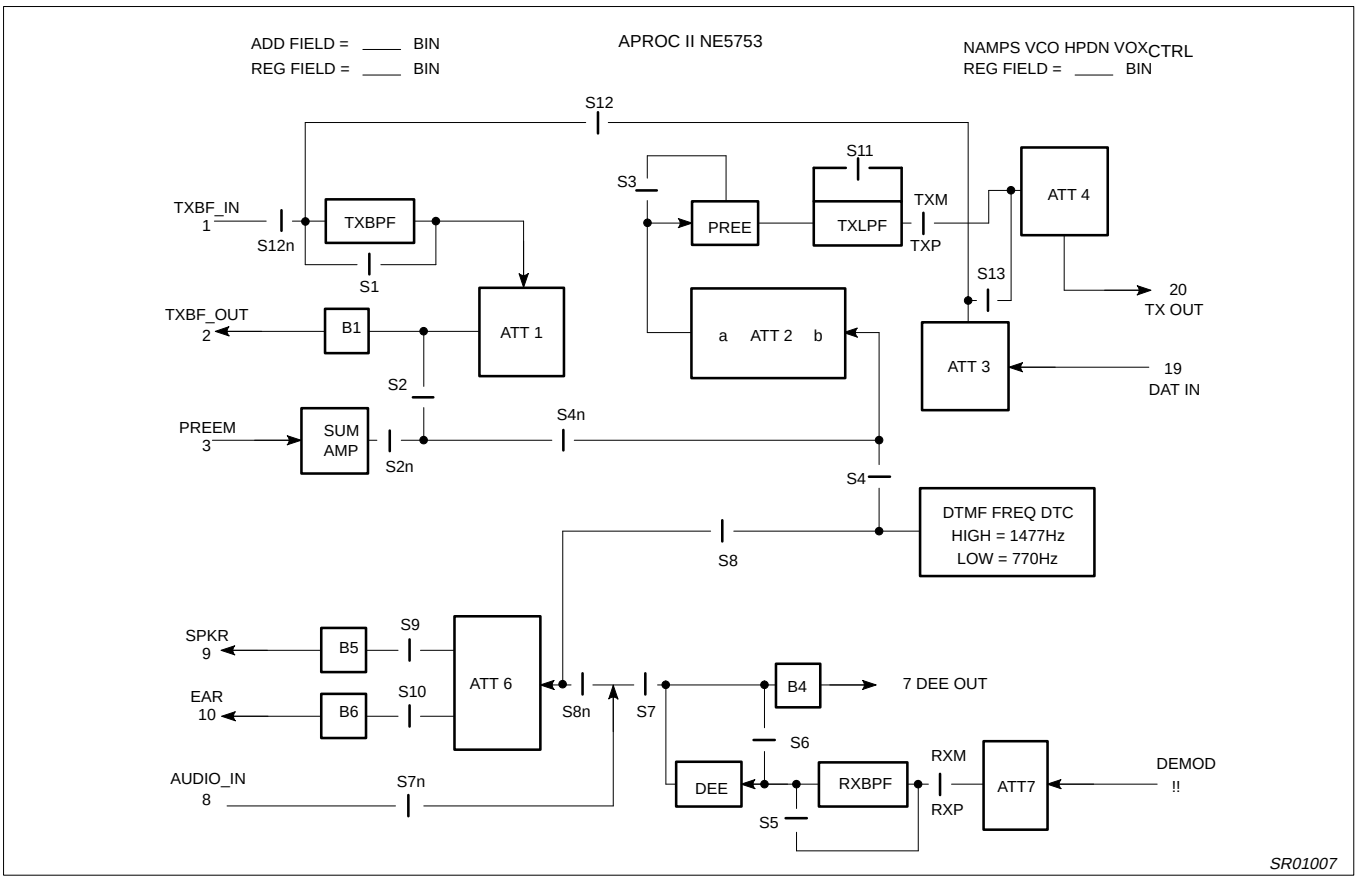

Figure 15. Graphical Display of SA5753 I²C Evaluation Program

Table 11. Gain Attenuator Steps

SYMBOL	Sequence of Gain Attenuator Steps
A1	0, –0.8, –1.6, –2.4, –3.2, –4.0, –4.8, –5.6, –6.4, –7.2, –8.0, –8.8, –9.6, –10.4 –11.2, –12
A2a	0, 0.25, 0.50, 0.75, 1.00, 1.25, 1.50, 1.75, 2.00, 2.25, 2.50, 2.75, 3.00, 3.25, 3.50, 3.75, 0, –0.25, –0.50, –0.75, –1.00, –1.25, –1.50, –1.75, –2.00, –2.25, –2.50, –2.75, –3.00, –3.25, –3.50, –3.75
A2b	0, –12, –18, –24
A3	–2, –3, –4, –5, –6, –7, –8, –9, –10, –11, –12, –13, –14, –15, –16, –17
A4	0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 0, –0.5, –1.0, –1.5, –2.0, –2.5, –3.0, –3.5
A6	0, –2, –4, –6, –8, –10, –12, –14, –16, –18, –20, –22, –24, –26, –28, –30
A7	0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5, 0, –0.5, –1, –1.5, –2, –2.5, –3, –3.5