Features

- **Comprehensive Library of Standard Logic and I/O Cells**
- **ATC18 Core and I/O Cells Designed to Operate with V_{DD} = 1.8V ± 0.15V as Main Target Operating Conditions**
- **IO25 and IO33 Pad Libraries Provide Interfaces to 2.5V and 3V Environments**
- **Memory Cells Compiled to the Precise Requirements of the Design**
- **Compatible with Atmel's Extensive Range of Microcontroller, DSP, Standard-interface and Application-specific Cells**

Description

The Atmel ATC18 CBIC family is fabricated on a proprietary 0.18 micron, up to six-layer-metal CMOS process intended for use with a supply voltage of 1.8V ± 0.15V. The following table shows the range for which Atmel library cells have been characterized.

Table 1. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	DC Supply Voltage	Core and Standard I/Os	1.65	1.8	1.95	V
$V_{DD2.5}$	DC Supply Voltage	2.5V Interface I/Os	2.25	2.5	2.75	V
$V_{DD3.3}$	DC Supply Voltage	3V Interface I/Os	3	3.3	3.6	V
V_I	DC Input Voltage		0		V_{DD}	V
V_O	DC Output Voltage		0		V_{DD}	V
TEMP	Operating Free Air Temperature Range	Industrial	-40		+85	°C

The Atmel cell libraries and megacell compilers have been designed in order to be compatible with each other. Simulation representations exist for three types of operating conditions. They correspond to three characterization conditions defined as follows:

- MIN conditions:
  T_J = -40°C
  V_{DD} (cell) = 1.95V
  Process = fast (industrial best case)
- TYP conditions:
  T_J = +25°C
  V_{DD} (cell) = 1.8V
  Process = typ (industrial typical case)
- MAX conditions:
  T_J = +100°C
  V_{DD} (cell) = 1.60V
  Process = slow (industrial worst case)

Delays to tri-state are defined as delay to turn off (VGS < VT) of the driving devices. Output pad drain current corresponds to the output current of the pad when the output voltage is V_{OL} or V_{OH}. The output resistor of the pad and the voltage drop due to access resistors (in and out of the die) are taken into account. In order to have accurate timing estimates, all characterization has been run on electrical netlists extracted from the layout database.

Cell-based ASIC

ATC18

Summary

Rev. 1389AS–11/00

Standard Cell Library SClib

The Atmel Standard Cell Library, SClib, contains a comprehensive set of combinational logic and storage cells. The SClib library includes cells which belong to the following categories:

- Buffers and Gates
- Multiplexers
- Flip-flops
- Scan Flip-flops
- Latches
- Adders and Subtractors

Decoding the Cell Name

Table 2 shows the naming conventions for the cells in the SClib library. Each cell name begins with either a two-, three-, or four-letter code that defines the type of cell. This indicates the range of standard cells available.

Table 2. Cell Codes

Code	Description	Code	Description
AD	Adder	INVT	Inverting 3-State Buffer
AH	Half Adder	JK	JK Flip-Flop
AS	Adder/Subtractor	LA	D Latch
AN	AND Gate	MI	Inverting Multiplexer
AOI	AND-OR-Invert Gate	MX	Multiplexer
AON	AND-OR-AND-Invert Gates	ND	NAND Gate
AOR	AND-OR Gate	NR	NOR Gate
BH	Bus Holder	OAI	OR-AND-Invert Gate
BUFB	Balanced Buffer	OAN	OR-AND-OR-Invert Gates
BUFF	Non-Inverting Buffer	OR	OR Gate
BUFT	Non-Inverting 3-State Buffer	ORA	OR-AND Gate
CG	Carry Generator	SD	Multiplexed Scan D Flip-Flop
CLK2	Clock Buffer	SE	Multiplexed Scan Enable D Flip-Flop
DE	D-Enabled Flip-Flop	SRLA	Set/Reset Latches with NAND input
DF	D Flip-Flop	SU	Subtractor
INV0	Inverter	XN	Exclusive NOR Gate
INVB	Balanced Inverter	XR	Exclusive OR Gate

Cell Matrices

Table 3, Table 4 and Table 5 provide a quick reference to the storage elements in the SClib library. Note that all storage elements feature buffered clock inputs and buffered output.

Table 3. JK Flip-Flops

Macro Name	Set	Clear	1xDrive	2xDrive
JKBRBx	•	•	•	•

Table 4. D Flip-Flops

Macro Name	Set	Clear	Enabled D Input	1xDrive	2xDrive	Single Output
DFBRBx	•	•		•	•	
DFCRBx		•		•	•	
DFCRQx		•		•	•	•
DFCRNx		•		•	•	
DFNRBx				•	•	
DFNRQx				•	•	•
DFPRBx	•			•	•	
DEPRQx	•		•	•	•	•
DENRQx			•	•	•	•
DENRBx			•	•	•	
DECRQx		•	•	•	•	•

Table 5. Scan Flip-flops

Macro Name	Set	Clear	1xDrive	2xDrive	Single Output
SDBRBx	•	•	•	•	
SDCRBx		•	•	•	
SDCRNx		•	•	•	•
SDCRQx		•	•	•	•
SDNRBx			•	•	
SDNRNx			•	•	•
SDNRQx			•	•	•
SDPRBx	•		•	•	
SECRQx		•	•	•	•
SENRQx			•	•	•
SEPRQx	•		•	•	•

Input/Output Pad Cell Libraries IO18lib, IO25lib and IO33lib

The Atmel Input/Output Cell Library, IO18lib, contains a comprehensive list of input, output, bidirectional and tristate cells. The ATC18 (1.8V) cell library includes two special sets of I/O cells, IO25lib and IO33lib, for interfacing with external 2.5V and 3.3V devices.

Voltage Levels

The IO18lib library is made up exclusively of low-voltage chip interface circuits powered by a voltage in the range of 1.65V to 1.95V. The library is compatible with the SClib 1.8-volt standard cells library.

Power and Ground Pads

Designers are strongly encouraged to provide three kinds of power pairs for the IO18lib library. These are “AC”, “DC” and core power pairs. AC power is used by the I/O to switch its output from one state to the other. This switching generates noise in the AC power buses on the chip. DC power is used by the I/O to maintain its output in a steady state. The best noise performance is achieved when the DC power buses on the chip are free of noise; designers are encouraged to use separate power pairs for AC and DC power to prevent most of the noise in the AC power buses from reaching the DC power buses. The same power pairs can be used to supply both DC power to the I/Os and power to the core without affecting noise performance.

Table 6. VSS Power Pad Combinations

Core	Switching I/O	Quiet I/O		
Vssi	**VssAC**	**VssDC**	**Library Cell Name**	**Signal Name**
•			pv18i18	VDD
	•		pv18a18	VDD
		•	pv18d18	VDD
	•	•	pv18e18	VDD
•		•	pv18b18	VDD
•	•	•	pv18f18	VDD

Table 7. VDD Power Pad Combinations

Core	Switching I/O	Quiet I/O		
Vssi	**VssAC**	**VssDC**	**Library Cell Name**	**Signal Name**
	•		pv18i18	VDD
		•	pv18a18	VDD
	•	•	pv18d18	VDD
•		•	pv18e18	VDD
•	•	•	pv18b18	VDD
	•		pv18f18	VDD

Cell Matrices

Table 8. CMOS Pads

CMOS Cell Name	3-state I/O	Output Only	3-state Output Only	Drive Strength	Pad Sites Used
PC18B01	•			1x	1
PC18B02	•			2x	1
PC18B03	•			3x	1
PC18B04	•			4x	1
PC18B05	•			5x	1
PC18O01		•		1x	1
PC18O02		•		2x	1
PC18O03		•		3x	1
PC18O04		•		4x	1
PC18O05		•		5x	1
PC18T01			•	1x	1
PC18T02			•	2x	1
PC18T03			•	3x	1
PC18T04			•	4x	1
PC18T05			•	5x	1

Table 9. TTL Pads

TTL Cell Name	3-state I/O	Output Only	3-state Output Only	Drive Strength	Pad Sites Used
PT18B01	•			2 mA	1
PT18B02	•			4 mA	1
PT18B03	•			8 mA	1
PT18O01		•		2 mA	1
PT18O02		•		4 mA	1
PT18O03		•		8 mA	1
PT18T01			•	2 mA	1
PT18T02			•	4 mA	1
PT18T03			•	8 mA	1

Table 10. CMOS/TTL Input Only Pad

CMOS Cell Name	Input Levels	Schmitt Input Level Shifter	Non-inverting	Inverting	Pad Sites Used
PC18D01	CMOS		•		1
PC18D11	CMOS			•	1
PC18D21	CMOS	•	•		1
PC18D31	CMOS	•		•	1

Note: All 3-state I/Os, 3-state output only and input pads are also available with pull-up and pull-down device.

IO25lib and IO33lib Low Slew Rate Cells

The IO25lib (IO33lib) cells comprise a series of 1.8V/2.5V (1.8V/3.3V) input/output pads developed for low supply voltage processes in order to interface 1.8V ASICs to 2.5V (3.3V) environments.

All IO25lib (IO33lib) cells are slew rate controlled. Advantage has been taken of the 1.8V to 2.5V (3.3V) level shifter (slow by construction) to reduce the slew rate without reducing speed.

Table 11. IO25lib/IO33lib Pads

3V Interface Pad Name	3-state I/O	Output Only	3-state Output Only	Input Only	Drive Strength	Pad Sites Used
pc25b0x/pc33b0x	•				2 mA, 4 mA, 8 mA, 16 mA	1
pc25d00/pc33d00				•		1
pc25o0x/pc33o0x		•			2 mA, 4 mA, 8 mA, 16 mA	1
pc25t0x/pc33t0x			•		2 mA, 4 mA, 8 mA, 16 mA	1

Note: All 3-state I/Os, 3-state output only and input pads are also available with pull-up and pull-down devices.

Table 12. IO25lib/IO33lib Power Pads

Cell Name	Power Bus Connection				Pad Sites Used
	vssi	mixvssi	vddi	mixvdd	
pv25e00/pv33e00		•			1
pv25i00/pv33i00	•				1
pv25i25/pv33i25			•		1
pv25e33/pv33e33				•	1
pv25ecrn/pv33ecrn		•		•	2

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-803-000
FAX (44) 1355-242-743

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex
France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

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