

Dual high slew rate operational amplifier

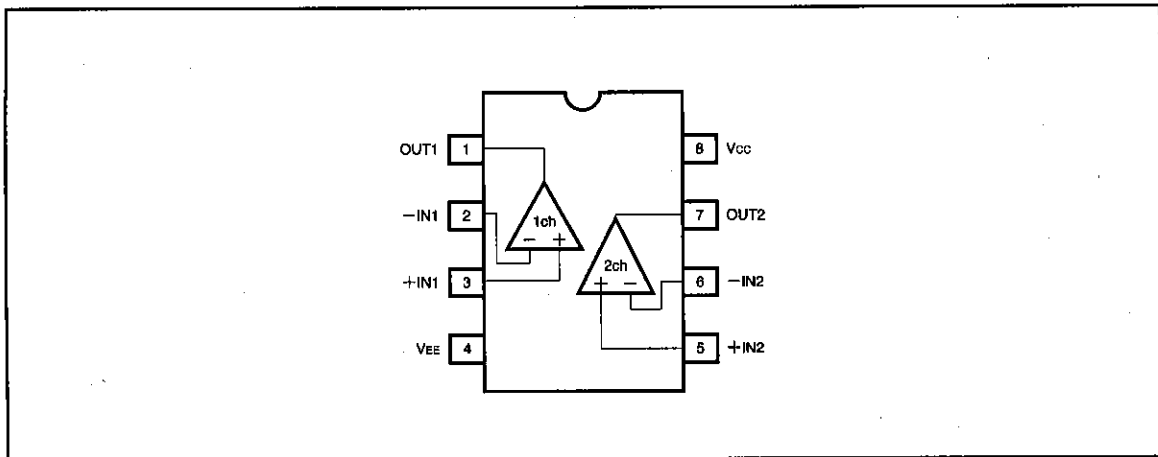
BA4510F/BA4510FV

The BA4510F and BA4510FV are monolithic ICs that contain two operational amplifiers with high slew rate, featuring phase compensation. These ICs can be driven with a low-voltage power supply, requiring a power supply range of ± 1 to ± 3.5 V for a dual power supply and 2 to 7V for a single power supply. In addition, an unbuffered type is used which enables ample output even in low voltage ranges, enabling swing at up to nearly the power supply voltage.

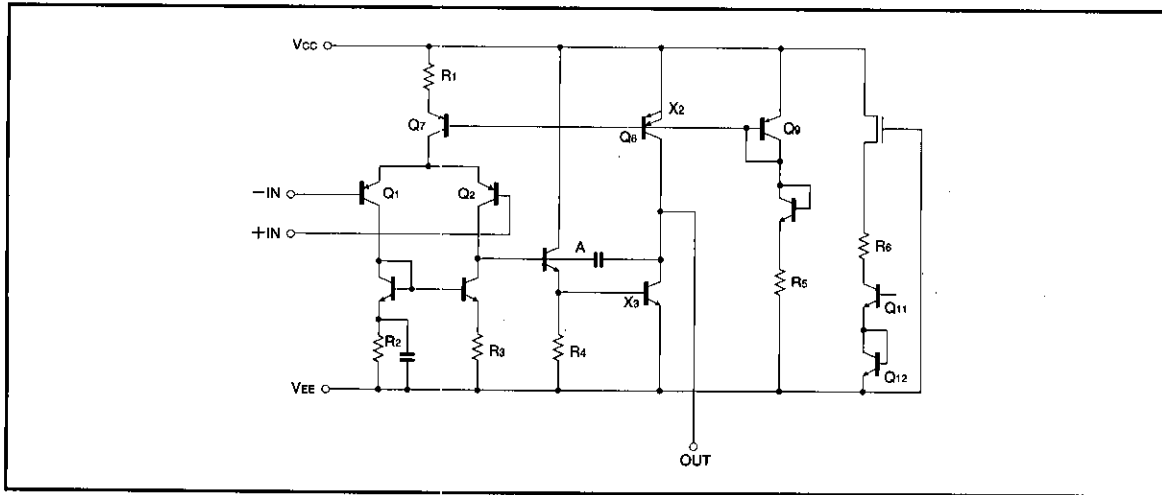
●Features

- 1) Low-voltage operation.
- 2) High slew rate.
- 3) Wide dynamic output range.
- 4) Compact 8-pin SSOP-B package. (BA4510FV)

●Block diagram



● Internal circuit configuration diagram



● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{CC}	±5	V
Power dissipation	P _d	550*1 (SOP)	mW
		350*2 (SSOP)	
Differential input voltage	V _{IO}	±V _{CC}	V
In-phase input voltage	V _I	0~V _{CC}	V
Operating temperature	T _{opr}	-20~75	°C
Storage temperature	T _{stg}	-40~125	°C

*1 If used at temperatures higher than 25°C, reduce power by 5.5 mW for each 1°C above Ta = 25°C.

This value is the value measured when mounted on a glass epoxy board (50 mm × 50 mm × 1.6 mm).

*2 If used at temperatures higher than 25°C, reduce power by 3.5 mW for each 1°C above Ta = 25°C.

This value is the value measured when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

The value is 300 mW when the IC is used alone.

●Electrical characteristics (Unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_{CC} = \pm 2.5\text{V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Input offset voltage	V_{IO}	—	1	6	mV	$R_s=50\ \Omega$	
Input offset current	I_{IO}	—	2	200	nA		
Input bias current	I_B	—	80	500	nA	*1	
High-amplitude voltage gain	A_V	60	90	—	dB	$R_L \geq 2\text{k}\ \Omega$, $V_{CC}=15\text{V}$	
Common mode input voltage range	V_{ICM}	-1.3	—	1.5	V		
Common mode rejection ratio	CMRR	60	80	—	dB		
Power supply voltage rejection ratio	PSRR	60	80	—	dB	$R_s=50\ \Omega$	
Quiescent circuit current	I_Q	2.5	5.0	7.5	mA	$R_L=\infty$ ALL AMPS	
Output voltage range	Hi	V_{OH}	2.0	2.4	—	V	$R_L=2\text{k}\ \Omega$
	Low	V_{OL}	—	-2.4	-2.0	V	$R_L=2\text{k}\ \Omega$
Slew rate	S.R.	—	5	—	V / μs		

*1 Because the initial stage is configured by the PNP transistor, the direction of the input bias current is the direction of the flow from the IC.

●Electrical characteristic curve

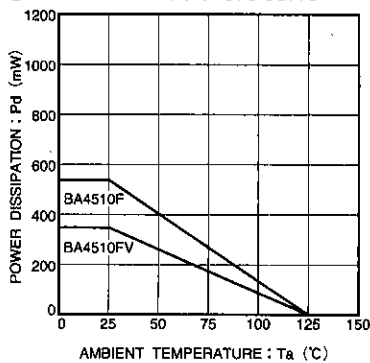


Fig. 1 Power dissipation - ambient temperature characteristic

●Operation notes

- Unused circuit connections
If there are any circuits which are not being used, we recommend making connections as shown in Figure 2, with the non-inverted input pin connected to the potential within the in-phase input voltage range (V_{ICM}).
- If used with a voltage follower, be careful of oscillation which may cause problems with the in-line input voltage range or the capacitance load.
- If using at power supply voltage +5.0 or higher, be sure the gain is reduced sufficiently to prevent oscillation.

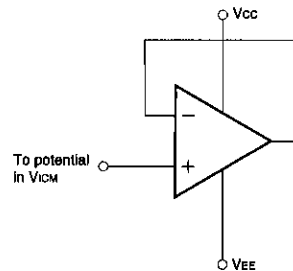
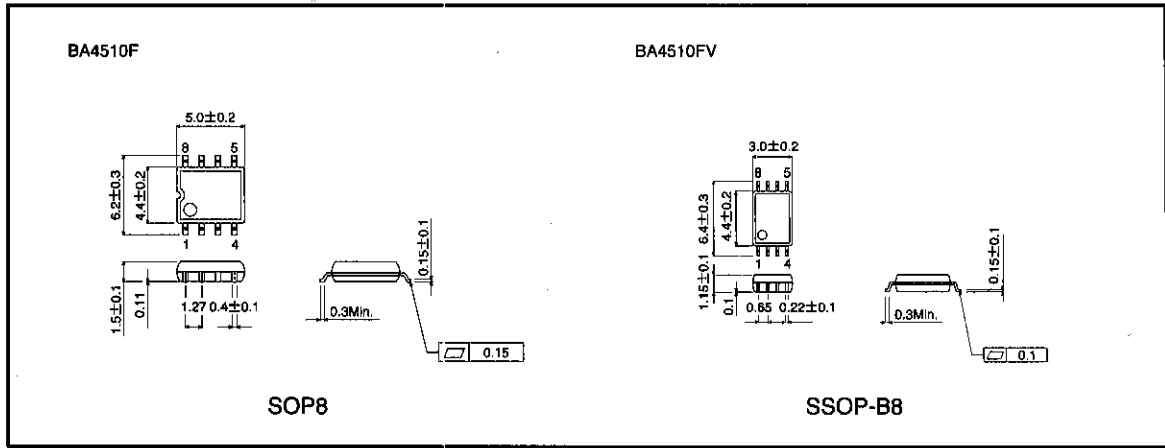


Fig. 2 Unused circuit connections

● External dimensions (Units: mm)



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