

2-channel driver for CD changers

BA6780

The BA6780 is a 2-channel driver IC for CD changers that includes a reversible, variable speed electronic governor and a reversible driver. On sets that have dual-rail power supplies, the BA6780 can be operated from just the negative supply to reduce influence on the positive power supply.

The input uses PWM control, and it is possible to directly input from a microprocessor running off the positive power supply.

●Applications

Changers for CD players and MD players.

●Features

- 1) Output voltage can be freely set using the output voltage setting pin.
- 2) Internal mute function if the power supply voltage drops.
- 3) Thermal shutdown function.
- 4) PWM input.
- 5) Settable reference voltage output pin.
- 6) Wide operating supply voltage range.

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{CC}	18	V
Logic input voltage	V _{FIN} , V _{RIN}	22	V
Power dissipation	P _d	1.31*1	W
Maximum current consumption	I _{max}	1.4*2	A
Operating temperature	T _{opr}	-25~+75	°C
Storage temperature	T _{stg}	-55~+150	°C

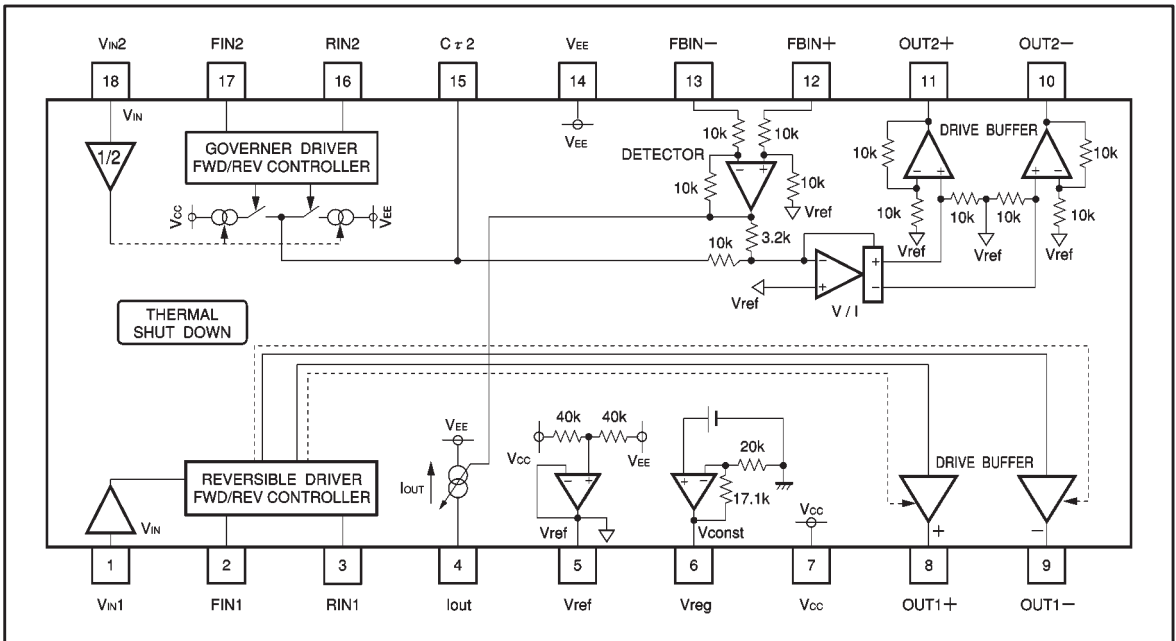
*1 When a DIP18 package is used. Reduced by 10.48mW for each increase in Ta of 1°C over 25°C.

*2 Should not exceed Pd or ASO values.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{CC}	7~16	V
Input voltage for pins 1 and 18	V _{IN}	0~V _{CC} /2-1.0	V

● Block diagram

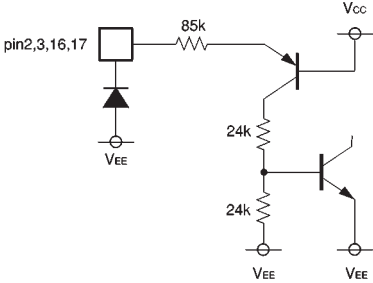
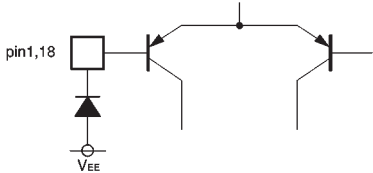
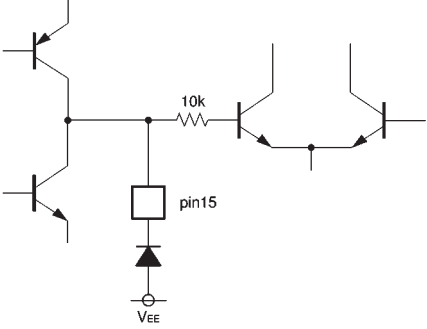
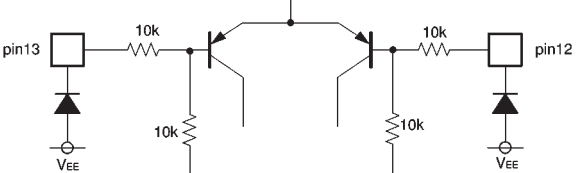


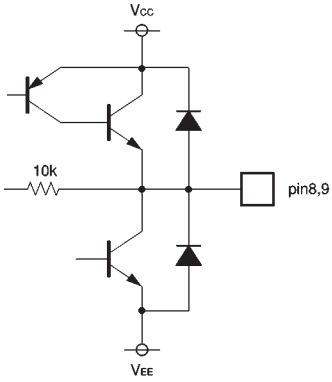
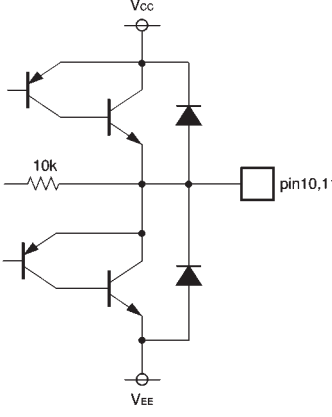
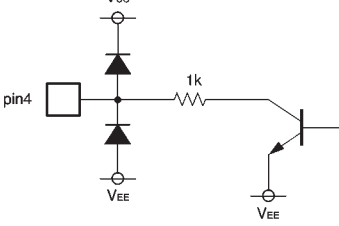
● Pin descriptions

Pin No.	Pin name	I/O	Function
1	V _{IN1}	I	Input pin for setting high output voltage for the reversible driver
2	FIN1	I	Input pin for forward control signal for the reversible driver
3	RIN1	I	Input pin for reverse control signal for the reversible driver
4	I _{OUT}	O	Governor load current detector output (open collector*1)
5	V _{ref}	O	Internal reference voltage pin
6	V _{reg}	O	4.6V constant voltage output
7	V _{cc}	I	Power supply (+)
8	OUT1+	O	Reversible driver output (+)
9	OUT1-	O	Reversible driver output (-)
10	OUT2-	O	Governor output (-)
11	OUT2+	O	Governor output (+)
12	FBIN+	I	Governor load current detector amplifier input (+)
13	FBIN-	I	Governor load current detector amplifier input (-)
14	V _{EE}	I	Power supply (-) (connection within substrate)
15	Cτ 2	I	For connection of capacitor for the governor PWM filter
16	RIN2	I	Governor reverse control signal input
17	FIN2	I	Governor forward control signal input
18	V _{IN2}	I	Input pin for setting high output voltage for the governor

*1 Refer to operating notes.

● Input / output circuits

Pin function	Equivalent circuit
Logic input	 <p>The diagram shows a logic input circuit. A square box representing the input is connected to a diode pointing towards the V_{EE} terminal. The other side of the input box is connected to a resistor labeled 85k, which is in series with the base of a PNP transistor. The emitter of this PNP transistor is connected to the V_{CC} terminal. The base of the PNP transistor is also connected to the base of an NPN transistor. The emitter of this NPN transistor is connected to a resistor labeled 24k, which is in series with the V_{EE} terminal. The collector of the NPN transistor is connected to the base of another NPN transistor. The emitter of this second NPN transistor is connected to a resistor labeled 24k, which is in series with the V_{EE} terminal. The collector of the second NPN transistor is connected to the V_{EE} terminal.</p>
Voltage setting input	 <p>The diagram shows a voltage setting input circuit. A square box representing the input is connected to a diode pointing towards the V_{EE} terminal. The other side of the input box is connected to the base of a PNP transistor. The emitter of this PNP transistor is connected to the V_{CC} terminal. The collector of the PNP transistor is connected to the base of an NPN transistor. The emitter of this NPN transistor is connected to the V_{EE} terminal. The collector of the NPN transistor is connected to the base of another NPN transistor. The emitter of this second NPN transistor is connected to the V_{EE} terminal. The collector of the second NPN transistor is connected to the V_{EE} terminal.</p>
For connection of capacitor for PWM filter	 <p>The diagram shows a circuit for connecting a capacitor for a PWM filter. A square box representing the input is connected to a diode pointing towards the V_{EE} terminal. The other side of the input box is connected to a node between two NPN transistors. The emitter of the top NPN transistor is connected to the V_{CC} terminal. The collector of the top NPN transistor is connected to the base of the bottom NPN transistor. The emitter of the bottom NPN transistor is connected to the V_{EE} terminal. The collector of the bottom NPN transistor is connected to the V_{EE} terminal. A resistor labeled 10k is connected between the node and the base of the bottom NPN transistor. A diode is connected between the node and the V_{EE} terminal.</p>
Load current detector	 <p>The diagram shows a load current detector circuit. A square box representing the input is connected to a diode pointing towards the V_{EE} terminal. The other side of the input box is connected to a resistor labeled 10k, which is in series with the base of a PNP transistor. The emitter of this PNP transistor is connected to the V_{CC} terminal. The base of the PNP transistor is also connected to a resistor labeled 10k, which is in series with the V_{EE} terminal. The collector of the PNP transistor is connected to the base of an NPN transistor. The emitter of this NPN transistor is connected to the V_{EE} terminal. The collector of the NPN transistor is connected to the base of another NPN transistor. The emitter of this second NPN transistor is connected to a resistor labeled 10k, which is in series with the V_{EE} terminal. The collector of the second NPN transistor is connected to the V_{EE} terminal. A square box representing the output is connected to the collector of the second NPN transistor. A diode is connected between the output box and the V_{EE} terminal.</p>

Pin function	Equivalent circuit
<p>Output (reversible driver)</p>	 <p>The circuit for pin 8,9 is a reversible driver. It features a central node connected to pin 8,9. This node is pulled up to V_{CC} by a 10k resistor. The node is also connected to the emitters of two NPN transistors. The base of the upper transistor is connected to V_{CC}, and the base of the lower transistor is connected to V_{EE}. The collectors of both transistors are connected to V_{CC}. Two diodes are connected in series between the central node and V_{EE}, with the cathode of the upper diode connected to the central node and the anode of the lower diode connected to V_{EE}.</p>
<p>Output (governor)</p>	 <p>The circuit for pin 10,11 is a governor output. It features a central node connected to pin 10,11. This node is pulled up to V_{CC} by a 10k resistor. The node is also connected to the emitters of two NPN transistors. The base of the upper transistor is connected to V_{CC}, and the base of the lower transistor is connected to V_{EE}. The collectors of both transistors are connected to V_{CC}. Two diodes are connected in series between the central node and V_{EE}, with the cathode of the upper diode connected to the central node and the anode of the lower diode connected to V_{EE}.</p>
<p>Load current detector signal output (governor)</p>	 <p>The circuit for pin 4 is a load current detector signal output. It features a central node connected to pin 4. This node is pulled up to V_{CC} by a 1k resistor. The node is also connected to the emitters of two diodes. The anode of the upper diode is connected to V_{CC}, and the cathode of the lower diode is connected to V_{EE}. The collector of the lower diode is connected to the base of an NPN transistor, whose emitter is connected to V_{EE}.</p>

● Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{CC} = 10V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I _Q	—	8.0	16.0	mA	Open mode with no load
Mute on voltage	V _{CC1}	—	—	3.5	V	Mute on voltage when V _{CC} falls
Mute off voltage	V _{CC2}	5.5	—	—	V	Mute off voltage when V _{CC} rises
V _{ref} input voltage range	V _{IN}	0	—	4	V	—
V _{ref} pin current	I _{IN}	—	0.02	1.0	μA	—
PWM input high level voltage	V _{IH}	4.0	—	—	V	With V _{CC} as the reference potential
PWM input low level voltage	V _{IL}	—	—	1.0	V	With V _{CC} as the reference potential
PWM input high level current	I _{IH}	—	—	100	μA	—
PWM input low level current	I _{IL}	−1.0	—	1.0	μA	—

〈Electronic governor〉

Output offset voltage	V _{OF}	−100	0	100	mV	RL (load)=9Ω, RO (current detector)=0.6Ω	
Max. pin-to-pin output voltage	V _{OM}	6.0	6.5	—	V	RL (load)=9Ω, RO (current detector)=0.6Ω	
Pin-to-pin output voltage 1-1	V _{OUT11}	4.2	4.7	5.2	V	Forward mode	12 and 13 open
Pin-to-pin output voltage 1-2	V _{OUT12}	−5.2	−4.7	−4.2	V	Reverse mode	RL (load)=9Ω
Pin-to-pin output voltage 1-3	V _{OUT13}	−100	0	100	mV	Brake mode	RO (current detector)=0.6Ω
Pin-to-pin output voltage 1-4	V _{OUT14}	−50	0	50	mV	Stop mode	V _{ref} =2.5V
Voltage gain of positive feedback amplifier	G _{VNF}	20.5	22.0	23.5	dB	V _{ref} =0V, V _{IN} =−20dBV, f=1kHz	

〈Reversible driver〉

Output saturation voltage	V _{CEsat}	—	1.0	2.1	V	I _o =100mA, V _{ref} =5V, Total of upper side and lower side ineffective voltage of output Tr	
Pin-to-pin output voltage 2-1	V _{OUT21}	4.5	5.0	5.5	V	Forward mode	I _c =100mA V _{ref} =2.5V
Pin-to-pin output voltage 2-2	V _{OUT22}	−5.5	−5.0	−4.5	V	Reverse mode	
Pin-to-pin output voltage 2-3	V _{OUT23}	−50	0	50	mV	Brake mode	
Pin-to-pin output voltage 2-4	V _{OUT24}	−50	0	50	mV	Stop mode	
Output load fluctuation	V _{OUT}	—	200	400	mV	Difference in output voltage for I=400mA and I=100mA	V _{ref} =2.5V

〈4.6V constant-voltage output〉

Output voltage	V _{reg}	4.35	4.60	4.85	V	—
Output load fluctuation (source)	V _{OSO}	−20	−5	—	mV	1mA source
Output load fluctuation (sink)	V _{OSI}	—	5	20	mV	1mA sink

© Not designed for radiation resistance.

● Measurement circuit

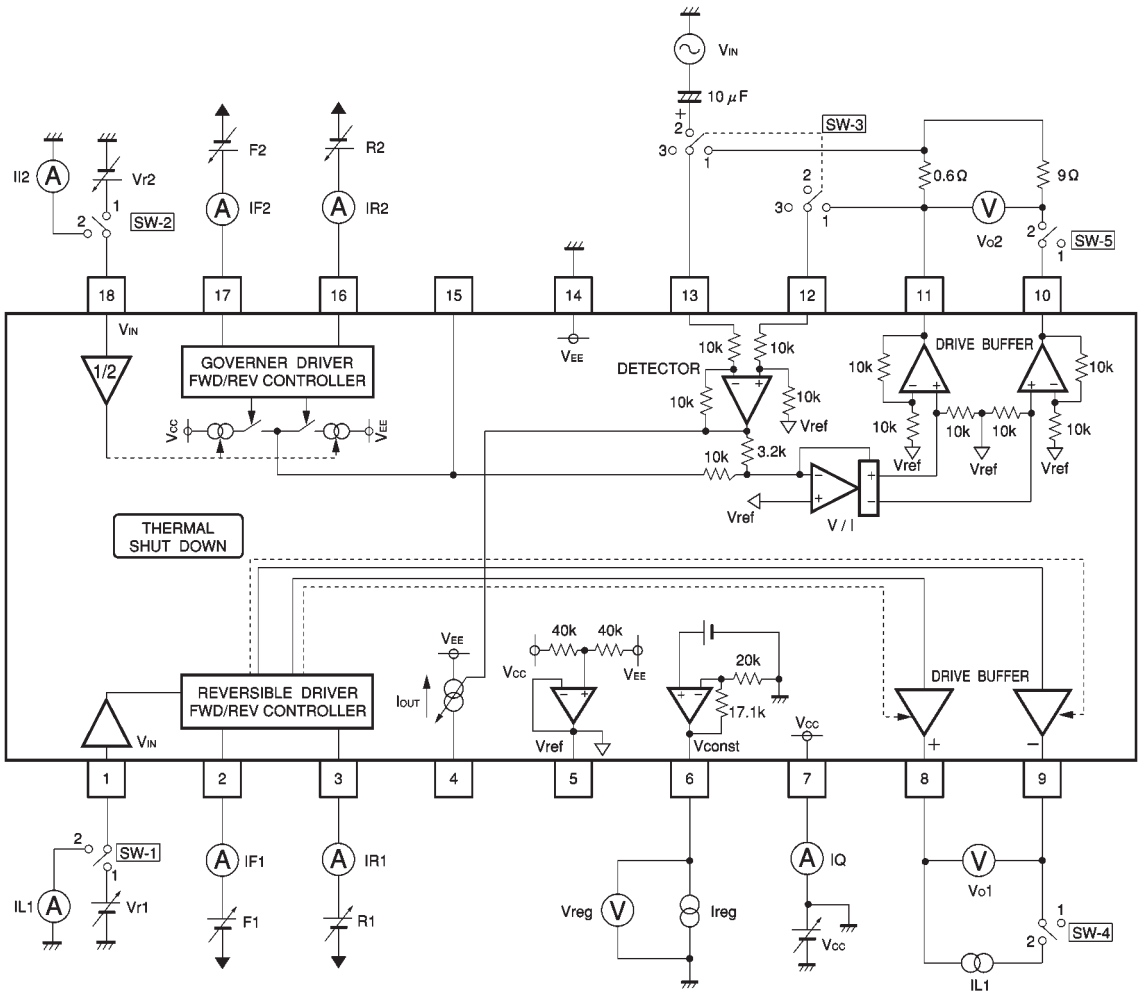


Fig.1

● Measurement circuit switch table

Parameter	SW					Input								Conditions	Measurement
	SW1	SW2	SW3	SW4	SW5	Vr1	Vr2	F1	R1	F2	R2	V _{IN}	IL1		
Quiescent current	1	1	3	1	1	0	0	0	0	0	0	—	—	—	IQ
Mute on voltage	1	1	3	1	1	2	0	0	5	0	0	—	—	V _{CC} swept down from 10V	Vo1
Mute off voltage	1	1	3	1	1	2	0	0	5	0	0	—	—	V _{CC} swept up from 0V	Vo1
V _{ref} input voltage range	1	1	3	1	2	*1	*1	0	5	0	5	—	—	*1 Check for abnormality in output in Vr1 and Vr2 input range	Vo1 Vo2
V _{ref} pin current	2	2	3	1	1	0	0	0	0	0	0	—	—	—	II1 II2
PWM input high level voltage	1	1	3	1	2	2	2	*2	*2	*2	*2	—	—	*2 Sweep the F/R input, and check that the mode switching is occurring in a range that satisfies the rated values	Vo1
PWM input low level voltage	1	1	3	1	2	2	2	*2	*2	*2	*2	—	—		Vo2
PWM input high level current	1	1	3	1	1	0	0	5	5	5	5	—	—	—	IF1 IF2
PWM input low level current	1	1	3	1	1	0	0	5	5	5	5	—	—	—	IR1 IR2
〈Electronic governor〉															
Output offset voltage	1	1	1	1	2	0	0	0	0	5	5	—	—	—	Vo2
Max. pin-to-pin output voltage	1	1	3	1	2	0	4	0	0	0	5	—	—	—	Vo2
										5	0				
Pin-to-pin output voltage 1-1	1	1	1	1	2	0	2.5	0	0	0	5	—	—	—	Vo2
Pin-to-pin output voltage 1-2	1	1	1	1	2	0	2.5	0	0	5	0	—	—	—	Vo2
Pin-to-pin output voltage 1-3	1	1	1	1	2	0	2.5	0	0	5	5	—	—	—	Vo2
Pin-to-pin output voltage 1-4	1	1	1	1	2	0	2.5	0	0	0	0	—	—	—	Vo2
Voltage gain of positive feedback amplifier	1	1	2	1	1	0	0	0	0	5	5	*3	—	*3 -20dBV, 1kHz	Vo2
〈Reversible driver〉															
Output saturation voltage	1	1	1	2	1	5	0	0	5	0	0	—	*4	*4 100mA (take care with polarity)	V _{CC} -Vo1
								5	0						
Pin-to-pin output voltage 2-1	1	1	3	2	1	2.5	0	0	5	0	0	—	*5	*5 100mA (take care with polarity)	Vo1
Pin-to-pin output voltage 2-2	1	1	3	2	1	2.5	0	5	0	0	0	—			
Pin-to-pin output voltage 2-3	1	1	3	1	1	2.5	0	5	5	0	0	—			
Pin-to-pin output voltage 2-4	1	1	3	1	1	2.5	0	0	0	0	0	—			
Output load fluctuation	1	1	3	2	1	2.5	0	0	5	0	0	—	*6	*6 Difference in output voltage for I=400mA and I=100mA	Vo1
								5	0						

Parameter	SW					Input								Conditions	Measurement
	SW1	SW2	SW3	SW4	SW5	Vr1	Vr2	F1	R1	F2	R2	V _{IN}	IL1		
〈4.6V constant-voltage output〉															
Output voltage	1	1	3	1	1	0	0	0	0	0	0	—	—	—	V _{reg}
Output load fluctuation (source)	1	1	3	1	1	0	0	0	0	0	0	—	—	Source I _{reg} =1mA	V _{reg}
Output load fluctuation (sink)	1	1	3	1	1	0	0	0	0	0	0	—	—	Sink I _{reg} =1mA	V _{reg}

●Application example

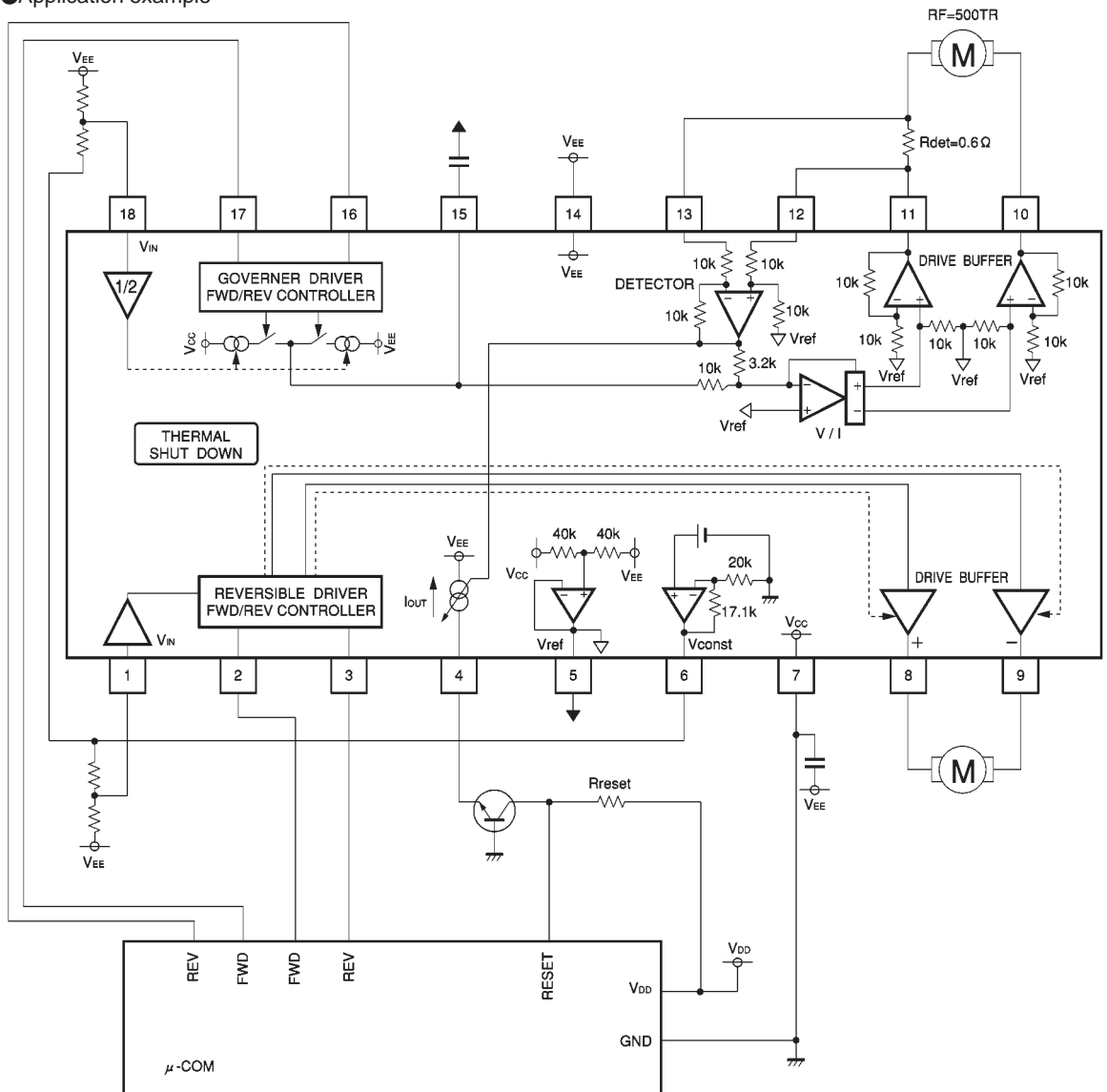


Fig.2

● Input / output truth table

〈Reversible drive〉

FIN	RIN	OUT (+)	OUT (-)	Mode
L	H	H	L	Forward mode
H	L	L	H	Reverse mode
H	H	L	L	Brake mode
L	L	OPEN	OPEN	Open mode

〈Governor drive〉

FIN	RIN	OUT (+)	OUT (-)	Mode
L	H	H	L	Forward mode
H	L	L	H	Reverse mode
H	H	$V_{CC} / 2$	$V_{CC} / 2$	Brake mode
L	L	OPEN	OPEN	Open mode

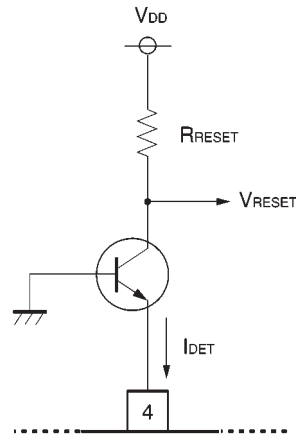
● Using the load current detector output pin (pin 4)

Refer to the example circuit on the right for the connection method. The V_{RESET} value is determined as follows:

$$I_{DET} = \frac{I_O \times R_{DET}}{3.2k\Omega} \quad V_{RESET} = V_{DD} - I_{DET} \times R_{RESET}$$

$$\therefore V_{RESET} = V_{DD} - \frac{I_O \times R_{DET} \times R_{RESET}}{3.2k\Omega}$$

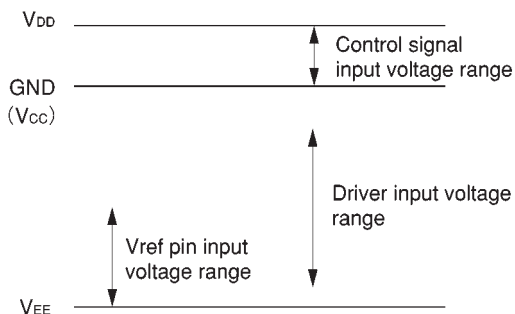
(R_{DET} is the load current detector resistance, refer to the application circuit)



●Operation notes

- (1) The BA6780 has a built in thermal shutdown circuit that mutes the output current when the chip temperature reaches 175°C (typ.). The hysteresis is set to 25°C (typ.), so the mute will be released when the chip temperature falls to 150°C (typ.).
- (2) The output current is muted when the supply (V_{CC}) falls to 3V or less. When the mute is applied, the reverse driver is set to the V_{EE} level, and the governor driver is set to the $V_{EE}/2$ level.

- (3) The V_{CC} voltage level is the reference for the logic input pin input voltage, so when it is converted from the V_{EE} potential, the high level becomes $(V_{CC} + 5.0)V$, and the low level becomes $(V_{CC})V$. The voltage potential levels for the pins are shown in the diagram below.
- (4) Connect a bypass capacitor at the base of this IC for the power supply.



●Electrical characteristics curves

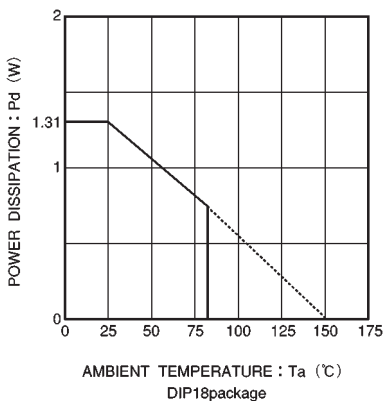


Fig.3 Thermal dissipation curve

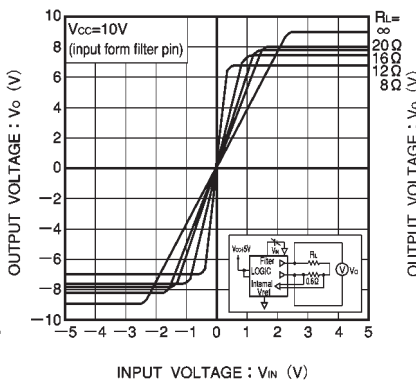


Fig.4 I/O characteristics with governor connected

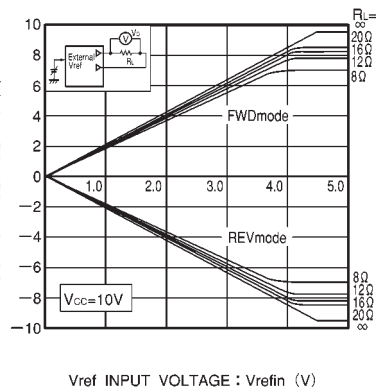


Fig.5 Reversible driver I/O characteristics

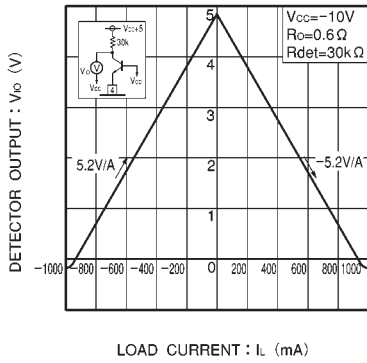


Fig.6 Load current detector output characteristics

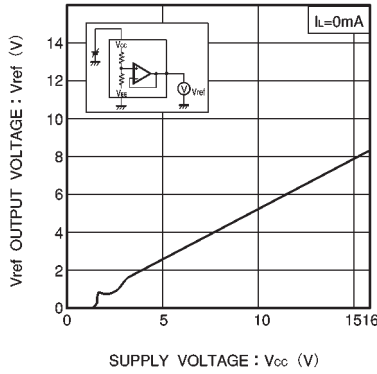


Fig.7 Internal Vref output characteristics

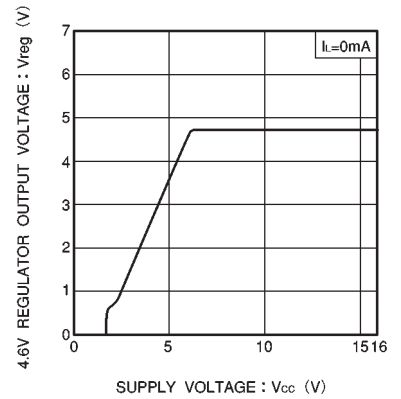


Fig.8 4.6V constant-voltage source output voltage characteristics

● External dimensions (Units: mm)

