

SYNC separator IC with AFC

BA7046/BA7046F

The BA7046 and BA7046F separates the synchronization signals from a video signal and outputs the horizontal and vertical synchronization signals (H_b and V_b), and the composite synchronization signal (Sync-out). The H_b and V_b pulse phase difference is guaranteed.

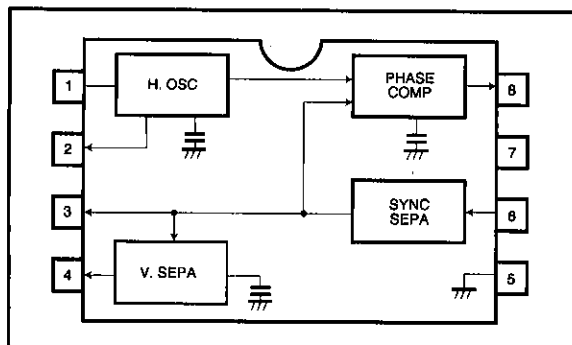
●Applications

TV and VCR

●Features

- 1) Built-in AFC circuit.
- 2) H_b and V_b phase difference guaranteed.
- 3) Low power dissipation. (approx. 21mW)
- 4) Low external parts count.
- 5) 8-pin DIP/SOP package.
- 6) Horizontal free-run frequency does not require adjustment.

●Block diagram



● Internal circuits

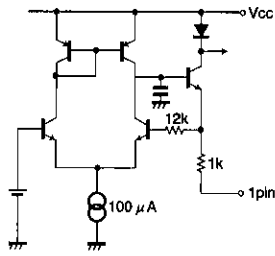


Fig. 1

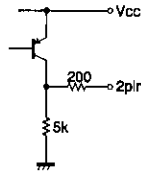


Fig. 2

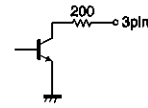


Fig. 3

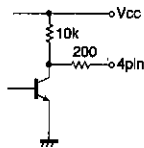


Fig. 4

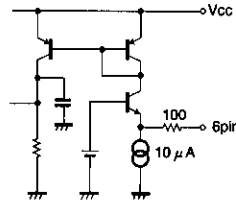


Fig. 5

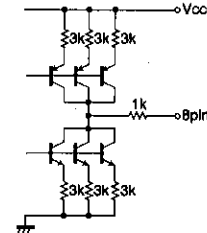


Fig. 6

● Absolute maximum ratings (Ta = 25°C)

BA7046 (DIP)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{CC Max.}	8.0	V
Power dissipation	P _d	500*	mW
Operating temperature	T _{opr}	-20~75	°C
Storage temperature	T _{stg}	-55~125	°C

* Reduced by 5mW for each increase in Ta of 1°C over 25°C.

BA7046F (SOP)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{CC Max.}	8.0	V
Power dissipation	P _d	350*	mW
Operating temperature	T _{opr}	-20~75	°C
Storage temperature	T _{stg}	-55~125	°C

* When mounted on a 50mm × 50mm PCB, reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

● Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V _{CC}	4.5	—	5.5	V

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● Electrical characteristics (Unless otherwise specified Ta=25°C and Vcc=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
Quiescent current	I _Q	2.0	4.1	6.2	mA	Pin 3 open	Fig.18
Minimum synchronization separation level	V _{syn-Min.}	—	0.08	0.15	V _{P-P}	Pin 6 terminated with 75Ω resistor	
Pulse voltage, LOW	V _{P-L}	—	0.1	0.3	V	2, 4pin	
Pulse voltage, HIGH	V _{P-H}	4.7	4.9	—	V	2, 4pin	
(Horizontal) free-running frequency	f _{H-O}	13.9	15.7	17.5	kHz	No input signal, I ₁ = open	
Capture range	Δf _{CAP}	±2.1	±2.9	—	kHz		
Lock-in phase difference	T _{HPH}	-1.0	0	+1.0	μs	2pin ↘ -6pin ↘	
H _b , V _b phase difference	T _{HVD}	17.0	23.5	30.0	μs	4pin ↘ -2pin ↗	
H _b pulse width	T _{HD}	4.6	5.1	5.6	μs	2pin ↘ ↗	
V _b pulse width	T _{VD}	190	230	270	μs	4pin ↘ ↗	

○ Not designed for radiation resistance.

● Electrical characteristic curves

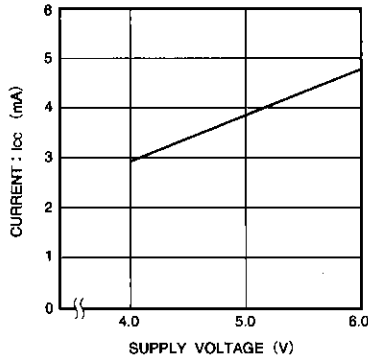


Fig. 7 Quiescent current vs. supply voltage

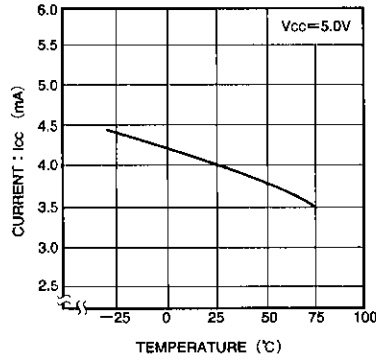


Fig. 8 Quiescent current vs. temperature

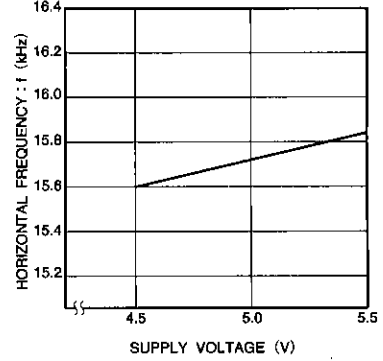


Fig. 9 Horizontal free-running frequency vs. supply voltage

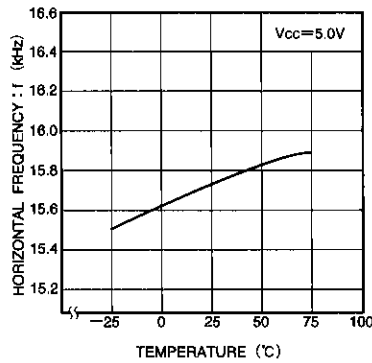


Fig. 10 Horizontal free-running frequency vs. temperature

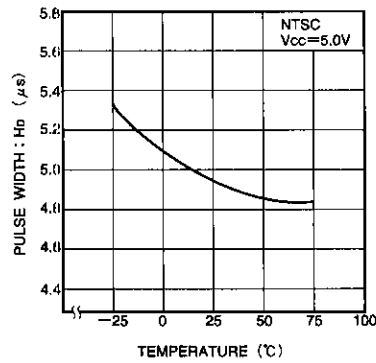


Fig. 11 H_b pulse width vs. temperature

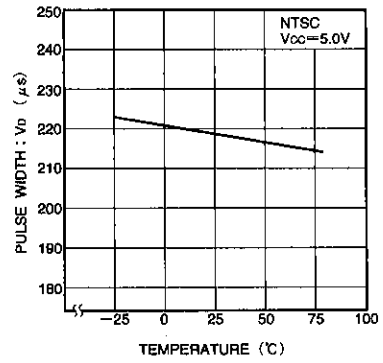


Fig. 12 V_b pulse width vs. temperature

●Electrical characteristic curves

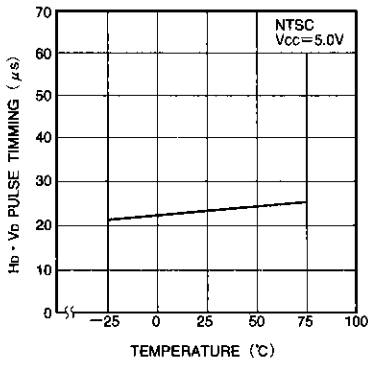


Fig. 13 H_b, V_b phase difference vs. temperature

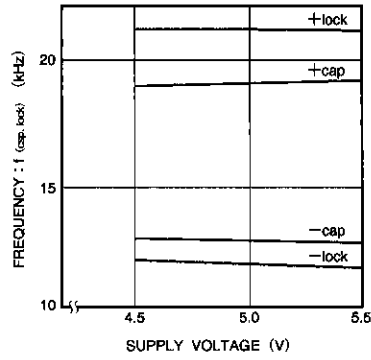


Fig. 14 Capture range/lock range vs. supply voltage

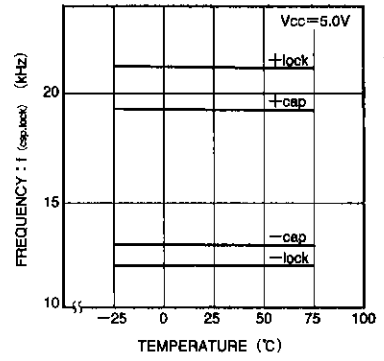


Fig. 15 Capture range charging/lock range vs. temperature

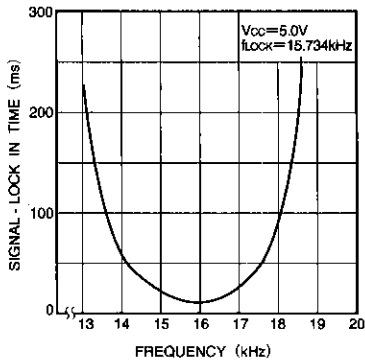


Fig. 16 Time from no signal to pull in

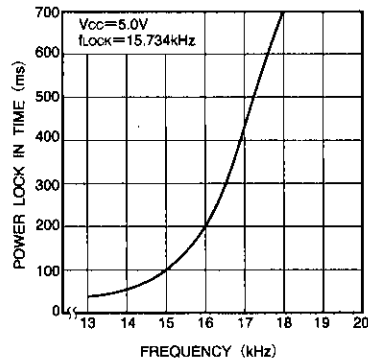


Fig. 17 Time from power on to pull in

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● Measurement circuit

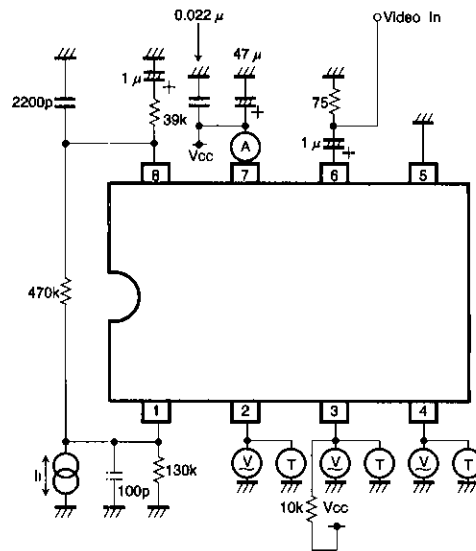


Fig. 18

● Circuit operation

- (1) Synchronization separation circuit
Detects the charging current to an externally-connected capacitor, and performs synchronization separation.
- (2) Horizontal oscillation circuit
When a video signal is input, it is synchronized with Hsync by the PLL. The horizontal free-running frequency is determined by external resistor R1.

$$f_{H-O} = \frac{2.05E6}{R1} \text{ [kHz]}$$

- (3) Vertical synchronization separation circuit
When a video signal is input, synchronization signal separation is done over the vertical synchronization pulse interval.

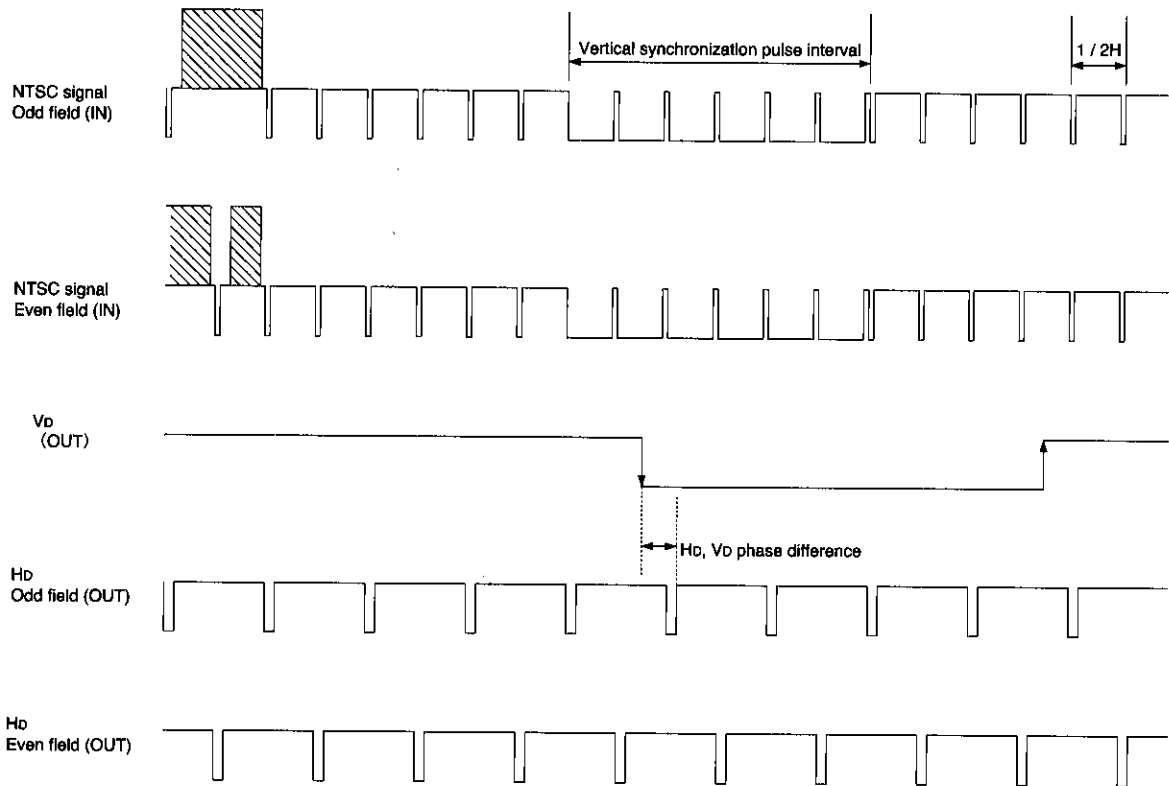
● Operation notes

- Make the ground line as thick as possible.
- Keep power supply noise to a minimum.

● Pin descriptions

Pin No.	Function
1	Horizontal oscillator resistor
2	H _D output
3	SYNC output (open collector)
4	V _D output
5	GND
6	Video input
7	Power supply
8	Phase comparator output

● V_{IN} , H_D , and V_D timing charts



1. The rise and fall positions for V_D are basically the same for both odd and even fields.
2. H_D shifts by $1/2H$ during the odd and even field interval.
3. Only the odd field is given for the specification.

Fig. 19

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● Application example

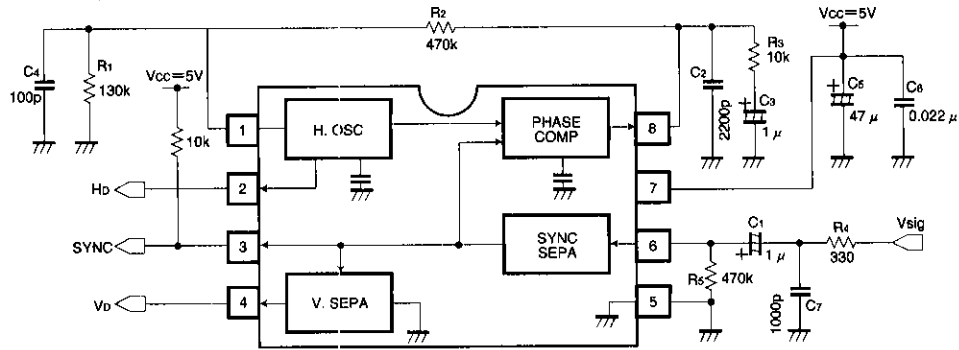


Fig. 20

- When SYNC SEPA output only is used, H_b and V_b unused.

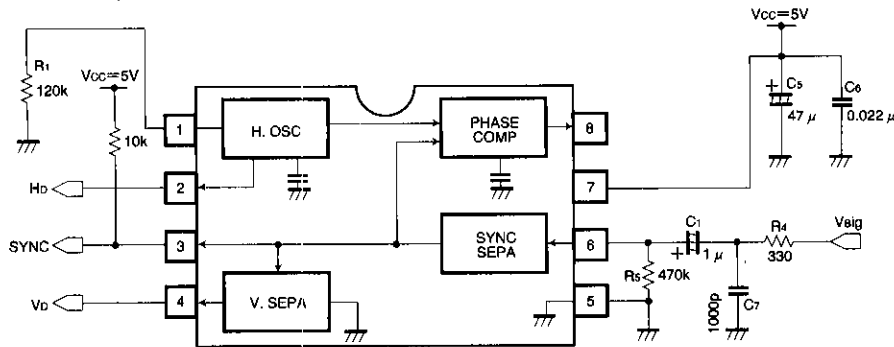


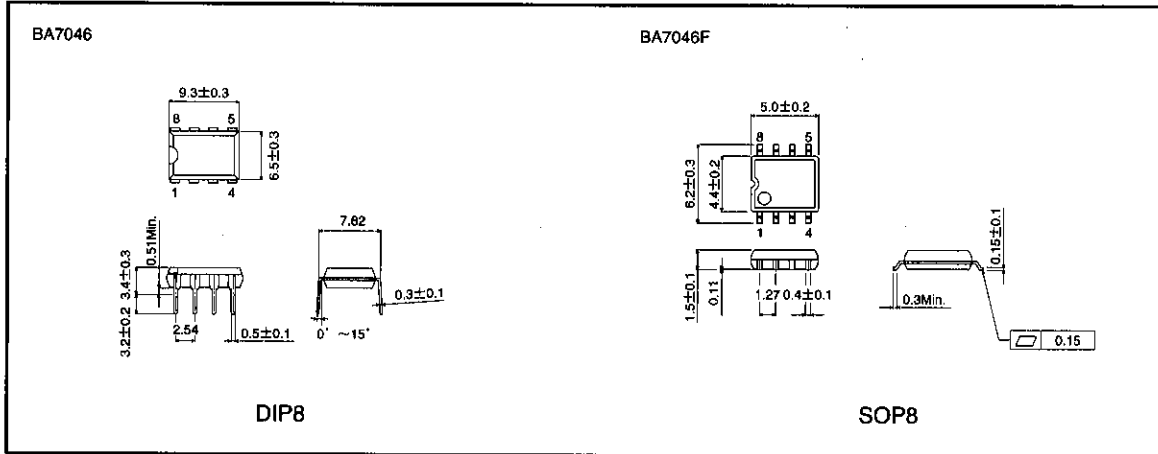
Fig. 21

1. Connect pin 1 to GND via a 120k Ω (approx.) resistor. Leave pins 2, 4 and 8 open.
2. SYNC output polarity (pin 3) is positive.
3. The delay time for rising edge of the SYNC output (pin 3) with respect to the falling edge of Sync for the Vsing input signal (pin 6) is 850ns (reference value).
4. The delay time for falling edge of the SYNC output (pin 3) with respect to the rising edge of Sync for the Vsing input signal (pin 6) is 450ns (reference value).

● External components

Resistor R₁ should have a tolerance of $\pm 2\%$, and a temperature coefficient of 100ppm or lower.

● External dimensions (Units: mm)



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