TOSHIBA

2003-2

PRODUCT GUIDE

BCE0012A

90nm (Ldrawn=70nm) CMOS ASIC TC300 Family

2003 semiconductor

http://www.semicon.toshiba.co.jp/eng

SoC Solution for a Wide Range of Ultra-High-Performance and Ultra-Low-Power Applications

TC300 Family

Featuring unparalleled CMOS performance, the Toshiba TC300 family can satisfy the demanding requirements of complex system-on-chip (SoC) designs. The TC300 family is ideally suited as an SoC platform for broadband infrastructure applications using xDSL, wireless and optical fiber technologies as well as high-performance and high-quality multimedia information systems.

While offering outstanding logic speed, the TC300 family also features ultra-low power consumption. The combination of high performance and low power broadens the capabilities of the TC300, enabling feature-rich mobile products with extended battery life.

The new CMOS4 process technology not only offers unprecedented embedded DRAM capability, but also permits easy mixing of analog and application-specific IP cores on the same chip. Each logic cell is available in three versions that operate at different threshold voltages; the optional multi-threshold process allows selective use of high-speed and low-power cells on and off critical paths.

The TC300 family capitalizes on copper technology, low-k dielectric and the industry's most aggressive 90-nm (70-nm-drawn gate) CMOS process. The process supports up to 11 levels of copper metal interconnect.

With the TC300 family, Toshiba offers a robust, state-of-the-art design environment geared to shorten the development time for large and complex SoC designs.

Toshiba's TC300 family offers an ideal solution for multimedia and high-speed networking applications, or any other application where both speed and low power consumption are important such as PDAs and portable devices.

Features and Benefits

Ultra-High Density and Ultra-Low Power

The TC300 family is fabricated using Toshiba's new CMOS4 process.

Design Rule

World-class 90-nm (70-nm-drawn gate) CMOS process

Copper Interconnect

Up to 11 levels of copper wiring combined with low-k dielectric

Improvements over the TC280 Family (L_{drawn} = 0.11 µm)

- **x2 improvement in logic density**
- **50% power savings per gate**
- **20% reduction in gate delay**

Cell Library

Primitive Cells

The TC300 family offers synthesis-friendly primitive cells for both high-performance- and low-power-intended chip designs. The multi-threshold process provides the ability to mix and match the cells of both high-speed and low-power libraries.

I/O Cells

The TC300 family offers I/O cells in two shapes: standard-height I/O cells for high-pin-count designs and low-height I/O cells for core-limited designs.

SRAMs

Performance- and density-optimized SRAMs

IP Cores

Toshiba supports an ever-growing selection of IP cores compliant with the VSI standard.

MPU	TX System RISC, ARM processors
Protocol Controllers	IEEE1394, USB, IrDA
High-Speed I/O	PCI, AGP, USB, LVDS, Direct RAC, HSTL
Multimedia	NTSC/PAL Video Encoder, JPEG, MPEG
Networking	Ethernet
Analog Functions	ADC, DAC, PLL
Memory	DRAM, SRAM, FIFO, ROM, EEPROM

DRAM Core Overview

The embedded DRAM cores based on Toshiba's leading trench capacitor technology provide many features, such as high memory bandwidth with a bus width selectable from 64, 128 and 256 bits, low power dissipation due to lower-capacitance connections and low switching noise on the data bus between memory and logic. The high-bandwidth SD-DRAM cores are upward compatible with those of the previous ASIC families. The fast-access FA-DRAM cores are being developed.

SD-DRAM with High Bandwidth

(Compliant with the synchronous DRAM standard)

Max. Clock Rate	300 MHz
Max. Data Rate	9.6 GB/s
I/O Bit Width	256 bits
Size	4 to 32 Mbits per macro

FA-DRAM with Fast Random Access Times

(High-density design for SRAM replacement)

Random Access Time	6 – 8 ns
I/O Bit Width	288 bits
Size	4 to 9 Mbits per macro

ARM is a registered trademark of ARM Limited in Europe and the U.S.

Design Methodology for SoC Designs

Production-proven tools and methodology ensure predictable results for SoC ASICs and reduce design time and iterations.

Hierarchical Design

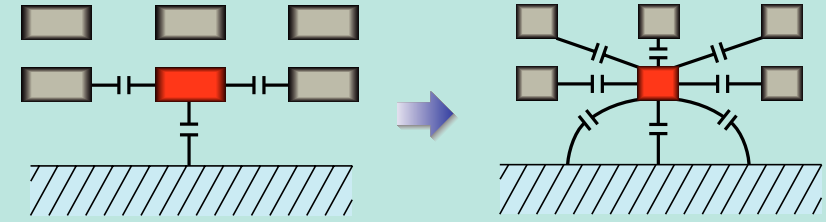
Toshiba provides support for hierarchical design approaches combined with a timing-driven design flow. This allows a design team to create sub-blocks in parallel and resolve timing problems at the block level.

Predictable Timing Closure

The advanced synthesis technique utilizes physical information to generate accurate wire models during RTL synthesis. This ensures a close correlation between pre-layout and post-layout delays. Accurate delay information is leveraged throughout the design flow, including design optimization (gate sizing), timing-driven routing and repeater insertion. The outcome is the ability to quickly achieve timing closure.

3D Capacitance Extraction

In today's deep-submicron ASICs, delays caused by interconnect are becoming increasingly dominant over gate delays. To accurately calculate deep-submicron delays, new techniques must be used. Toshiba employs 3D capacitance extraction to improve the accuracy of timing estimates for multi-layer metal processes.

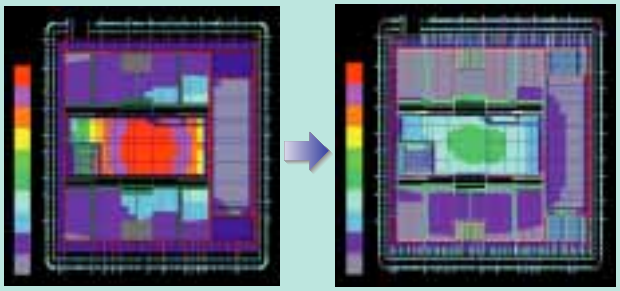


2D Extraction Considering Adjacent Wire Effects

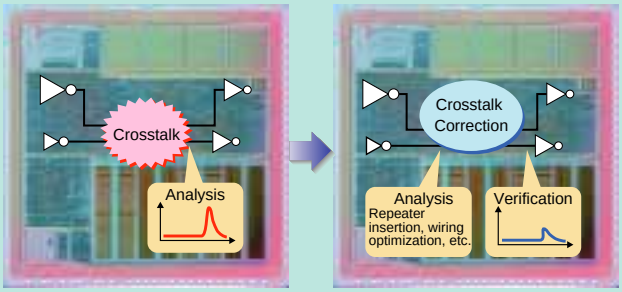
3D Extraction

Signal Integrity Analysis and Repair

To ensure signal integrity, Toshiba optimizes power grid routing, based on IR drop estimation, early in the design cycle. Additionally, electromigration, antenna effects, hot-carrier injection (HCI) and negative bias temperature instability (NBTI) are all considered. The TC300 design flow also embraces crosstalk analysis and elimination.



IR Drop Analysis and Power Grid Optimization



Crosstalk-Free Design

Packaging

Toshiba offers a complete range of packaging options, satisfying the requirements of advanced systems-on-chip (SoCs). For designs requiring high pin counts (600 to over 2000), Toshiba's flip-chip BGA packaging (PBGA[FC]) offers the highest I/O density and electrical performance available today. PFBGAs with 109 to 265 pins have a package body size no larger than 15 x 15 mm and are optimal for applications requiring minimal form factor. TBGAs and PBGAs with 256 to 868 pins are cost-effective solutions for mid-range I/O pin count requirements. In addition, Toshiba offers multi-layer PBGA[4L] packaging with excellent electrical performance for the 256 to 868 pin range.

Toshiba provides the electrical models for its packages to help you select an optimal one that satisfies your design specification.

General Product Specifications

Design Rule	90 nm (70-nm-drawn gate), CMOS process, 11-layer Cu
Power Supply	Core = 1.2 V; analog = 2.5 V; I/O: 2.5 / 3.3 V (1.8-V option)
Gate Delay (F/O=1, CIVX4 Gate)	14 ps (Low-Power Library), 11 ps (High-Speed Library), 9.5 ps (Very-High-Speed Library) * Three types of transistors are available with different threshold voltages.
Gate Density	403 kgates/mm^2 or more
Power Dissipation	7 nW/MHz/gate (CIVX1 gate)

OVERSEAS SUBSIDIARIES AND AFFILIATES

Toshiba America Electronic Components, Inc.

Headquarters-Irvine, CA
9775 Toledo Way, Irvine, CA 92618, U.S.A.
Tel: (949)455-2000 Fax: (949)859-3963

Boulder, CO (Denver)
3100 Araphahoe #500,
Boulder, CO 80303, U.S.A.
Tel: (303)442-3801 Fax: (303)442-7216

Wellington
PBM 337, #22, 11924 Forest Hill Blvd.,
Wellington, FL 33414, U.S.A.
Tel: (561)733-4949 Fax: (561)753-1489

Deerfield, IL (Chicago)
One Pkwy., North, #500, Deerfield,
IL 60015-2547, U.S.A.
Tel: (847)945-1500 Fax: (847)945-1044

Duluth, GA (Atlanta)
3700 Crestwood Pkwy, #160,
Duluth, GA 30096, U.S.A.
Tel: (770)931-3363 Fax: (770)931-7602

Edison, NJ
2035 Lincoln Hwy, #3000, Edison,
NJ 08817, U.S.A.
Tel: (732)248-8070 Fax: (732)248-8030

Beaverton/Portland, OR
1700 NW 167th Place, #240,
Beaverton, OR 97006, U.S.A.
Tel: (503)629-0818 Fax: (503)629-0827

Raleigh, NC
3120 Highwoods Blvd., #108, Raleigh,
NC 27604, U.S.A.
Tel: (919)859-2800 Fax: (919)859-2898

Richardson, TX (Dallas)
777 East Campbell Rd., #650, Richardson,
TX 75081, U.S.A.
Tel: (972)480-0470 Fax: (972)235-4114

San Jose Engineering Center, CA
1060 Rincon Circle, San Jose, CA 95131, U.S.A.
Tel: (408)526-2400 Fax:(408)526-8910

Wakefield, MA (Boston)
401 Edgewater Place, #360, Wakefield,
MA 01880-6229, U.S.A.
Tel: (781)224-0074 Fax: (781)224-1095

Toshiba do Brasil, S.A.

Electronics Component Div.
Estrada dos Alvarengas 5500,
São Bernardo do Campo, S.P. 09850-550, Brasil
Tel: (011)4358-7144 Fax: (011)4358-7179

Toshiba India Private Ltd.

6F DR. Gopal Das Bhawan 28, Barakhamba Road,
New Delhi, India
Tel: (011)331-8422 Fax: (011)371-4603

Toshiba Electronics Europe GmbH

Düsseldorf Head Office
Hansaallee 181, D-40549 Düsseldorf,
Germany
Tel: (0211)5296-0 Fax: (0211)5296-400

München Office
Büro München Hofmannstrasse 52,
D-81379, München, Germany
Tel: (089)748595-0 Fax: (089)748595-42

Toshiba Electronics France S.A.R.L.
Immeuble Robert Schuman 3 Rue de Rome
F-93561, Rosny-Sous-Bois, Cédex, France
Tel: (1)48-12-48-12 Fax: (1)48-94-51-15

Toshiba Electronics Italiana S.R.L.
Centro Direzionale Colleoni,
Palazzo Perseo 3,
I-20041 Agrate Brianza, (Milan), Italy
Tel: (039)68701 Fax: (039)6870205

Toshiba Electronics España, S.A.
Parque Empresarial, San Fernando, Edificio Europa,
1^{a} Planta, E-28831 Madrid, Spain
Tel: (91)660-6798 Fax:(91)660-6799

Toshiba Electronics (UK) Ltd.
Riverside Way, Camberley Surrey,
GU15 3YA, U.K.
Tel: (01276)69-4600 Fax: (01276)69-4800

Toshiba Electronics Scandinavia A.B.
Gustavslundsvägen 18, 5th Floor,
S-167 15 Bromma, Sweden
Tel: (08)704-0900 Fax: (08)80-8459

Toshiba Electronics Asia (Singapore) Pte. Ltd.

Singapore Head Office
438B Alexandra Road, #06-08/12 Alexandra
Technopark, Singapore 119968
Tel: (6278)5252 Fax: (6271)5155

Toshiba Electronics Service (Thailand) Co., Ltd.

135 Moo 5, Bangkadi Industrial Park, Tivanon Road,
Pathumthani, 12000, Thailand
Tel: (02)501-1635 Fax: (02)501-1638

Toshiba Electronics Trading (Malaysia)Sdn. Bhd.

Kuala Lumpur Head Office
Suite W1203, Wisma Consplant, No.2,
Jalan SS 16/4, Subang Jaya, 47500 Petaling Jaya,
Selangor Darul Ehsan, Malaysia
Tel: (03)5631-6311 Fax: (03)5631-6311

Penang Office
Suite 13-1, 13th Floor, Menara Penang Garden,
42-A, Jalan Sultan Ahmad Shah,
10050 Penang, Malaysia
Tel: (04)226-8523 Fax: (04)226-8515

Toshiba Electronics Philippines, Inc.

26th Floor, Citibank Tower, Valero Street, Makati,
Manila, Philippines
Tel: (02)750-5510 Fax: (02)750-5511

Toshiba Electronics Asia, Ltd.

Hong Kong Head Office
Level 11, Tower 2, Grand Century
Place, No.193, Prince Edward Road West,
Mongkok, Kowloon, Hong Kong
Tel: 2375-6111 Fax: 2375-0969

Beijing Office
Room 714, Beijing Fortune Building,
No.5 Dong San Huan Bei-Lu, Chao Yang District,
Beijing, 100004, China
Tel: (010)6590-8796 Fax: (010)6590-8791

Chengdu Office
Suite 403A, Holiday Inn Crown Plaza 31, Zongfu Street,
Chengdu, 610016, Sichuan, China
Tel: (028)8675-1773 Fax: (028)8675-1065

Shenzhen Office
Room 3010-3013, Office Tower Shun Hing Square,
Di Wang Commercial Centre, 5002 ShenNan
East Road, Shenzhen, 518008, China
Tel: (0755)246-3218 Fax: (0755)246-1581

Qingdao Office
Room B707, Full Hope Plaza,
12 Hong Kong Central Road, Qingdao,
Shandong, 266071, China
Tel: (0532)502-8105 Fax: (0532)502-8109

Toshiba Electronics Korea Corporation

Seoul Head Office
14F, KEC Building, 275-7 Yangjae-dong,
Seocho-ku, Seoul, 137-739, Korea
Tel: (02)589-4300 Fax: (02)589-4302

Gumi Office
6F, Goodmorning Securities Building,
56 Songjung-dong, Gumi-shi,
Kyeongbuk, 730-090, Korea
Tel: (054)456-7613 Fax: (054)456-7617

Toshiba Electronics (Shanghai) Co., Ltd.

23F, HSBC Tower, 101
Yin Cheng East Road, Pudong New Area, Shanghai,
200120, China
Tel: (021)6841-0666 Fax: (021)6841-5002

Tsurong Xiamen Xiangyu Trading Co., Ltd.

8N, Xiamen SEZ Bonded Goods Market Building,
Xiamen, Fujian, 361006, China
Tel: (0592)562-3798 Fax: (0592)562-3799

Toshiba Electronics Taiwan Corporation

Taipei Head Office
17F, Union Enterprise Plaza Building, 109
Min Sheng East Road, Section 3, Taipei,
105, Taiwan
Tel: (02)2514-9988 Fax: (02)2514-7892

Kaohsiung Office
16F-A, Chung-Cheng Building, 2, Chung-Cheng 3Road,
Kaohsiung, 800, Taiwan
Tel: (07)237-0826 Fax: (07)236-0046

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