2-wire serial sound control IC

BH3856S / BH3856FS

The BH3856S and BH3856FS are signal processing ICs designed for volume and tone control in televisions, mini component stereo systems, and other audio products. Their two-line serial control (I^2C-BUS) enables them to control volume and tone on the basis of signals from a microcomputer, etc.

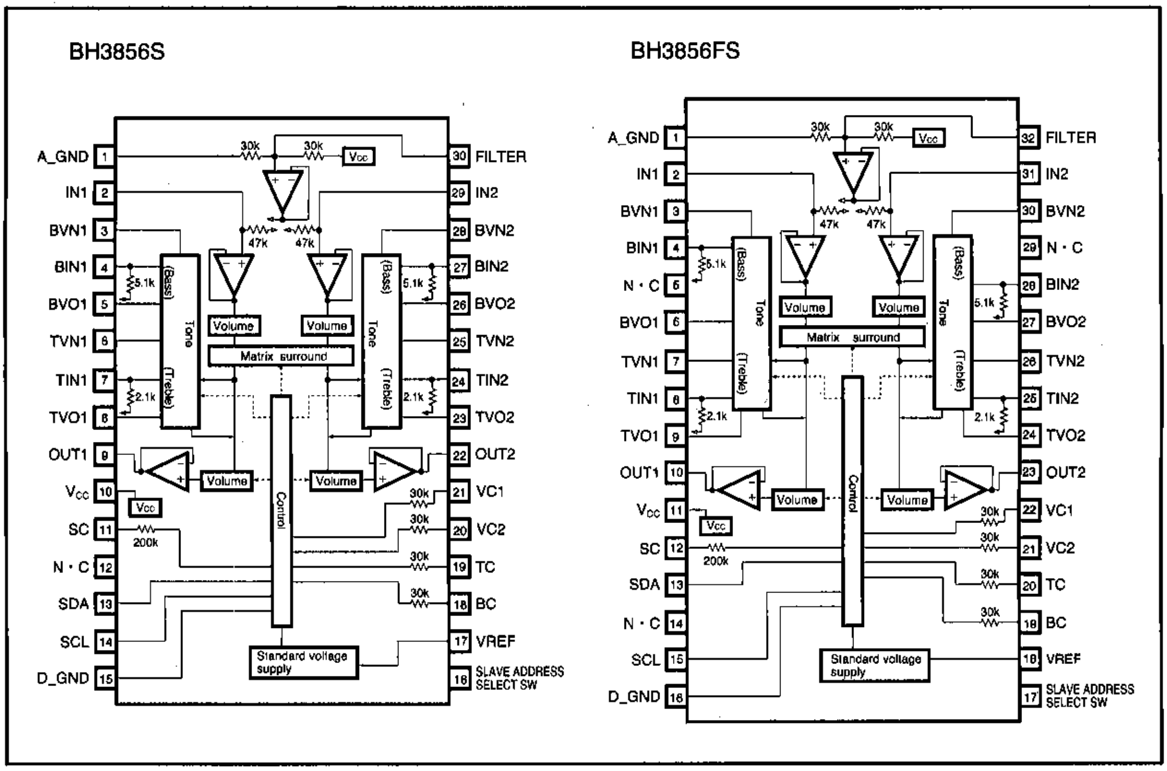
●Applications

Televisions, [VCRs] personal computer televisions, mini component stereo systems, car stereos

●Features

1) I^2C-BUS facilitates direct serial control from a microcomputer of volume (main volume), balance (left / right), and tone (bass, treble). DC control is also possible.
2) Volume is produced by a low-distortion, low-noise VCA. Designed to minimize step noise.
3) Stable standard voltage supply and built-in I / O buffer mean that few attachments are needed. SSOP32 package designed to save space.
4) Matrix surround yields powerful sound.

●Block diagram



●Absolute maximum ratings (Ta = 25℃)

Parameter		Symbol	Limits	Unit
Supply voltage		Vcc	10.0	V
Power dissipation	BH3856S	Pd	1200 *1	mW
	BH3856FS		850 *2	
Operating temperature		Topr	−40~+85	℃
Storage temperature		Tstg	−55~+150	℃

*1 Reduced by 12 mW for each increase in Ta of 1℃ over 25℃.
*2 Reduced by 6.8 mW for each increase in Ta of 1℃ over 25℃.

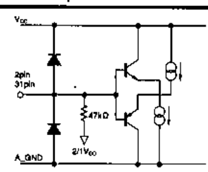
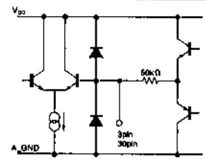
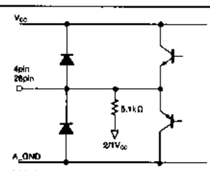
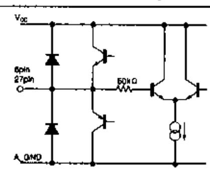
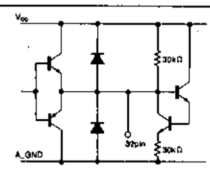
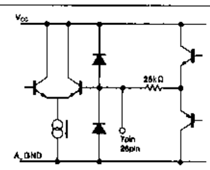
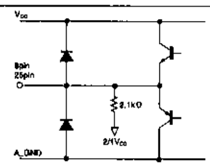
●Recommended operating conditions (Ta = 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	6.0	9	9.5	V

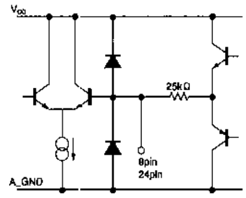
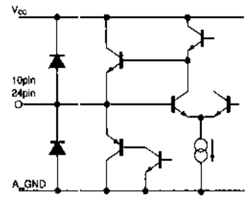
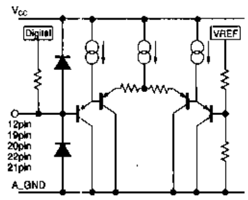
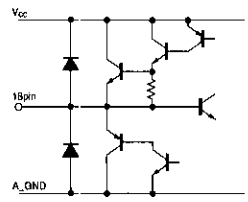
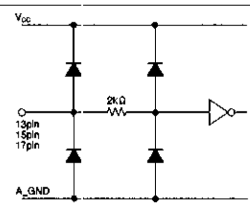
●Pin description

Pin No.		Symbol	Description
BH3856S	BH3856FS		
1	1	A_GND	Analog system ground
2	2	IN1	Pin for ch 1 volume input
3	3	BVN1	Pin for connection to ch 1 low-band filter
4	4	BIN1	Pin for connection to ch 1 low-band filter
5	6	BVO1	Pin for connection to ch 1 low-band filter
6	7	TVN1	Pin for connection to ch 1 high-band filter
7	8	TIN1	Pin for connection to ch 1 high-band filter
8	9	TVO1	Pin for connection to ch 1 high-band filter
9	10	OUT1	Pin for ch 1 volume output
10	11	Vcc	Power supply pin
11	12	SC	Time constant pin for prevention of switching shock
13	13	SDA	SDA data input pin
14	15	SCL	SCL data input pin
15	16	D_GND	Digital system ground
16	17	SASS	Slave address selection pin
17	18	VREF	Standard voltage output pin
18	19	BC	Time constant pin for prevention of switching shock
19	20	TC	Time constant pin for prevention of switching shock
20	21	VC2	Time constant pin for prevention of switching shock
21	22	VC1	Time constant pin for prevention of switching shock
22	23	OUT2	Pin for ch 2 volume output
23	24	TVO2	Pin for connection to ch 2 high-band filter
24	25	TIN2	Pin for connection to ch 2 high-band filter
25	26	TVN2	Pin for connection to ch 2 high-band filter
26	27	BVO2	Pin for connection to ch 2 low-band filter
27	29	BIN2	Pin for connection to ch 2 low-band filter
28	30	BVN2	Pin for connection to ch 2 low-band filter
29	31	IN2	Pin for ch 2 volume input
30	32	FILTER	Filter pin
12	5,14,28	NC	Not connected internally.

●Input / output circuit

Symbol	Pin Voltage	Equivalent circuit	Description
IN1 IN2	4.5V 4.5V		Main volume input pin. Designed for input impedance of 47 kΩ Typ).
BVN1 BVN2	4.5V 4.5V		Pin for low band filter connection.
BIN1 BIN2	4.5V 4.5V		Pin for low band filter connection.
BVO1 BVO1	4.5V 4.5V		Pin for low band filter connection.
FILTER	5.2V		Filter input pin. Please install a capacitor of about 10 μF to the filter pin. Has built-in precharge and discharge circuits.
TVN1 TVN2	4.5V 4.5V		Pin for high band filter connection.
TIN1 TIN2	4.5V 4.5V		Pin for high band filter connection.

※The pin numbers are for the BH3856S.

Symbol	Pin Voltage	Equivalent Circuit	Description
TVO1 TVO2	4.5V 4.5V		Pin for high band filter connection.
OUT1 OUT2	4.5V 4.5V		Main volume output pin. OUT1 is the volume output for CH1. OUT2 is the volume output for CH2.
SC BC TC VC1 VC2			For prevention of shock noise during step switching. SC: Surround pin BC: Bass pin TC: Treble pin VC1: Volume pin (CH1) VC2: Volume pin (CH2)
VREF	3.8V		3.8V regulator output pin. Output requires capacitor for stopping oscillation. Output pin has built-in precharge and discharge circuits, so there is no problem with start-up or shut-down even with a large capacitor. This pin is for connection to the high-band filter.
SDA SCL SASS			• I²C bass input pin SDA: serial data line SCL: serial clock line • Slave address selection pin SASS: slave address selection switch
VCC		Power supply voltage pin.	
A_GND		Analog GND pin. Connected to IC board.	
D_GND		Digital GND pin. Separate from Analog GND pin.	

∗The pin numbers are for the BH3856S.

●Electrical characteristics (Unless otherwise specified, Ta = 25℃, V_{CC} = 9V, f = 1kHz, BW = 20 ~ 20kHz, VOL = Max., TONE = ALL FLAT, R_g = 600Ω, R_L = 10kΩ)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	−	20	27	mA	No signal
Max. input	Vim	2.3	2.5	−	Vrms	THD=1%, VOL=−20dB (ATT)
Max. output	Vom	2.3	2.5	−	Vrms	THD=1%
Voltage gain	Gv	−1.5	0	+1.5	dB	Vin=1Vrms
Max. attenuation	ATT	90	110	−	dB	Vo=1Vrms
Cross talk	V_{CT}	70	80	−	dB	Vo=1Vrms
Low-band control width	VB Max.	+12	+15	+18	dB	100Hz, Vin=100mVrms
	VB Min.	−18	−15	−12	dB	100Hz, Vin=100mVrms
High-band control width	VT Max.	+12	+15	+18	dB	100kHz, Vin=100mVrms
	VT Min.	−18	−15	−12	dB	100kHz, Vin=100mVrms
Matrix surround single-channel gain	G_{SR}	4	6	8	dB	Vo=1Vrms *
Total Harmonic distortion	THD	−	0.01	0.1	%	Vo=0.5Vrms, BPF=400Hz~30kHz
Output noise voltage	$V_{NO}1$	−	45	65	μVrms	No signal, VOL=MAX, Rg=0 *
Residual output noise voltage	VM_{NO}	−	2	10	μVrms	No signal, VOL=−∞, Rg=0 *
Standard power supply output voltage	V_{REF}	3.5	3.8	4.1	V	I_{REF}=3mA
Standard power supply output current capability	I_{REF}	3.0	10	−	mA	V_{REF}>3.7V
Channel balance	G_{CB}	−1.5	0	+1.5	dB	CH1 taken as the standard for measurements.
Input impedance	R_{IN}	33	47	61	kΩ	f=1kHz
Output impedance	R_{OUT}	−	−	10	Ω	f=1kHz
Ripple rejection	RR	40	−	−	dB	f=100Hz, V_{RR}=1Vrms
Input voltage H	V_{IH}	4	−	−	V	SCL, SDA
Input voltage L	V_{IL}	−	−	1	V	SCL, SDA

Items marked with an asterisk (*) were measured with the VP-9690A (displays mean detection and effective value), produced by Matsushita Communication Industrial.
◎ Not designed for radiation resistance.
◎ Signal input occurs in equiphase.

●Measurement circuit

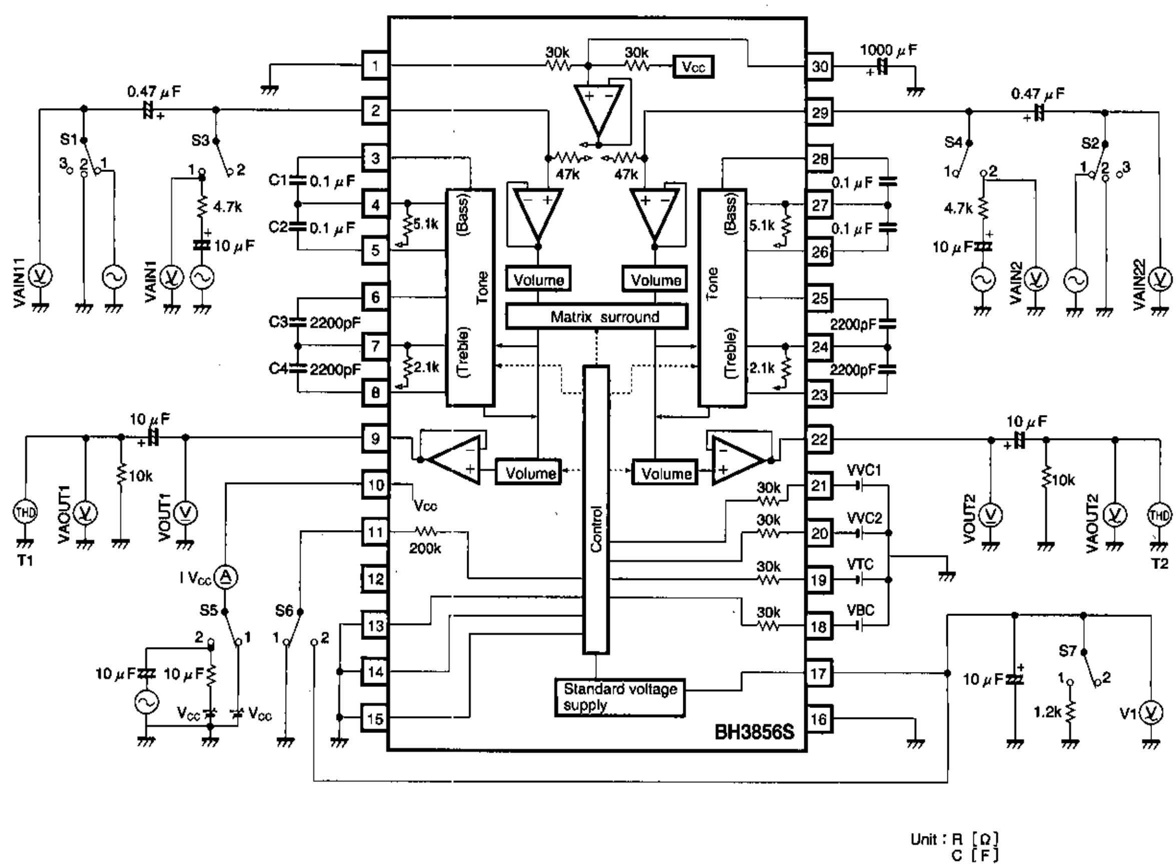


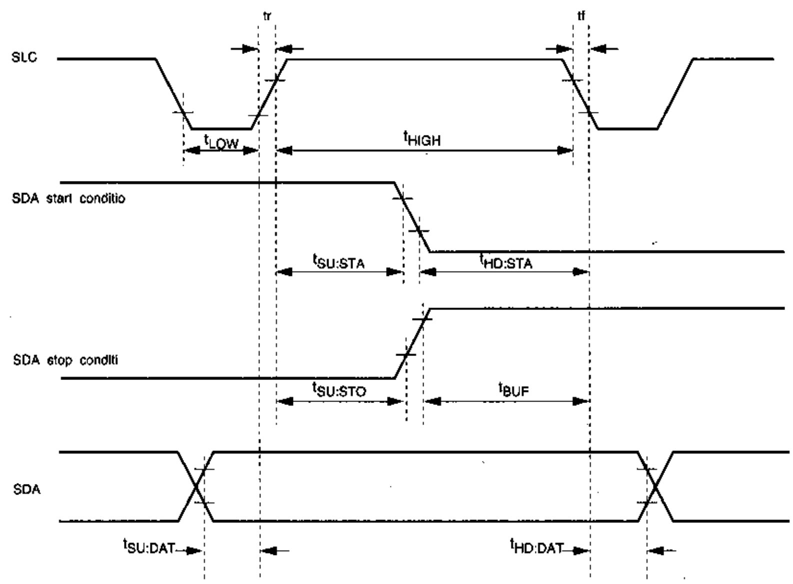
Fig. 1

Note: Diagram depicts the BH3856S.

●Performing data settings

(1) I^2C BUS timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	100	kHz
SCL clock hold time, HIGH state	t_{HIGH}	4	—	—	μs
SCL clock hold time, LOW state	t_{LOW}	4.7	—	—	μs
SDA and SDL signal start-up time	tr	—	—	1	μs
SDA and SDL signal shut-down time	tf	—	—	0.3	μs
Set-up time for re-send [start] conditions	t_{SU};STA	4.7	—	—	μs
Hold time (re-send) [start] conditions (After hold time ends, initial clock pulse is generated.)	t_{HD};STA	4	—	—	μs
Set time for [stop] conditions.	t_{SU};STO	4.7	—	—	μs
Bus free time between [stop] condition and [start] condition	t_{BUF}	4.7	—	—	μs
Data set-up time	t_{SU};DAT	250	—	—	ns



t_{SU};STA=start code set-up time.
t_{HD};STA=start code hold time.
t_{SU};STO=stop code set-up time.
t_{BUF}=bus free time.
t_{SU};DAT=data set-up time.
t_{HD};DAT=data hold time.

I^2C-BUS timing rules

(2) I²C BUS data format

S	Slave address	A	Select address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

- S = start condition (start bit recognition)
- Slave address = IC recognition. Upper 7 bits are random. Bottom bit is "L" for the sake of overwrite.
- A = acknowledge bit (recognition of acknowledgment)
- Select address = selection between volume, bass, treble, and matrix surround
- Data = volume and tone data
- P = stop condition (stop bit recognition)

(3) BH3856S/BH3856FS slave addresses

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	A	0

- Slave address selection
  ①A = 1 (10000010) [SASS pin HI]
  ②A = 0 (10000000) [SASS pin LOW]

(4) Interface protocol

1) Basic protocol

S	Slave address	A	Select address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

2) Auto increment (Select address increases (+1) by the value of the data.)

S	Slave address	A	Select address	A	Data 1, data 2,...data N	A	P
	MSB LSB		MSB LSB		MSB LSB		

(Examples) ①The address data specified by select address is taken as data 1.
②The address data specified by select address +1 is taken as data 2.
③The address data specified by select address +N is taken as data N.

3) Structure with which transmission is not possible (In this case, only select address 1 is set.)

S	Slave address	A	Select address 1	A	Data	A	Select address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

Note: Following transmission of data, data transmitted as select address 2 will not be recognized as select address 2, but as data.

(5) Specification of select address and data

Function	Select address (MSB)							(LSB)	Data (MSB) D7	D6	D5	D4	D3	D2	D1	(LSB) D0
⓪ Volume CH1 (L)	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
① Volume CH2 (R)	0	0	0	0	0	0	0	1	VR7	VR6	VR5	VR4	VR3	VR2	VR1	VR0
② Bass	0	0	0	0	0	0	1	0	0	0	BA5	BA4	BA3	BA2	BA1	BA0
③Treble	0	0	0	0	0	0	1	1	0	0	TR5	TR4	TR3	TR2	TR1	TR0
④ Surround	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	SR0

- The auto increment function cycles the select address in the manner shown in Figure A.

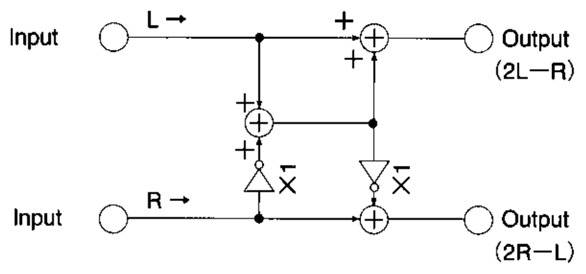
  (Figure A) ⓪ → ① → ②
  ↑ ↓
  ④ ← ← ← ③

- The cycle commences from the initially specified select address.

(6) Surround data

Function	Data (MSB) D7	D6	D5	D4	D3	D2	D1	(LSB) D0
Matrix surround OFF	0	0	0	0	0	0	0	0
Matrix surround ON	0	0	0	0	0	0	0	1

(7) Matrix surround



(8) Volume attenuation (reference values)

ATT (dB)	DATA (HEX)	ATT (dB)	DATA (HEX)	ATT (dB)	DATA (HEX)
0	FF	−19	85	−56	42
−1	E4	−20	82	−58	3F
−2	D8	−22	7C	−60	3C
−3	CF	−24	78	−62	39
−4	C8	−26	74	−64	36
−5	C2	−28	70	−66	34
−6	BD	−30	6D	−68	32
−7	B8	−32	6A	−70	2F
−8	B2	−34	68	−72	2D
−9	AD	−36	65	−74	2A
−10	A9	−38	61	−76	28
−11	A5	−40	5C	−78	26
−12	A0	−42	59	−80	24
−13	9C	−44	55	−82	22
−14	98	−46	52	−84	20
−15	94	−48	4E	−86	1E
−16	90	−50	4B	−90	1A
−17	8C	−52	48	−100	13
−18	89	−54	45	−112	00

Note: All figures in this table are reference values. When using this IC, check this table carefully and perform the appropriate setting.

(9) Bass/Treble gain settings (reference values)

ATT (dB)	DATA (HEX)	ATT (dB)	DATA (HEX)
15	3F	0	1F
14	38	−1	1C
13	35	−2	1B
12	33	−3	19
11	31	−4	18
10	2F	−5	17
9	2E	−6	16
8	2D	−7	15
7	2C	−8	13
6	2B	−9	12
5	2A	−10	11
4	29	−11	0F
3	27	−12	0D
2	26	−13	0B
1	25	−14	08
0	1F	−15	05

Notes: (1) The gain values in the treble and bass data setting tables above are based on the assumption that the filter constants have been set so that maximum and minimum gain are equal to the peak and bottom values listed in the frequency characteristics drawings.

(2) All figures in this table are reference values. When using this IC, check this table carefully and perform the appropriate setting.

●Application example

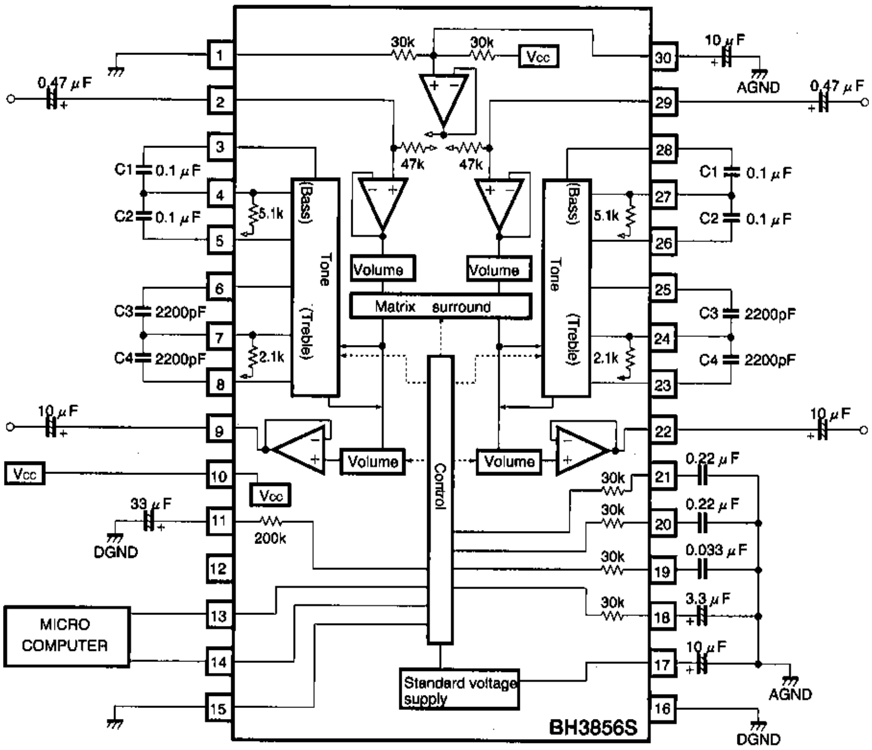


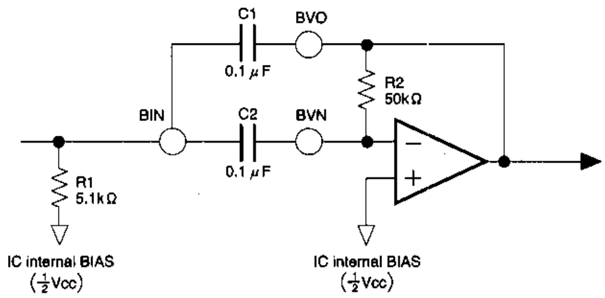
Fig. 2

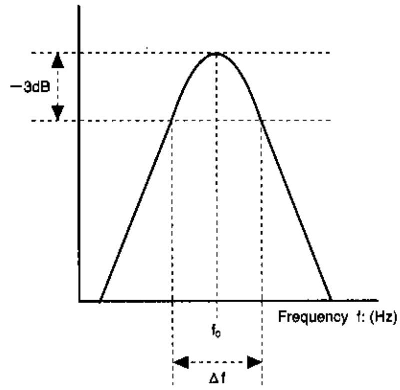
Note: Diagram depicts the BH3856S.

●Operation notes

1. Operating power supply voltage range
   As long as the operating power supply voltage and ambient temperature are kept within the specified range, the basic circuits are guaranteed to function, but be sure to check the constants as well as the element settings, voltage settings, and temperature settings.

2. Bass filter





- B.P.F. composed of multiple feedback active f_0 can be varied according to the value of C. (theoretical equation)

$$f_0 = \frac{1}{2\pi} \times \left(\frac{1}{R_1 R_2 C_1 C_2} \right)^{\frac{1}{2}}$$

$$Q \fallingdotseq \left[\left(\frac{R_1}{R_2 C_1 C_2} \right)^{\frac{1}{2}} \times (C_1 + C_2) \right]^{-1}$$

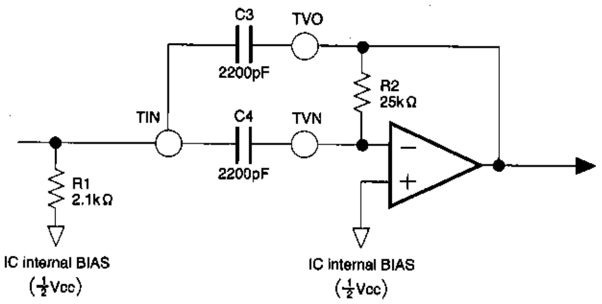
Note: Filter gain is calculated using the equation on the left. Total output gain is the sum of the gain for each of the internal circuits.

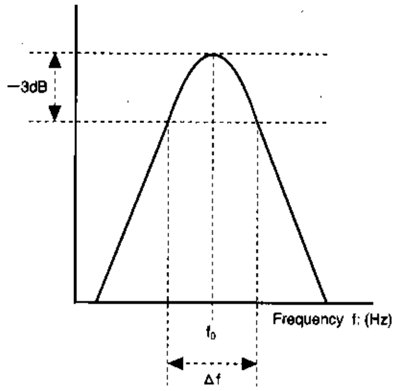
$$G = \frac{R_2}{5k\Omega} \times \left(1 + \frac{C_1}{C_2} \right)^{-1}$$

(When $R_1 = 5.1k\Omega$, $R_2 = 50k\Omega$, $C_1 = C_2 = C$)

$$f_0 = \frac{1.0 \times 10^{-5}}{C} \qquad Q \fallingdotseq 1.57 \qquad G = 5.0$$

3. About the treble filter





・The band-pass filter is constructed using a multiple-feedback active filter.
f_0 can be varied by changing the value of the capacitors.
(Theoretical formulas)

$$f_0 = \frac{1}{2\pi} \times \left(\frac{1}{R_1R_2C_3C_4}\right)^{\frac{1}{2}} \qquad Q \fallingdotseq \left(\left(\frac{R_1}{R_2C_3C_4}\right)^{\frac{1}{2}} \times (C_3+C_4)\right)^{-1}$$

Note: The filter gain is given by the formula on the left, but the total output gain is determined by the this in combination with the internal circuit.

$$G = \frac{R_2}{5k\Omega} \times \left(1+\frac{C_3}{C_4}\right)^{-1}$$

(When $R_1 = 2.1k\Omega$, $R_2 = 25k\Omega$, $C_3 = C_4 = C$)

$$f_0 = \frac{2.2\times10^{-5}}{C} \qquad Q \fallingdotseq 1.73 \quad G=2.5$$

4. I^2CBUS control

High-frequency digital signals are input on the SCL and SDA terminals, so ensure that the wiring and PCB pattern is designed in such a way as to ensure that these signals do not interfere with the analog signal system.

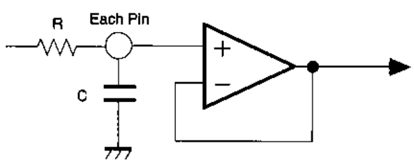
If you are not using I^2CBUS control (i.e. you are using DC control), connect the SCL, SDA and SASS terminals to GND (do not leave them disconnected).

5. Step switching noise

The VC1, VC2, TC, BC and SC terminals have components connected to them the application example circuit. The values of these components may need to be changed depending on the signal level setting and PCB pattern.

Investigate carefully before deciding on the values of the various circuit constants.

The equivalent circuit for these terminals is given below (an integrator circuit is set at the first stage to slow the variation).

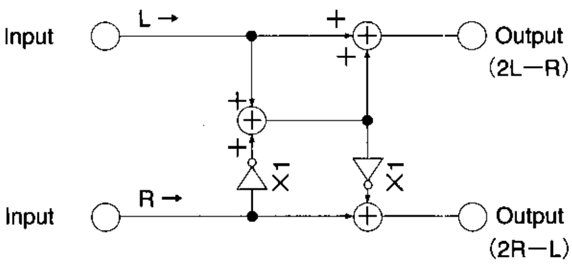


	R value (kΩ)
VC1, VC2, BC, TC	30
SC	200

6. Volume and tone level settings
This specification sheet gives reference values for the amount of attenuation and gain with respect to the serial control data. The internal D / A convertor is an R-2R circuit, and data exists for the places where continuous variation does not occur between data. Use this when fine setting is required. The setting limits are up to 8 bits for volume (256 steps) and 6 bits (64 steps) for tone.

7. Digital / analog separation
The digital and analog power supplies and grounds for this IC (BH3856) are completely separate. The digital circuits are supplied from a stable reference source that is on the chip (VREF (3.8V)). For this reason, there is no need to worry about timing shifts, or interference due to digital noise.

8. Matrix surround



◎The matrix surround circuit construction is as shown in the diagram above. The gain is obtained from the formulas in the diagram.

Phase Gain	OdB
Negative Phase Gain	6dB

(However, reverse-phase gain is for input to one Ch only)

9. DC control
An internal impedance of 30kΩ is seen from the VC1, VC2, TC, and BC terminals, and 200kΩ is seen from the SC (pin 11) terminal, so with regard to DC control, we recommend direct control with the voltage source. When using variable volume, take the impedance into consideration when making the setting.
Note: The DC control voltage range is 0V to VREF.
Do not apply voltages above VREF to the terminals.

10. GND
- As shown in the application example circuit, connect the external component GND to the analog GND.
- However, the GND for the capacitor connected to the VREF term inal should be connected to the digital GND.
- If a capacitor with goof high-frequency characteristics is connected in parallel with the capacitor connected to VREF, the performance of the circuit with respect to static noise will improve (we recommend a ceramic capacitor of between 0.001 μF and 0.1 μF)
- When using long digital and analog ground lines, take care to ensure that there is no potential difference between the two ground lines.

● Electrical characteristic curves

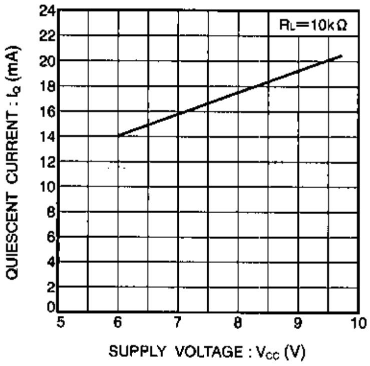


Fig. 3 Quiescent curve - Supply voltage characteristics

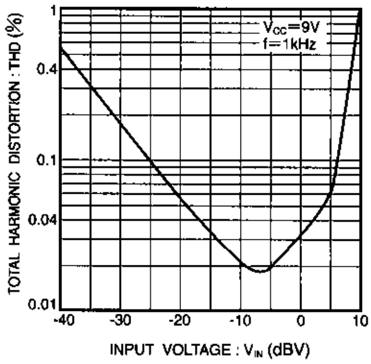


Fig.4 Total harmonic distortion - Input voltage characteristics

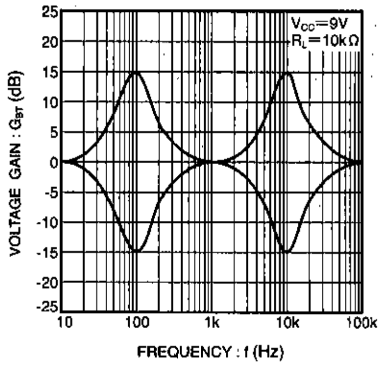


Fig. 5 Output gain - Frequency

● External dimensions (Unit: mm)

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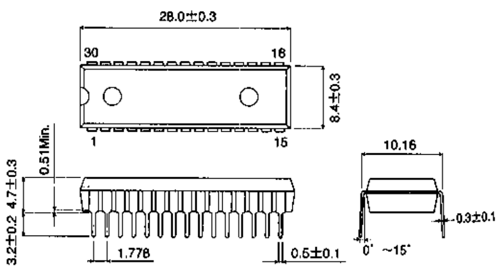

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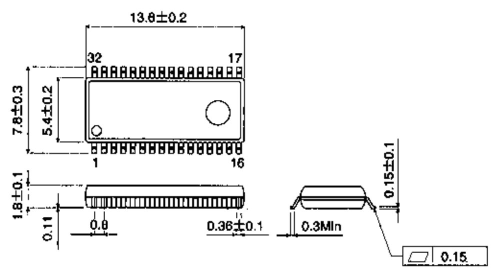

SSOP-A32

Sound control

Audio accessory components

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