Read/Write Amplifier for FDD

BH6627FS

The BH6627FS is a 4-mode read/write IC designed for floppy disk drives. This IC has an internal active filter that can be set to any of multiple settings according to transfer rate, and internal switches for density and inner edge/outer edge. Write current can be set to any of multiple settings.

●Applications

Floppy disk drives (1MB, 1.6MB and 2MB drives)

●Features

1) Internal active filter with four settings that can be selected for multiple Q and f_0.
2) Time domain filter with internal switch set according to transfer rate.
3) Any of multiple write current settings can be selected, and inner track/outer track switching is done internally.

●Absolute maximum ratings (Ta=25℃)

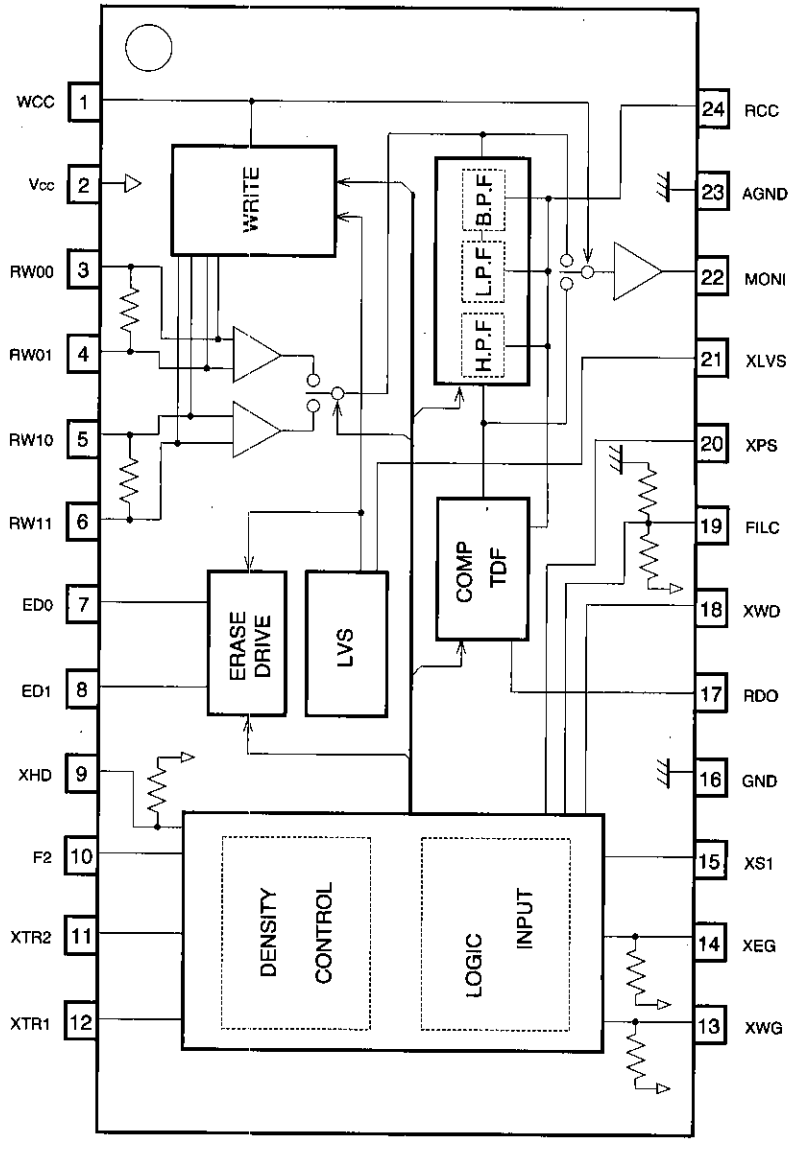
Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	+7	V
Operating temperature	T_{OPR}	0~+70	℃
Storage temperature	T_{STG}	−55~+125	℃
Digital input voltage	VI	−0.5~V_{CC}+0.3	V
RW pin voltage	VRW	+15	V
LVS output voltage	VLVS	V_{CC}+0.3	V
ED pin voltage	VER	V_{CC}+0.3	V
Power dissipation	P_D	650*	mW

* When using at temperatures of Ta=25℃ or higher, reduce power by 6.5 mW for each 1℃ above 25℃.

●Recommended operating conditions

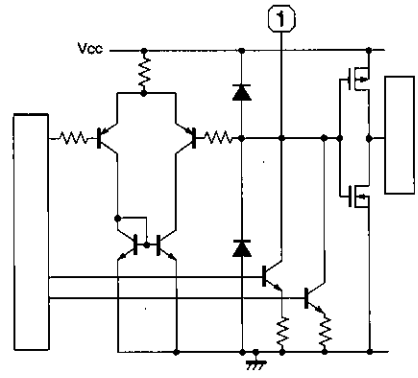
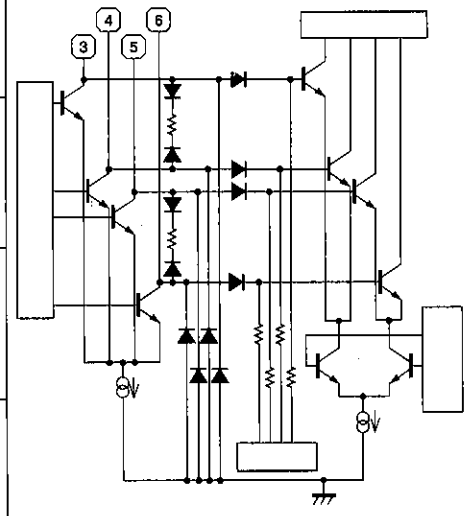
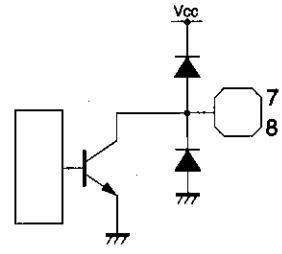
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V

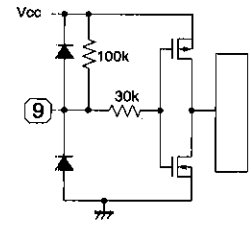
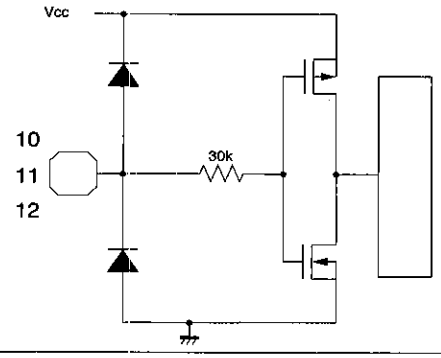
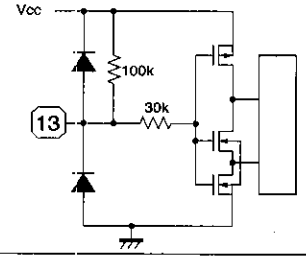
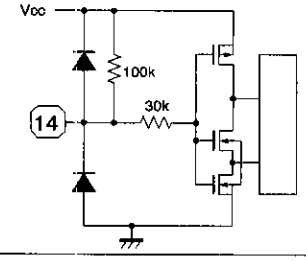
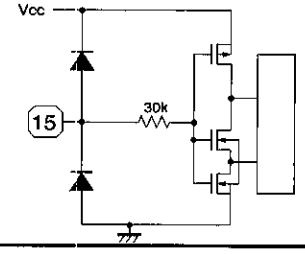
●Block diagram

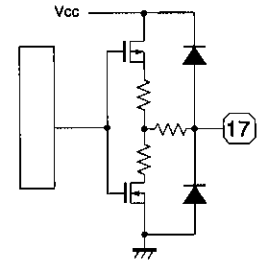
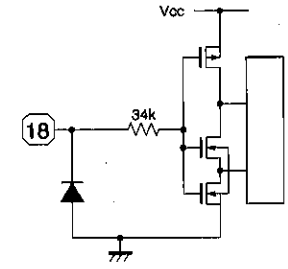
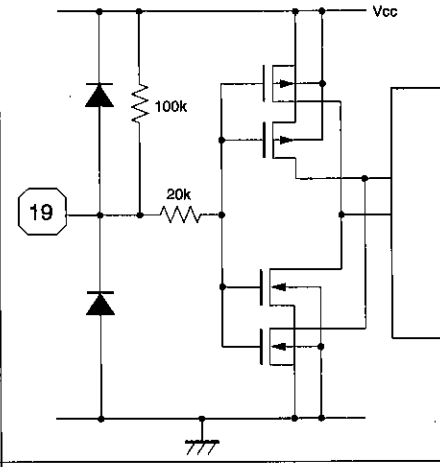
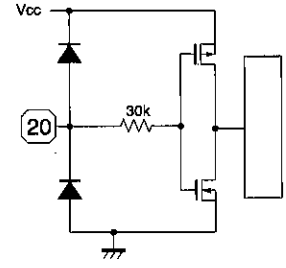


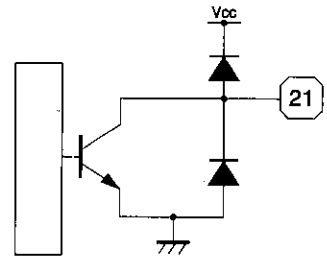
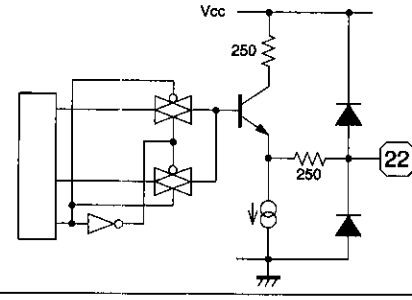
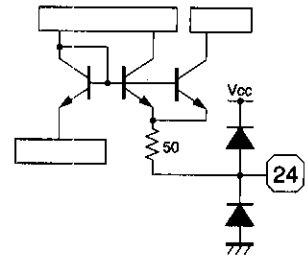
(Note) The Vcc fret pattern must be short, and the impedance between Vcc and GND must be lowered by inserting a pass conductor.

●Pin descriptions

Pin No.	Name	Equivalent circuit	Function
1	WCC		For connecting the write current adjustment resistor Connect the write current adjustment resistor between this pin and Vcc. Setting this pin to the low level during reading switches MONI to differentiator output.
2	Vcc		Power supply pin
3	RW00		Active when SIDE0 and the read/write head connecting pin (pin 15, XS1) is at the high level (side 0) Starts at RW00 during the start of writing (from reading to writing)
4	RW01		
5	RW10		Active when the read/write head connecting pin (pin 15, XS1) is at the low level (side 1) Starts at RW10 during the start of writing (from reading to writing)
6	RW11		
7	ED0		Side 0 erase current sink
8	ED1		Side 1 erase current sink

Pin No.	Name	Equivalent circuit	Function
9	XHD		1 MB/2 MB selector High = 1 MB Low = 2 MB
10	F2		1.6 MB drive selector Selector signal high level = active High = 1.6 MB drive, low = 2 MB drive
11	XTR2		Inner track/outer track position setting Controls the write current
12	XTR1 (XSWF)		Inner track/outer track position setting Controls the filter and write current
13	XWG		Write enable gate (Schmidt input) Low = active
14	XEG		Erase enable gate (Schmidt input) Low = active
15	XS1		Head/side switching signal Low = active (Schmidt input) High = side 0, low = side 1

Pin No.	Name	Equivalent circuit	Function
16	DGND		Digital ground
17	RDO		Read data output TTL high level = active
18	XWD		Write data input Operates at falling edge (Schmidt input)
19	FILC		Filter control (f0, Q) Used to switch filter cutoff frequency (tri-state input)
20	XPS		Power save selector Low = active

Pin No.	Name	Equivalent circuit	Function
21	XLVS		External low level - voltage detection pin Open collector output when low level voltage is detected. Switches to low level when Vcc drops below the specified voltage
22	MONI		Preamplifier output and differentiator output monitoring Monitor is switched with pin 1 (WCC)
23	AGND		Analog ground
24	RCC		Filter (LPF, BPF) cutoff frequency and TDF 1st M/M pulse width setting resistor connection

●Electrical characteristics (unless otherwise noted, Ta=25℃, Vcc=5V)

Current consumption

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Current consumptioin,Standby	ICCST	—	165	400	μA	*1
Current consumptioin,Read	ICCR	—	28	42	mA	*1
Current consumptioin,Write	ICCW	—	8.5	15	mA	*2

*1 RRCC=2.0 [kΩ] (XHD=H)
*2 RWCC=2.4 [kΩ] * (2 MB inner track, XTR2=H time, except IWR and IER)

Low level voltage detection circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Threshold voltage	VTH+	—	3.95	4.2	V	When power supply voltage rises
	VTH−	3.5	3.75	4.0	V	When power supply voltage falls
Hysteresis voltage	VH	50	—	—	mV	
Output voltage, low level	VOL	—	—	0.40	V	Vcc=2.5[V] IOL=0.2[mA]
Output leakage current	IOH	—	—	10	μA	

Recovery time

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
POWER·SAVE→READ	TR2	—	—	500	μs	by XPS
READ→ERASE	TR3	—	—	6	μs	by XEG
READ→WRITE	TR4	—	—	4	μs	by XWG
WRITE→READ	TR5E	—	—	20	μs	by XEG
	TR5W	—	—	160	μs	by XWG
SIDE0↔SIDE1	TR6	—	—	40	μs	by XS1
1MB↔2MB	TR7	—	—	40	μs	by XHD
1.6 MB ↔2 MB	TR8	—	—	40	μs	by F2
Inner↔outer track	TR9	—	—	40	μs	by XTR1
Write current switch	TR10	—	—	40	μs	by XTR2

Preamplifier

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Voltage gain (1)	GVD1	43	46	49	dB	f=125[kHz], VIN=2.5[mVp-p] (XTR1=L) (differential)
Voltage gain (2)	GVD2	46	49	52	dB	f=125[kHz], VIN=2.5[mVp-p] (XTR1=H) (differential)
SIDE0↔SIDE1 cross talk	GCTLK	50	—	—	dB	f=125[kHz], VIN=100[mVp-p] (differential) *3
Differential input resistance	RID	—	8	—	kΩ	
Input conversion noise voltage	VN	—	2.5	3.7	μVrms	f=500[Hz]~1[MHz]
Input sink current	ISINK	—	180	—	μA	
Differential input voltage amplitude tolerance (1)	VIN1	—	—	5.0	mVp-p	Distortion factor 5% (with sine wave input) (XTR1=L)
Differential input voltage amplitude tolerance (2)	VIN2	—	—	3.5	mVp-p	Distortion factor 5% (with sine wave input) (XTR1=H)
Common mode rejection ratio	CMRR	50	—	—	dB	f=125[kHz], VIN=100[mVp-p] *3
Power supply rejection ratio	PSRR	40	—	—	dB	f=250[kHz], VIN=100[mVp-p] *3

Preamplifier- L.P.F. - differentiator (B.P.F.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Filter - time constant accuracy	EFIL	−10	—	+10	%	*3
Preamplifier - L.P.F. - Differentiator total gain (1)	GVDD1	40.5	44.5	48.5	dB	f=250[kHz], VIN=2.5[mVp-p] (differential) (2MB setting XTR1 = L, FILC = H)
Preamplifier - L.P.F. - Differentiator total gain (2)	GVDD2	43.5	47.5	51.5	dB	f=250[kHz], VIN=2.5[mVp-p] (differential) (2MB setting XTR1 = H, FILC = H)
Differentiator output peaking Frequency setting range	f_0	0.1	—	0.5	MHz	Defined by set-up Typ. value

*3 RRCC=2.0 [kΩ] (XHD=L, XTR1=H, F2=L, FILC=H)

Comparator and waveform shaping

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
TDF M/M pulse width accuracy(1)	TDF1	−10	—	+10	%	XHD=H, F2=L (Typ. : 2120[ns]) f=62.5[kHz]~125[kHz] *4
TDF M/M pulse width accuracy(2)	TDF2	−10	—	+10	%	XHD=H, F2=H (Typ. : 1800[ns]) f=62.5[kHz]~125[kHz] *4
TDF M/M pulse width accuracy(3)	TDF3	−10	—	+10	%	XHD=L, F2=H/L (Typ. : 1140[ns]) f=125 [kHz]~250 [kHz] *4
RD pulse width	TRD	270	400	530	ns	Judgment level 1.5[V]
Rise time	TTLH	—	—	70	ns	Rise time for 0.4 [V] - 2.0 [V]
Fall time	TTHL	—	—	70	ns	Fall time for 2.0 [V] - 0.4 [V]
Peak shift	P. S.	—	—	1.0	%	f=250[kHz] , VIN=1[mVp-p] (differential)
Output "L" level voltage	VOL	—	—	0.4	V	IOL=0.2[mA]
Output "H" level voltage	VOH	2.7	—	—	V	IOH=−15[μA] *5

*4 RRCC=2.0 [kΩ]
*5 Rise level from 0.4 [V] to 70 [ns]

Write circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Write current adjustment range	IWR	2.0	—	20	mA0-p	
Write current accuracy	ACIW	−7.0	—	+7.0	%	*6
Write current pairability	△IWR	−1.0	—	+1.0	%	RWCC=2.4 [kΩ]
Write current supply voltage depedency	PSIW	−4.0	−0.8	+3.0	%/V	RWCC=2.4 [kΩ]
Output saturation voltage	VSATRW	—	0.4	1.0	V	IWR=12[mA]
Off-state leakage current	ILKRW1	—	—	20	μA	Unselected side
	ILKRW2	—	—	50	μA	Selected side
Minimum write date pulse width	TWD	70	—	—	ns	
Write current inner/outer track ratio accuracy	ACIWTR	+/-10 x (1-setting ratio)			%	*7

*6 RWCC=1.2 [kΩ], each of XTR1, XTR2 can be set by the user.
*7 Setting ratio errors based on XTR1=L, XTR2=L

Erase output

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Erase current setting range	IER	—	—	40	mA	
Output saturation voltage	VSATER	—	0.2	0.6	V	IER=40[mA]
Output leakage current	IOH	—	—	10	μA	Off time, ED0=ED1=Vcc

Logic input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
"H" Input voltage	VIH	2.0	—	—	V	Except for FILC
"L" Input voltage	VIL	—	—	0.8	V	Except for FILC
Input voltage hysteresis	VH	0.15	—	—	V	Applicable to XWD, XWG, XEG and XS1
"L" Input current	IIL1	—	50	100	μA	Vcc=5[V] VIL=GND Applicable to XWG, XEG, XHD, FILC
"H" Input voltage 2	VIH2	4.2	—	—	V	Applicable to FILC
"L" Input voltage 2	VIL2	—	—	0.8	V	Applicable to FILC

●Read characteristics

Density				1MB				1.6MB		2MB	
Transfer route			FILC	250[kbps]		300[kbps]		500[kbps]		500[kbps]	
Input	Mode	XHD	NO CARE	HI		HI		LOW		LOW	
		F2	NO CARE	LOW		HI		HI		LOW	
	Track	XTR1 (XSWF)	NO CARE	Outer track LOW	Inner track HI	Outer track LOW	Inner track HI	Outer track LOW	Inner track HI	Outer track LOW	Inner track HI
	Filter	f_0 [kHz] (Characteristics) *1	HI	150	158	178	185	323	404	366	358(C)
			LOW	↑	↑	↑	↑	300	366	338	361(B)
	TDF	[nSEC]	NO CARE	2120		1800		1140		1140	

(Note) *1 (B) Chebyshev's characteristics (However, RRCC=2.0 [kΩ]
(C) Except for the high ripple Chebyshev's characteristics, 2MB inner track, all are Butterworth characteristics. Refer to filter characteristics.

Total filter peak frequency settingouter edge

$f_0 = a / (RRCC\ [k\Omega] + 0.09)$ [kHz]

FILC	"H"	"L"	
a =	313	313	250 [kbps] outer track
	330	330	250 [kbps] inner track
	376	376	300 [kbps] outer track
	387	387	300 [kbps] inner track
	675	627	500 [kbps] outer track (when F2 = H)
	844	765	500 [kbps] inner track (when F2 = H)
	765	706	500 [kbps] outer track (when F2 = L)
	748	754	500 [kbps] inner track (when F2 = L)

TDF time constant setting

250 [kbps] : $T = 758 \times RRCC\ [k\Omega] + 604$ [ns]
500 [kbps] : $T = 683 \times RRCC\ [k\Omega] + 434$ [ns]
500 [kbps] : $T = 333 \times RRCC\ [k\Omega] + 388$ [ns]

●Write current switching ratio

Track		Outer track ⟵ ⟶ Inner track			
	XTR1	L		H	
	XTR2	L	H	L	H
Density 2MB		0.383	0.350	0.333	0.300
Density 1.6MB		0.450	0.417	0.383	0.350
Density 1MB (250kbps)		0.933	0.900	0.800	0.733
Density 1MB (300kbps)		0.933	0.900	0.800	0.733

Write current setting

$$Iwr = \frac{24.0}{RWCC\ [k\Omega]}\ [mA]$$

●Filter characteristic

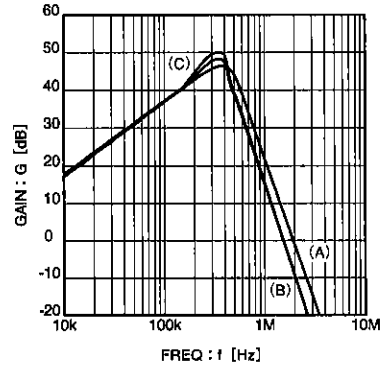
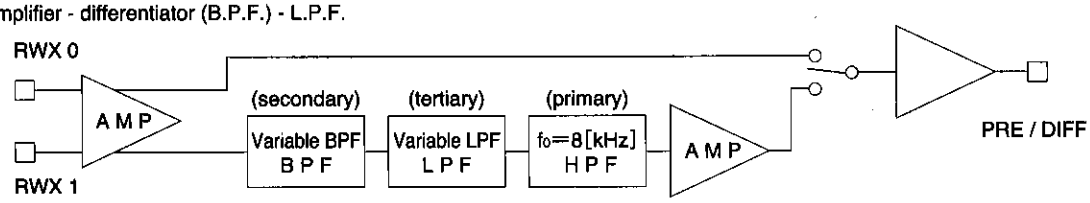
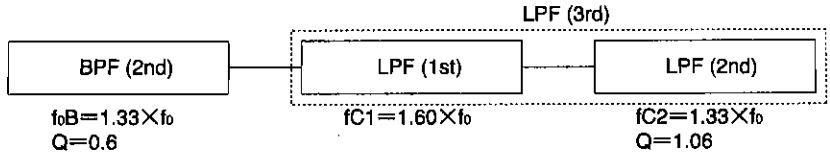


Fig. 1 PRE IN vs. DIFF OUT characteristics

Preamplifier - differentiator (B.P.F.) - L.P.F.

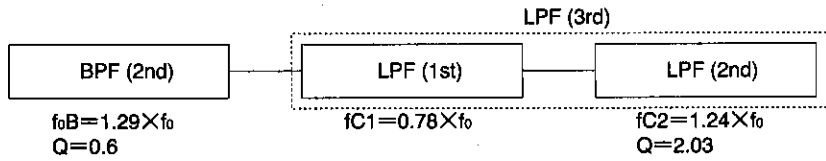


(A) [1M/1.6M/2M outer track] total characteristics peak frequency fo



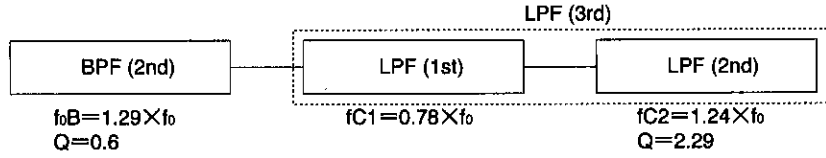
: Butterworth setting

(B) FILC="L" time [2M inner track] total characteristics peak frequency fo



: Chebyshev's setting

(C) FILC="H" time [2M inner track] total characteristics peak frequency fo



: High ripple chebyshev's setting

●Measurement circuit

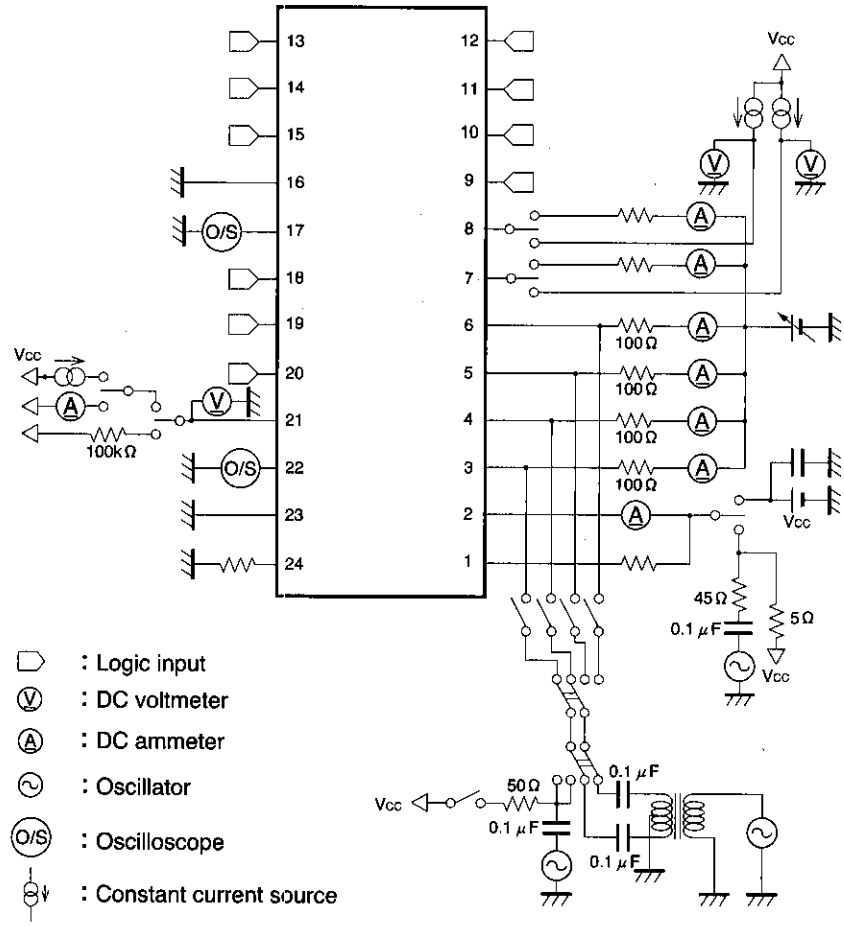


Fig. 2

●Circuit operation

(1) Read

The input signal from the head coils from each side of the disc is amplified by the preamplifier and then differentiated. The filter time constant can be set externally. After differentiation, the differential output is input to the comparator. The time domain filter detects zero cross, and the output is converted to read data. The monostable multivibrator width can be set externally, while the read data pulse width is a constant 400ns.

(2) Write

Input write data are converted to toggle movements by the internal flip-flops, operating the write driver. The write driver current is supplied by the write current generator, but the externally set current can be controlled according to density and by selecting inner track/outer track.

(3) Erase

An open collector output pin is used, and the erase current is set with a resistor between it and the head.

(4) Power supply

When the low level voltage detector detects a drop in the supply voltage, writing and erasing are prohibited.

●Operation notes

(1) Use a short pattern for V_{CC}, and a sufficiently wide AGND and DGND. Keep the impedance between V_{CC} and GND low by inserting a bypass capacitor.

(2) Use a pattern that will minimize interference between digital signals and the head.

●Electrical characteristic curves

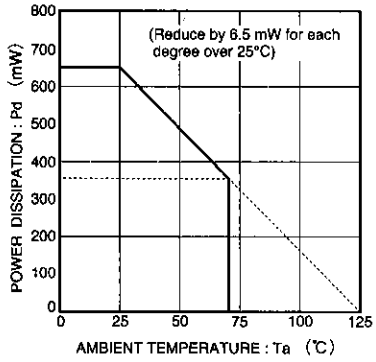


Fig. 3 Thermal derating characteristics

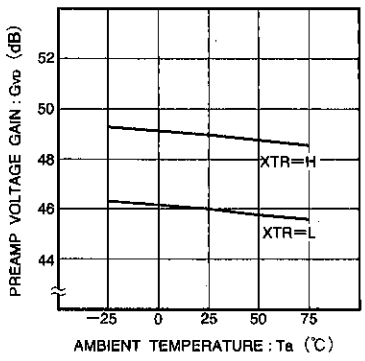


Fig. 4 Preamp voltage gain vs. ambient temperature

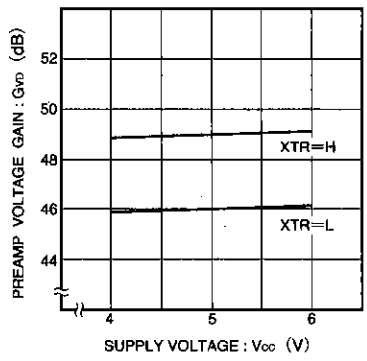


Fig. 5 Preamp voltage gain vs. supply voltage

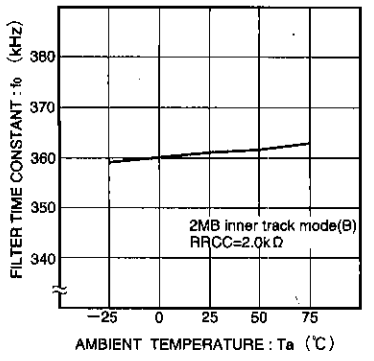


Fig. 6 Filter time constant (f_0) vs. ambient temperature

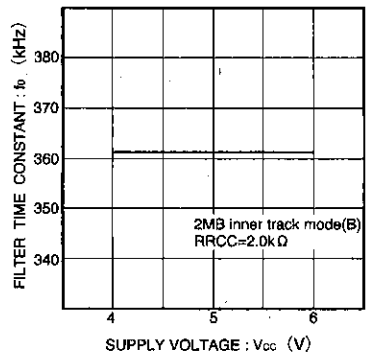


Fig. 7 Filter time constant (f_0) vs. supply voltage

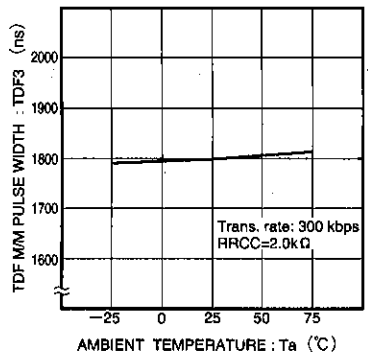


Fig. 8 TDF time constant vs. ambient temperature

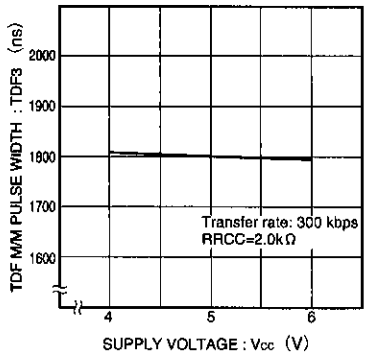


Fig. 9 TDF time constant vs. supply voltage

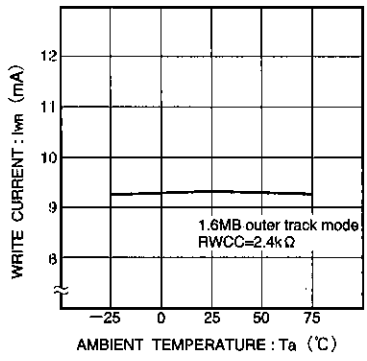


Fig. 10 Write current vs. ambient temperature

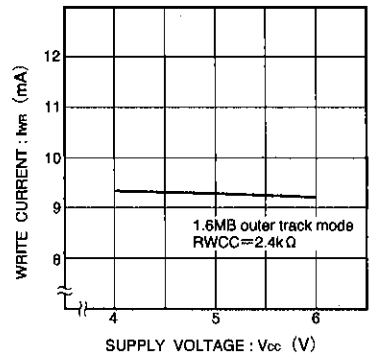


Fig. 11 Write current vs. power supply voltage

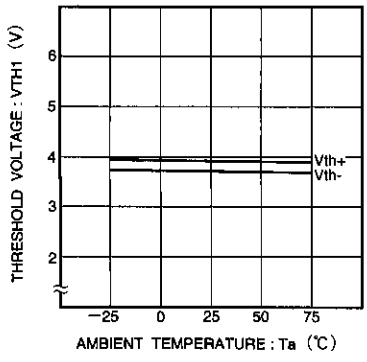


Fig. 12 Low level detection voltage vs. ambient temperature

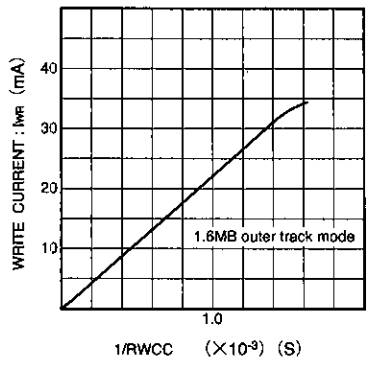
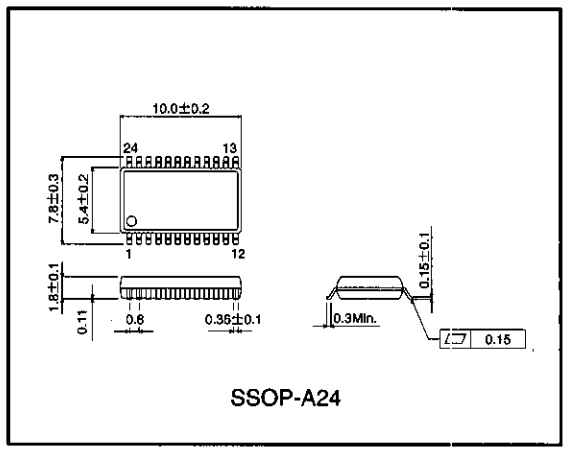


Fig. 13 Write current vs. write current adjustment resistance

●External dimensions (Units: mm)



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