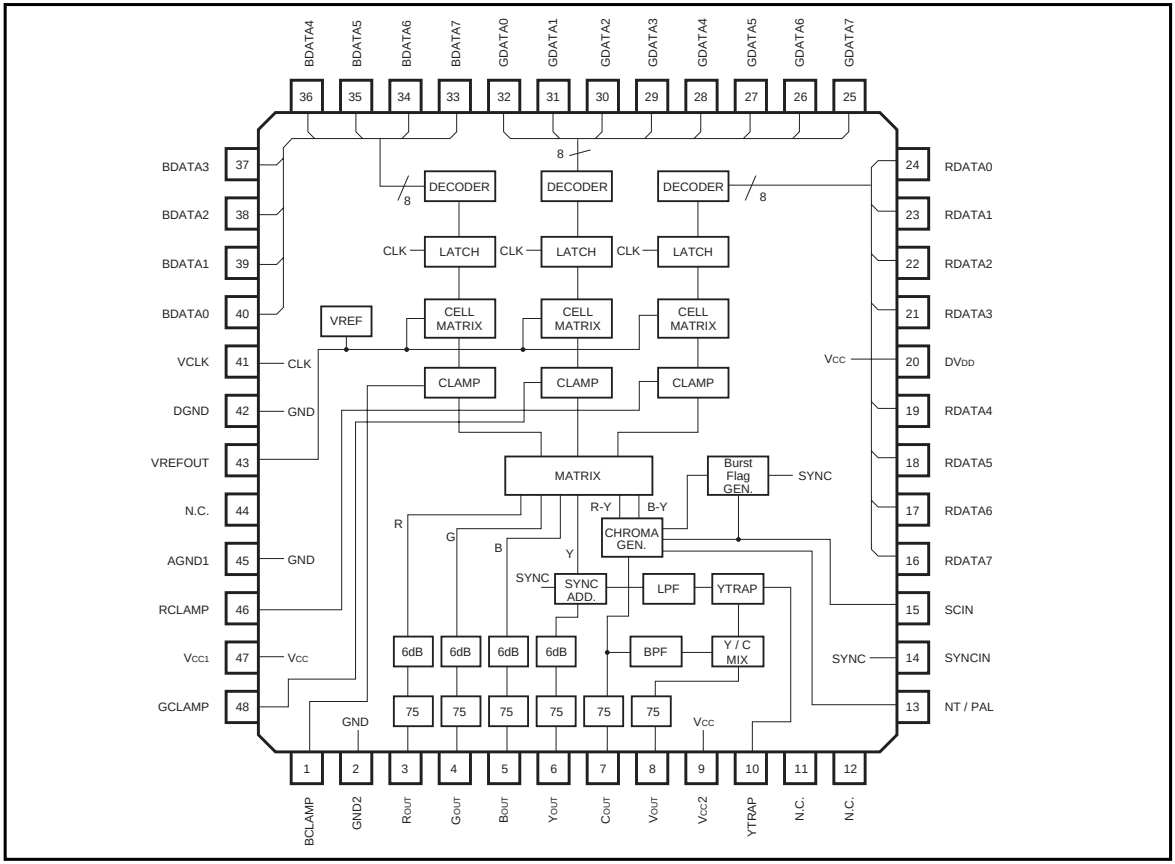
Color TV signal encoder
BH7240AKV

The BH7240AKV is an IC that converts digital RGB signals (8-bit) to NTSC and PAL color TV signals. In addition to composite output, luminance output, chrominance output, and analog RGB output are available. Each type of output is equipped with an internal 75Ω driver.

●Applications
TV peripheral devices

●Features
1) Supports both NTSC and PAL.
2) Internal RGB3-channel DAC (internal regulator).
3) Internal burst timing generator circuit.
4) Y / C separation output pin.
5) Analog RGB signal output pin.
3) Internal 75Ω driver.

●Block diagram



●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	DV_{DD}, $AV_{CC}1$ $AV_{CC}2$	7*1	V
Power dissipation	Pd	900*2	mW
Operating temperature	Topr	– 20 ~ + 70	°C
Storage temperature	Tstg	– 55 ~ + 125	°C

*1 At Ta = 25°C
*2 Reduced by 9.0mW for each increase in Ta of 1°C over 25°C.
(When mounted on a 70mm × 70mm × 1.6mm glass epoxy board.)

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	DV_{DD}, $AV_{CC}1$ $AV_{CC}2$	4.50 ~ 5.50	V

●Recommended input conditions (at DV_{DD} = $AV_{CC}1$ = $AV_{CC}2$ = 5.0V)

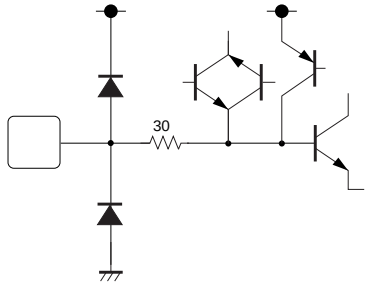
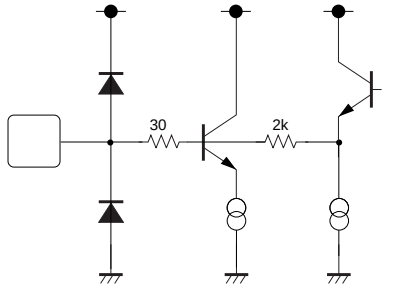
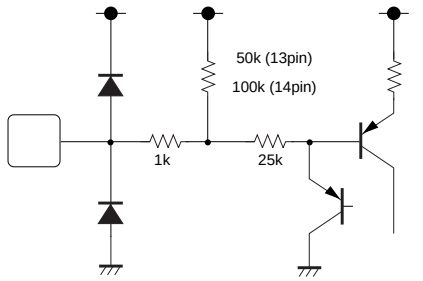
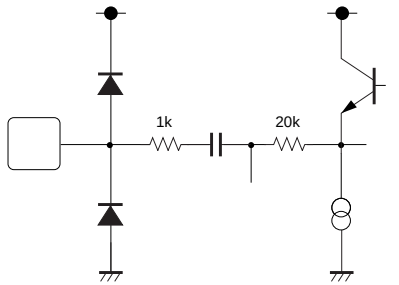
Parameter	Symbol	Limits	Unit
VCLK, RGBDATA input high level	VTH	2.2 ~ 5.0	V
VCLK, RGBDATA input low level	VTL	GND ~ 0.8	V
SYNCIN, NT / PAL input high level	VTH	2.2 ~ 5.0	V
SYNCIN, NT / PAL input low level	VTL	GND ~ 0.8	V

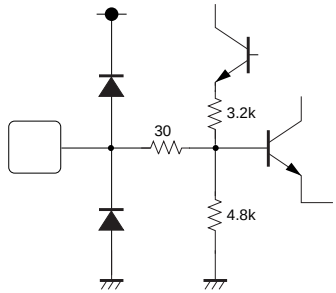
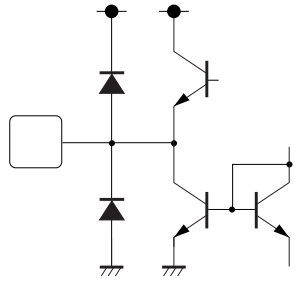
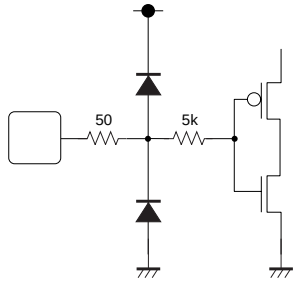
●Pin descriptions

Pin No.	Pin name	Function
1	BCLAMP	Analog blue signal clamping pin
2	AGND2	GND pin for 75Ω driver
3	R_{OUT}	Analog red signal output. Internal 75Ω driver
4	G_{OUT}	Analog green signal output. Internal 75Ω driver
5	B_{OUT}	Analog blue output. Internal 75Ω driver
6	Y_{OUT}	Luminance signal output. Internal 75Ω driver
7	C_{OUT}	Chrominance signal output. Internal 75Ω driver
8	V_{OUT}	Composite video signal output. Internal 75Ω driver
9	$AV_{CC}2$	Power supply pin for 75Ω driver
10	YTRAP	Luminance trap filter connection pin. Connecting a trap filter eliminates the chrominance band component included in the luminance signal, and reduces the amount of chrominance color. Output impedance is approximately 2kΩ. This is effective only for composite video output.
11	N.C.	This pin is not connected within the IC.
12	N.C.	This pin is not connected within the IC.
13	NT / PAL	Video output method selector pin. NTSC when HIGH, PAL when LOW
14	SYNCIN	Composite SYNC input. For LOW input, SYNC is output to YOUT and VOUT. At the same time, DC clamping of the RGB signal takes place.
15	SCIN	Color subcarrier input. Sine waves of a frequency corresponding to the required output method, or pulse waves with a duty of 50%, should be input in a range not exceeding V_{CC}-GND.
16	RDATA7	Red data input pin (bit 7)
17	RDATA6	Red data input pin (bit 6)
18	RDATA5	Red data input pin (bit 5)
19	RDATA4	Red data input pin (bit 4)
20	DV_{DD}	Power supply pin for digital circuit
21	RDATA3	Red data input pin (bit 3)
22	RDATA2	Red data input pin (bit 2)
23	RDATA1	Red data input pin (bit 1)
24	RDATA0	Red data input pin (bit 0)
25	GDATA7	Green data input pin (bit 7)
26	GDATA6	Green data input pin (bit 6)
27	GDATA5	Green data input pin (bit 5)
28	GDATA4	Green data input pin (bit 4)
29	GDATA3	Green data input pin (bit 3)
30	GDATA2	Green data input pin (bit 2)
31	GDATA1	Green data input pin (bit 1)
32	GDATA0	Green data input pin (bit 0)
33	BDATA7	Blue data input pin (bit 7)
34	BDATA6	Blue data input pin (bit 6)
35	BDATA5	Blue data input pin (bit 5)
36	BDATA4	Blue data input pin (bit 4)
37	BDATA3	Blue data input pin (bit 3)
38	BDATA2	Blue data input pin (bit 2)
39	BDATA1	Blue data input pin (bit 1)

Pin No.	Pin name	Function
40	BDATA0	Blue data input pin (bit 0)
41	VCLK	System clock input. RGB data is taken into the IC at the timing of this clock.
42	DGND	GND pin for digital circuit
43	VREFOUT	RGB DAC reference voltage output pin. A 0.1μF capacitor should be connected between the GND pins.
44	N.C.	This pin is not connected internally in the IC.
45	AGND1	GND pin for analog circuits (other than 75Ω driver)
46	RCLAMP	Analog red signal clamping pin
47	$V_{CC}1$	Power supply pin for analog circuits (other than 75Ω driver)
48	GCLAMP	Analog green signal clamping pin

●Pin equivalent circuits

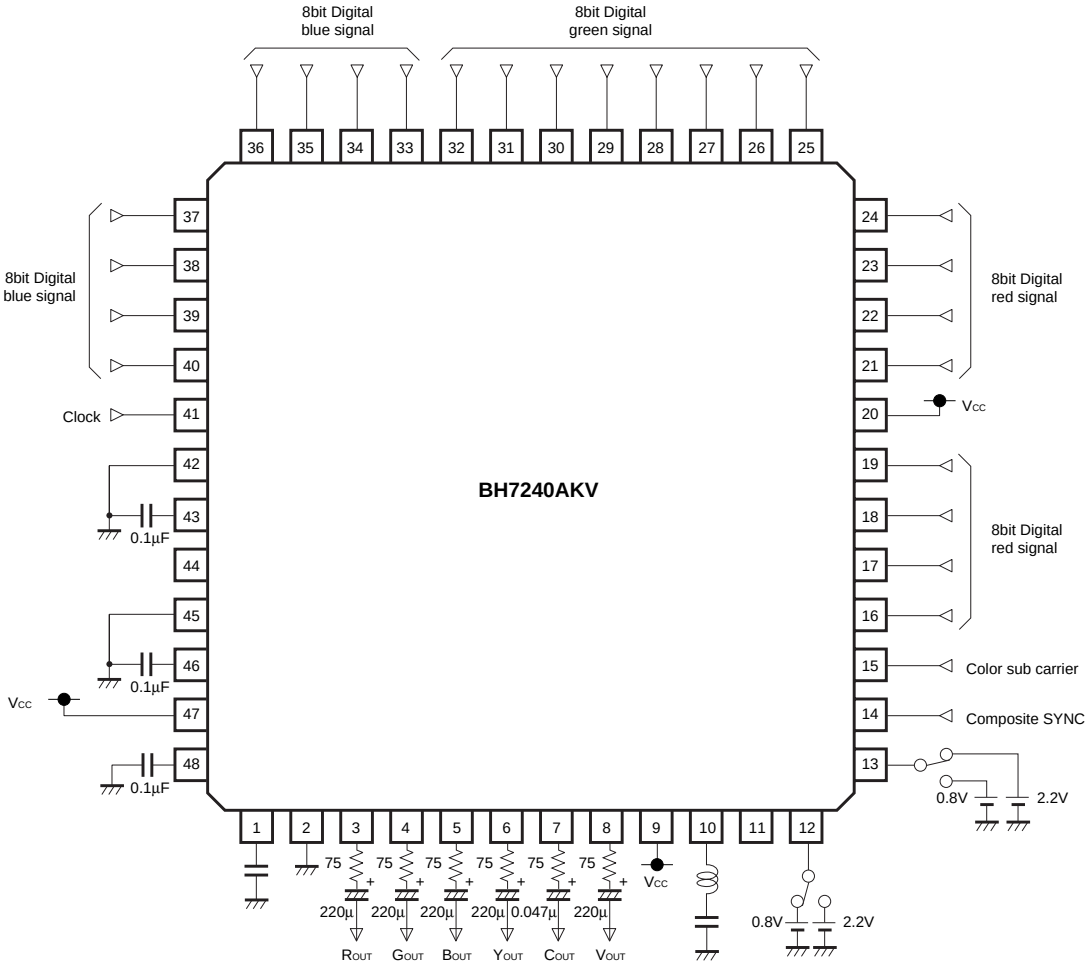
Pin No.	Pin name	Equivalent circuit
1 46 48	BCLAMP RCLAMP GCLAMP	
10	YTRAP	
13 14	NT / RAL SYNCIN	
15	SCIN	

Pin No.	Pin name	Equivalent circuit
43	VREFOUT	
3 4 5 6 7 8	ROUT GOUT BOUT YOUT COUT VOUT	
16 ~ 19 21 ~ 24 25 ~ 32 33 ~ 40 41	RDATA7 ~ 4 RDATA3 ~ 0 GDATA7 ~ 0 BDATA7 ~ 0 VCLK	

●Electrical characteristics (unless otherwise noted, Ta = 25°C, DV_{DD} = $AV_{CC}1$ = $AV_{CC}2$ = 5.0V)

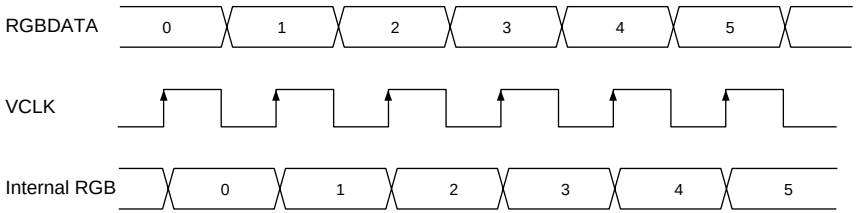
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Current consumption	ICC	—	85	105	mA	RGBDATA = 00 input
⟨Luminance level⟩ (V_{OUT}, Y_{OUT})						
White level	VL_{WHITE}	0.59	0.70	0.81	V_{P-P}	RGBDATA = FF input
Red level	VL_{RED}	0.18	0.21	0.24	V_{P-P}	RDATA = FF input
Green level	VL_{GREEN}	0.35	0.41	0.47	V_{P-P}	GDATA = FF input
Blue level	VL_{BLUE}	0.07	0.08	0.09	V_{P-P}	BDATA = FF input
Sync level	VL_{SYNC}	0.27	0.30	0.33	V_{P-P}	—
Sync / white level ratio	RS / W	0.37	0.43	0.49	—	—
⟨Chrominance level⟩ (V_{OUT}, C_{OUT})						
Red / Burst level ratio	R_R / B_U	2.69	3.16	3.63	—	RDATA = FF input
Green / Burst level ratio	R_G / B_U	2.51	2.95	3.39	—	GDATA = FF input
Blue / Burst level ratio	R_B / B_U	1.91	2.24	2.57	—	BDATA = FF input
Burst level	VC_{BURST}	0.25	0.29	0.33	V_{P-P}	—
Red phase	θ_{RED}	94	104	114	deg	RDATA = FF input
Green phase	θ_{GREEN}	231	241	251	deg	GDATA = FF input
Blue phase	θ_{BLUE}	337	347	357	deg	BDATA = FF input
⟨RGB level⟩ (R_{OUT}, G_{OUT}, B_{OUT})						
ROUT output level	V_{ROUT}	0.56	0.70	0.81	V_{P-P}	RDATA = FF input
GOUT output level	V_{GOUT}	0.59	0.70	0.81	V_{P-P}	GDATA = FF input
BOUT output level	V_{BOUT}	0.59	0.70	0.81	V_{P-P}	BDATA = FF input
⟨Other⟩						
RGB DATA conversion frequency	f_{DA}	—	—	20	MHz	—
RGB DATA setup time	T_{SET}	20	—	—	ns	—
RGB DATA hold time	T_{HOLD}	20	—	—	ns	—
SYNCIN, NT / PAL input high level current	IH	—	—	300	μA	When 5V is applied to pin
SYNCIN, NT / PAL output low level current	IL	—	—	200	μA	When 0V is applied to pin

●Measurement circuit



●Circuit operation

(1) The DAC system clock is input to the VCLK pin. RGB data is taken into the IC at the rising edge of this clock.



(2) The subcarrier is input to the SCIN pin. There is an internal input capacitor in the IC, so no external DC cutoff is necessary. Also, the input level supports a range of 0.5 to 5$V_{p\text{-}p}$. To avoid offset in the chrominance phase, distortion-free sine waves or pulses with a duty of 50% should be input in a range which does not exceed the V_{CC} and GND.

(3) Composite SYNC signals are input to SYNCIN. When the input level is low, SYNC signals are output to the composite output (V_{OUT}) and luminance output (Y_{OUT}), and DC clamping of the RGB signals from the DAC is carried out at this timing. To prevent erroneous clamping, RGB data should be set to 00 input during the SYNC interval.

(4) Burst timing and the chrominance phase reversal timing when PAL is used are generated by SYNC signals and subcarriers. For this reason, signals input as SYNC signals and subcarriers should be in conformance with standards.

(5) The NT / PAL pin is used to select the video output system. When the input level is high, NTSC is selected, and when the input level is low, PAL is selected. When PAL is selected, the chrominance phase is reversed once every hour.

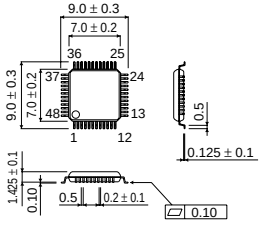
(6) A trap filter is connected to the YTRAP pin. This eliminates the chrominance band component that includes the luminance signal, and reduces cross-color. This filter is effective only for composite output (V_{OUT}), and does not affect luminance output (Y_{OUT}).

(7) Composite signals are output from the V_{OUT} pin. An internal 75Ω driver enables direct drive of the 75Ω load. (However, DC cutoff is required.)

(8) Luminance signals and chrominance signals are output from the Y_{OUT} and C_{OUT} pins, respectively. An internal 75Ω driver enables direct drive of the 75Ω load. (However, DC cutoff is required.)

(9) Analog RGB signals are output from R_{OUT}, G_{OUT}, and B_{OUT}. An internal 75Ω driver enables direct drive of the 75Ω load. (However, DC cutoff is required.)

●External dimensions (Units: mm)



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