bq2058T

Lithium Ion Pack Supervisor For 2-Cell Packs

Features

- Protects and individually monitors two Li-Ion series cells for overvoltage, undervoltage
- Monitors pack for overcurrent
- Designed for battery pack integration
- Minimal external components
- Drives external FET switches
- Selectable overvoltage (V_{OV}) thresholds
  - Mask programmable by Benchmarq
  - Standard version–4.25V
- Supply current: 12µA typical
- Sleep current: 0.7µA typical
- 16-pin 150-mil narrow SOIC

General Description

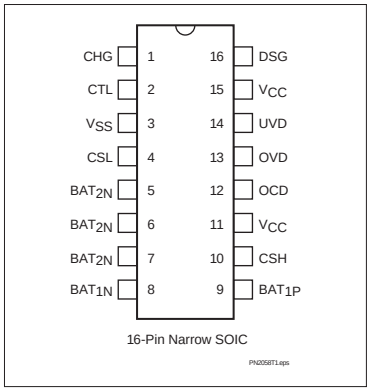
The bq2058T Lithium Ion Pack Supervisor is designed to control the charge and discharge cell voltage limits for two lithium-ion (Li-Ion) series cells, accommodating battery packs containing series/parallel configurations. The low operating current does not overdischarge the cells during periods of storage and does not significantly increase the system discharge load. The bq2058T can be part of a low-cost Li-Ion charge control system within the battery pack.

The bq2058T controls two external FETs to limit the charge and discharge potentials. The bq2058T allows charging when each individual cell voltage is below V_{OV} (overvoltage limit). If the voltage on any cell exceeds V_{OV} for a user-configurable delay period (t_{OVD}), the open-drain CHG pin goes to the high-impedance state, shutting off charge to the battery pack. This safety feature prevents overcharge of any cell within the battery pack. After an overvoltage condition occurs, each cell must fall below V_{CE} (charge enable voltage) for the bq2058T to re-enable charging.

The bq2058T protects batteries from overdischarge. If the voltage on any cell falls below V_{UV} (undervoltage limit) for a user-configurable delay period (t_{UVD}), the DSG output is driven low, shutting off the battery discharge. This safety feature prevents overdischarge of any cell within the battery pack.

The bq2058T also stops discharge on detection of an overcurrent condition, such as a short circuit. If an overcurrent condition occurs for a user-configurable delay period (t_{OCD}), the DSG output is driven low, disconnecting the load from the pack. DSG remains low until removal of the short circuit or overcurrent condition.

Pin Connections



16-Pin Narrow SOIC

PN2058T1.eps

Pin Names

CHG	Charge control output
CTL	Pack disable input
V_{SS}	Low potential input
CSL	Overcurrent sense low-side input
BAT_{2N}	Battery 2 negative input
BAT_{1N}	Battery 1 negative input
DSG	Discharge control output
UVD	Undervoltage delay input
OVD	Overvoltage delay input
OCD	Overcurrent delay input
V_{CC}	High potential input
CSH	Overcurrent sense high-side input
BAT_{1P}	Battery 1 positive input

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Pin Descriptions

CHG **Charge control output**

This open-drain output controls the charge path to the battery pack. Charging is allowed when high.

CTL **Pack disable input**

When high, this input allows an external source to disable the pack by making both DSG and CHG inactive. For normal operation, the CTL pin is low.

V_{SS} **Low potential input**

CSL **Overcurrent sense low-side input**

This input is connected between the low-side discharge FET (or sense resistor) and BAT_{2N} to enable overcurrent sensing in the battery pack's ground path.

BAT_{2N} **Battery 2 negative inputs (3 pins)**

These pins are connected to the negative terminal of the cell designated BAT2 in Figure 2.

BAT_{1N} **Battery 1 negative input**

This input is connected to the negative terminal of the cell designated BAT1 in Figure 2.

DSG **Discharge control output**

This push-pull output controls the discharge path to the battery pack. Discharge is allowed when high.

UVD **Undervoltage delay input**

This input uses an external capacitor to V_{CC} to set the undervoltage delay timing.

OVD **Overvoltage delay input**

This input uses an external capacitor to V_{CC} to set the overvoltage delay timing.

OCD **Overcurrent delay input**

This input uses an external capacitor to V_{CC} to set the overcurrent delay timing.

V_{CC} **High potential inputs (2 pins)**

CSH **Overcurrent sense high-side input**

This input is connected between the high-side discharge FET (or sense resistor) and BAT_{1P} to enable overcurrent sense in the battery pack's positive supply path.

BAT_{1P} **Battery 1 positive input**

This input is connected to the positive terminal of the cell designated BAT1 in Figure 2.

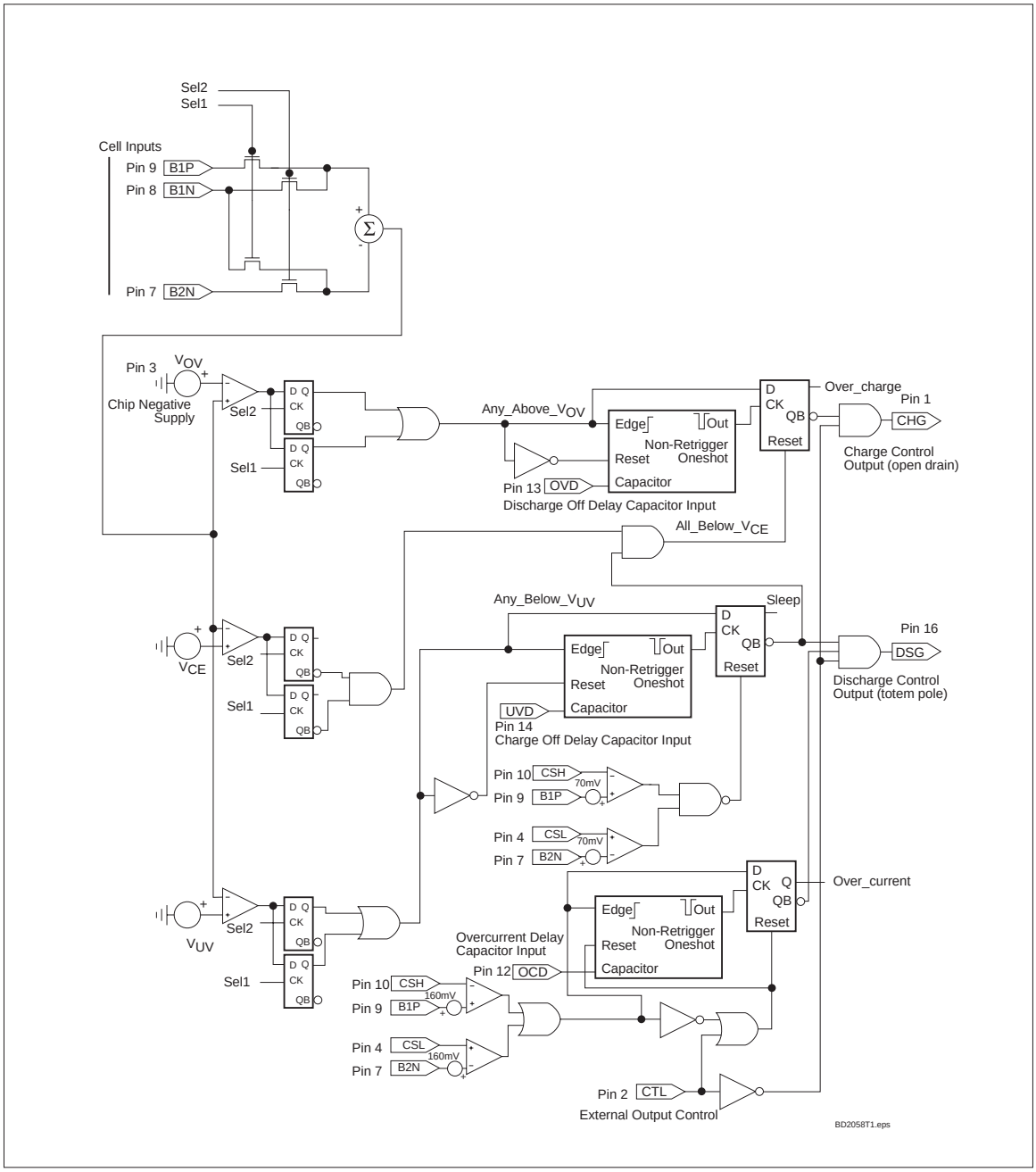


Figure 1. Block Diagram

Functional Description

Figure 1 is a block diagram outlining the major components of the bq2058T. Figure 2 shows a low-side control connection diagram. The following sections detail the various functional aspects of the bq2058T.

Thresholds

The bq2058T monitors the lithium ion pack for the conditions listed below. Shown with these conditions are the respective thresholds used to determine if that condition exists:

- Overvoltage (V_{OV})
- Undervoltage (V_{UV})
- Overcurrent (V_{OCH}, V_{OCL})
- Charge Enable (V_{CE})
- Charge Detect (V_{CD})

The bq2058T samples a cell every 60ms (typical). Every sample is a fully differential measurement of each cell. During this sample period, the bq2058T compares the measurements with these thresholds to determine if any of the these conditions exist: V_{OV}, V_{UV}, and V_{CE}.

Overcurrent and charge detect are conditions that are not sampled, but are continuously monitored.

Initialization

On initial power-up, such as connecting the battery pack for the first time to the bq2058T, the bq2058T enters the low-power sleep mode, disabling the DSG output. **It is recommended that a top to bottom cell connection be made at pack assembly for proper initialization.** A charging supply must be applied to the bq2058T circuit to enable the pack. See Low-Power Sleep Mode and Charge Detect sections.

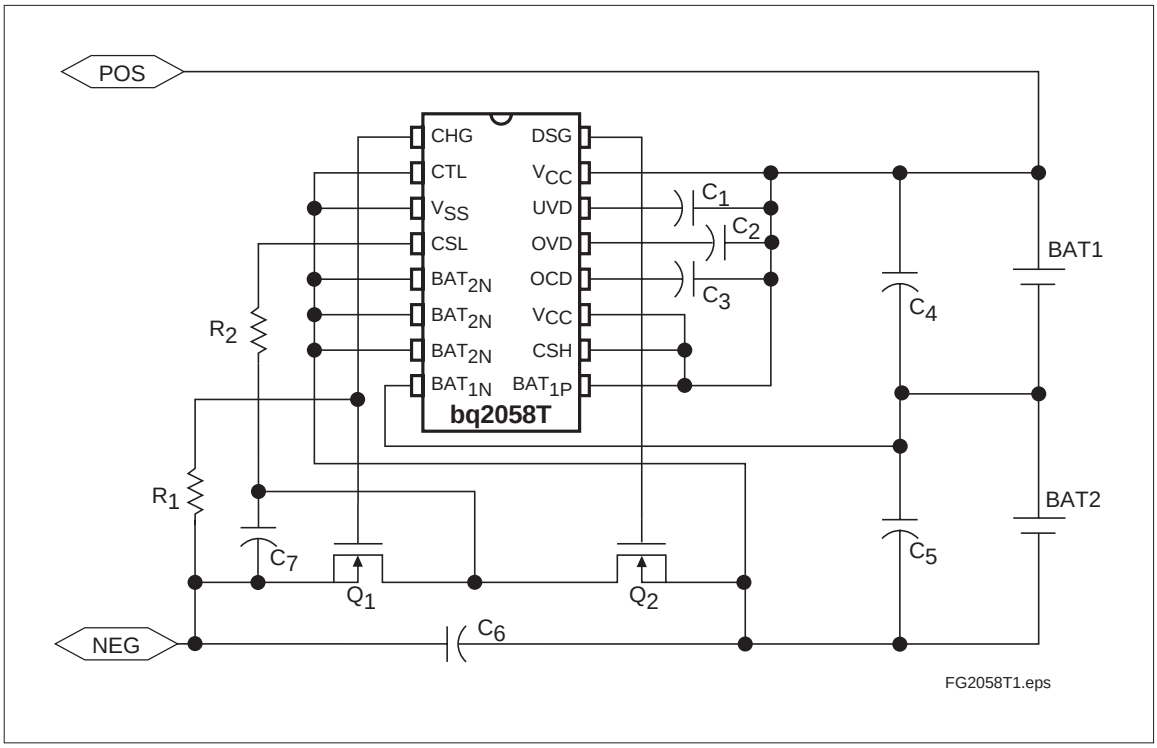


Figure 2. 2-Cell Connection Diagram, Low-Side Control

Low-Power Sleep Mode

The bq2058T enters the low-power sleep mode in two different ways:

1. On initial power-up.
2. After the detection of an undervoltage condition–V_{UV}.

When the bq2058T enters the low-power sleep mode, DSG is driven low and the device consumes 0.7µA (typical). The bq2058T only comes out of low-power sleep mode when a valid charge detect condition exists.

Charge Detect

The bq2058T continuously monitors for a charge detect condition. A valid charge detect condition exists when either of the conditions is true:

$$CSL < BAT_{2N} - 70mV\ (V_{CD})$$

$$CSH > BAT_{1P} + 70mV\ (V_{CD})$$

A valid charge detect enables the DSG output, allowing charging of the lithium ion cells. This is accomplished by applying the charging supply to the pack.

Undervoltage

Undervoltage (or overdischarge) protection is asserted when any cell voltage drops below the V_{UV} threshold and remains below the V_{UV} threshold for a time exceeding a user-configurable delay (t_{UVD}). The DSG output is driven low, disabling the discharge of the pack. The bq2058T then enters the low-power sleep mode. V_{UV} is defined as follows:

$$V_{UV} = 2.25V$$

Overvoltage

Overvoltage (or overcharge) protection is asserted when any cell voltage exceeds the V_{OV} threshold and remains above the V_{OV} threshold for a time exceeding a user-configurable delay (t_{OVD}). The CHG pin goes to the high impedance state, disabling charge into the battery pack. Since the charge control output is an open drain output, a pull-down resistor is needed from the CHG pin to the negative side of the pack. This pulls the gate of the charge FET low when the CHG pin goes to high impedance. Charging is disabled until a valid charge enable exists. See Charge Enable section.

Important note: If any battery pin floats (BAT_{1P}, BAT_{1N}, BAT_{2N}), the bq2058T assumes an overvoltage has occurred.

Because of different manufacturers' specifications for overvoltage thresholds, the bq2058T can be available with different V_{OV} options. Table 1 summarizes these different voltage thresholds.

Table 1. Overvoltage Threshold Options

Part #	V_{OV} Limit
bq2058T	4.25V
bq2058TR	4.35V

The overvoltage threshold limits are programmed at Benchmarq. The bq2058T is the standard option that is more readily available for sampling and prototyping purposes. Please contact Benchmarq for other voltage threshold and tolerance options.

Charge Enable

A valid charge enable indicates that an overvoltage (overcharge) condition no longer exists and that the pack is ready to accept further charge. Once overvoltage protection is asserted, charging will not be enabled until all cell voltages fall below V_{CE}. The V_{CE} threshold is a function of $V_{OV,}$ and changes with different V_{OV} limits.

$$V_{CE} = V_{OV} - 150mV$$

Overcurrent

The bq2058T detects an overcurrent (or short circuit) condition only in the discharge direction. Overcurrent protection is asserted when either of the conditions occurs and remain for a time exceeding a user-configurable delay (t_{OCD}):

$$CSL > BAT_{2N} + V_{OCL}$$

$$CSH < BAT_{1P} - V_{OCH}$$

where:

$$V_{OCL} = 160mV\ (\text{low-side detect})$$

$$V_{OCH} = 160mV\ (\text{high-side detect})$$

When either of these conditions occurs, DSG is driven low, disconnecting the load from the pack. DSG remains low until both of the voltage conditions are false, indicating removal of the short-circuit condition. The user can facilitate clearing these conditions by inserting the battery pack into a charger.

The high-side overcurrent sense can be disabled by connecting CSH to BAT_{1P}. This ensures that CSH is never greater than BAT_{1P}. If high-side detection is disabled, low-side detection must be used with CSL.

The FETs in the charge/discharge path controlled by the CHG and DSG pins affect the overcurrent level. The on-resistance of these FETs need to be taken into account when determining overcurrent levels.

CHG and DSG States

The CHG and DSG output truth table is shown below:

Condition	CHG pin	DSG pin
Normal operation	High	High
Overvoltage	Z	High
Undervoltage	High	Low
Overcurrent	High	Low
Floating battery input	Z	Indeterminate
CTL = high	Z	Low

The polarities of CHG and DSG are mask programmable at Benchmarq. Push-pull vs. open-drain configuration is also mask-configurable at Benchmarq. Please contact Benchmarq for availability of these variations.

Pack Disable Input–CTL

The CTL pin is used to electrically disconnect the battery from the pack terminals through an externally supplied signal. When CTL is taken high, CHG goes to the high impedance state and DSG is driven low. Any load on the pack terminals will be interpreted as an overcurrent condition by the bq2058T with the overcurrent delay timer held in reset. When the CTL pin is driven low, the overcurrent delay timer is allowed to start. If the programmed delay (t_{OCD}) is too short, the overcurrent recovery circuit, if implemented, will be unable to correct the overcurrent situation prior to the delay timeout. It is recommended that a delay time of greater than 10ms ($C_{OCD} \geq 0.01\mu F$) be used if the CTL pin function is to be utilized.

Important note: If CTL floats, it is internally pulled high making both DSG and CHG inactive, thus disabling the pack. If CTL is not used, it should be tied to V_{SS}.

The polarity of CTL is mask-programmable at Benchmarq. Please contact Benchmarq for other polarity options.

Protection Delay Timers

The delay time between the detection of an overcurrent, overvoltage, or undervoltage condition and the deactivation of the CHG and/or DSG outputs is user-configurable by the selection of capacitor values between V_{CC} and OCD, OVD, and UVD pins (respectively. See Table 2 below.

The fault condition must persist through the entire delay period, or the bq2058T may not deactivate either FET control output.

Figure 3 shows a step-by-step event cycle for the bq2058T.

Table 2. Protection Delay Timers

Protection Feature	Delay Period	Capacitor from V_{CC} to:	Typical		Tolerance
			Capacitor	Time	
Overcurrent	t_{OCD}	OCD	0.010µF	12ms	±40%
Overvoltage	t_{OVD}	OVD	0.100µF	950ms	±40%
Undervoltage	t_{UVD}	UVD	0.100µF	950ms	±40%

Notes:

1. The delay time versus capacitance can be approximated by the following equations:.

   For t_{OCD}: $t_{(s)} \approx 1.2 * C_{(\mu f)}$, where $0.001\mu F \leq C \leq 0.1\mu F$
   For t_{OVD}, t_{UVD}: $t_{(s)} \approx 9.5 * C_{(\mu f)}$, where $0.01\mu F \leq C \leq 1\mu F$

2. Overvoltage and undervoltage conditions are sampled by the bq2058T. The delay in Table 2 is in addition to the time required for the bq2058T to detect the violation, which may vary from 0 to 120 ms depending on where in the sampling period the violation occurs. Overcurrent is continuously monitored and is subject to a delay of approximately 1.5ms.

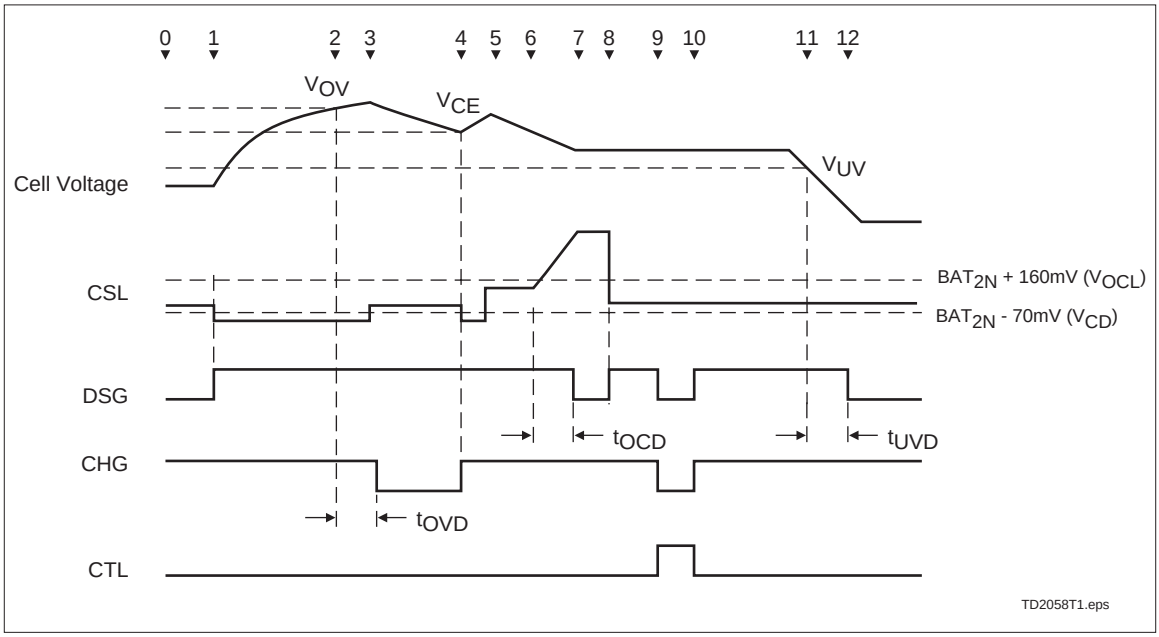


Figure 3. Protector Event Diagram

Event Definition:

0: The bq2058T is in the low-power sleep mode because one or more of the cell voltages are below V_{UV}.

1: A charger is applied to the pack, causing the difference between CSL and BAT_{2N} to become greater than 70mV. This awakens the bq2058T, and the discharge pin DSG goes high.

2: One or more cells charge to a voltage equal to V_{OV}, initiating the overvoltage delay timer.

3: The overvoltage delay time expires, causing CHG to go to high impedance (pulled low externally).

4: All cell voltages fall below V_{CE}, causing CHG to go high.

5: Stop charging, apply a load.

6: An overcurrent condition is detected, initiating the overcurrent delay timer.

7: The overcurrent delay time expires, causing DSG to go low.

8: The overcurrent condition is no longer present. DSG is driven high.

9: Pin CTL is driven high; both DSG and CHG go inactive.

10: Pin CTL is driven low; both DSG and CHG go active resuming their normal function.

11: One or more cells fall below V_{UV}, initiating the overdischarge delay timer.

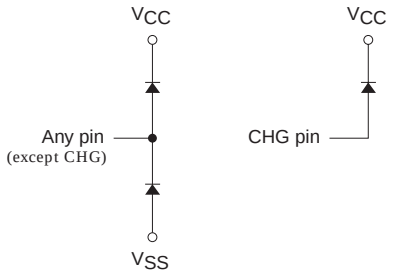
12: Once the overdischarge delay timer expires, if any of the cells is below V_{UV}, the bq2058T drives DSG low and enters the low-power sleep mode.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	Supply voltage	18	V	Relative to V_{SS}
T_{OPR}	Operating temperature	-30 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{IN}	Maximum input current	±100	µA	All pins except V_{CC}, V_{SS}

Notes: 1 Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

2. Internal protection diodes are in place on every pin relative to V_{CC} and V_{SS}. See picture below.



DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OH}	Output high voltage	V_{CC} - 0.5	-	-	V	I_{OH} = 10µA, CHG, DSG
V_{OL}	Output low voltage	-	-	V_{SS} + 0.5	V	I_{OL} = 10µA, CHG, DSG
V_{OP}	Operating voltage	0	-	9.0	V	V_{CC} relative to V_{SS}
V_{IL}	Input low voltage	-	-	V_{SS} + 0.5	V	Pin CTL
V_{IH}	Input high voltage	V_{SS} + 2.0	-	-	V	Pin CTL
I_{CCA}	Active current	-	12	25	µA	
I_{CCS}	Sleep current	-	0.7	1.5	µA	
R_{CELL}	Input impedance	-	10	-	MΩ	Pins BAT_{2N}, BAT_{1N}, and BAT_{1P}

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Unit	Tolerance	Conditons
V_{OV}	Overvoltage threshold	4.25	V	±55mV	See note 1
		Table 1			Customer option
V_{CE}	Charge enable threshold	V_{OV} - 150mV	V	±55mV	
V_{UV}	Undervoltage threshold	2.25	V	±100mV	
V_{OCH}	Overcurrent detect high-side	160	mV	±35mV	
V_{OCL}	Overcurrent detect low-side	160	mV	±35mV	
V_{CD}	Charge detect threshold	70	mV	-60mV, +80mV	
t_{OVD}	Overvoltage delay threshold	950	ms	±40%	C_{OVD} = 0.100µF T_A = 30°C See note 2
t_{UVD}	Undervoltage delay threshold	950	ms	±40%	C_{UVD} = 0.100µF T_A = 30°C See note 2
t_{OCD}	Overcurrent delay thresh-old	12	ms	±40%	C_{OCD} = 0.01µF T_A = 30°C

Notes: 1. Standard device. Contact Benchmarq for different thresholds and tolerance options

2. Does not include cell sampling delay, which may add up to 120ms of additional delay until the condition is detected.

Typical Characteristics

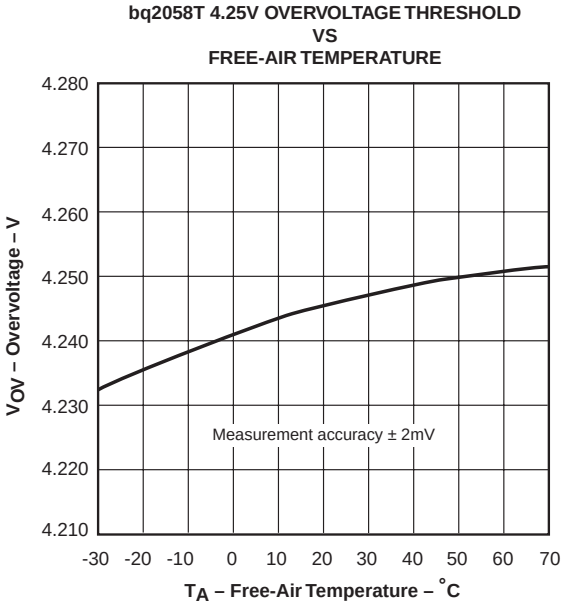


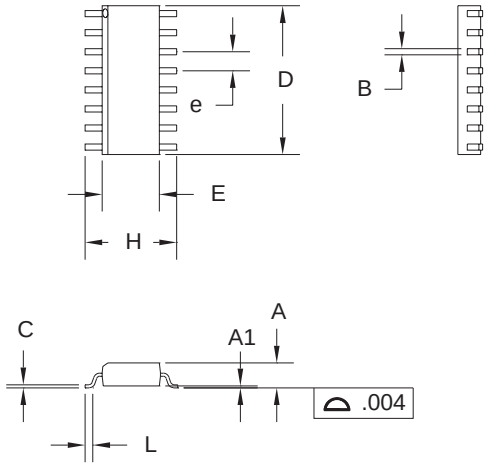
Figure 4

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	5	CHG pin output state	CHG pin state at overvoltage and floating battery input was low, is now Z
1	9	Overcurrent limits	Was: V_{OCL} = 100mV ±25mV Is: V_{OCL} = 150mV ±25mV
1	9	Charge detect threshold	Was: 70mV +10mV, +80mV Is: 70mV -60mV, +80mV
2	4	Overvoltage options, Table 1	Added bq2058TR
2	4	Figure 2	Corrected schematic
2	6, 9	Delay thresholds	Was: t_{OCD} = 10ms ±30% t_{OVD} = 800ms ±30% t_{UVD} = 800ms ±30% Is: t_{OCD} = 12ms ±40% t_{OVD} = 950ms ±40% t_{UVD} = 950ms ±40%
2	7	DSG and CHG timing diagram	Inverted lines for proper logic levels
2	7	Timing Diagram	Was: CSH timing Is: CSL timing
2	8	Maximum input current	Added I_{IN}
2	9	V_{OV} tolerance	Was: ±50mV Is: ±55mV
2	9	Overcurrent limits	Was: V_{OCH} = 160mV +25mV V_{OCL} = 150mV +25mV Is: V_{OCH} = 160mV +35mV V_{OCL} = 160mV +35mV
2	9	V_{OP}	Was: 0V min, 18V max Is: 4V min, 9V max

Note: Change 1 = June 19, 1997 changes from April 22, 1997.
Change 2 = July 1997 changes from June 19, 1997

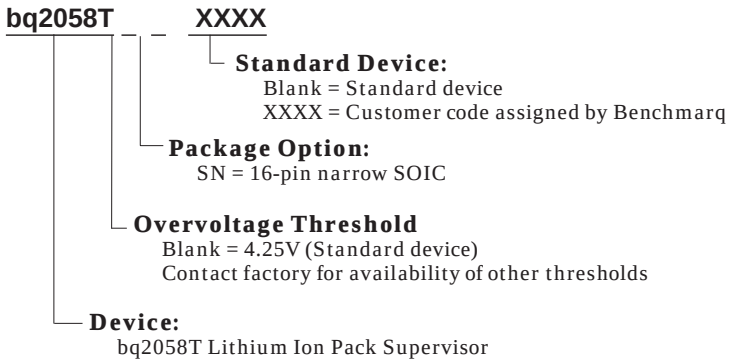
SN: 16-Pin SN (0.150" SOIC)



16-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

Ordering Information



Package Devices		
T_A	V_{OV} Threshold	16-pin Narrow SOIC (SN)
-30°C to +70°C	4.25V	bq2058TSN
	4.35V	bq2058TRSN

Note: bq2058TSN is Standard Device
Contact factory for availability of other thresholds and tolerances.

Notes

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July 1997

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