

# 16kbit serial ferroelectric memory

## BR24CF16F

The BR24CF16F is a non-volatile ferroelectric memory developed for use in ROHM's non-volatile memory technology and ferroelectric technology. Using a ferroelectric memory enables faster writing speeds than EEPROM and flash memories, increases the number of times that rewriting can be carried out, and reduces the power consumption. This product is compatible with general-purpose EEPROM memory hardware (supports the I<sup>2</sup>C BUS) and software.

### ●Applications

Portable equipment (PDAs, etc.), memory backup units for game machines, cable TVs, displays, printers, facsimile machines, TVs, cameras, and other office automation equipment

### ●Features

- 1) Non-volatile random access memory
- 2) Rewriting possible up to 10<sup>12</sup> times
- 3) No waiting time when writing data
- 4) Data can be retained for up to ten years
- 5) Supports 2 wire serial interface (I<sup>2</sup>C BUS)
- 6) Low current consumption (100  $\mu$ A max., in normal mode)

### ●Absolute maximum ratings (Ta=25°C)

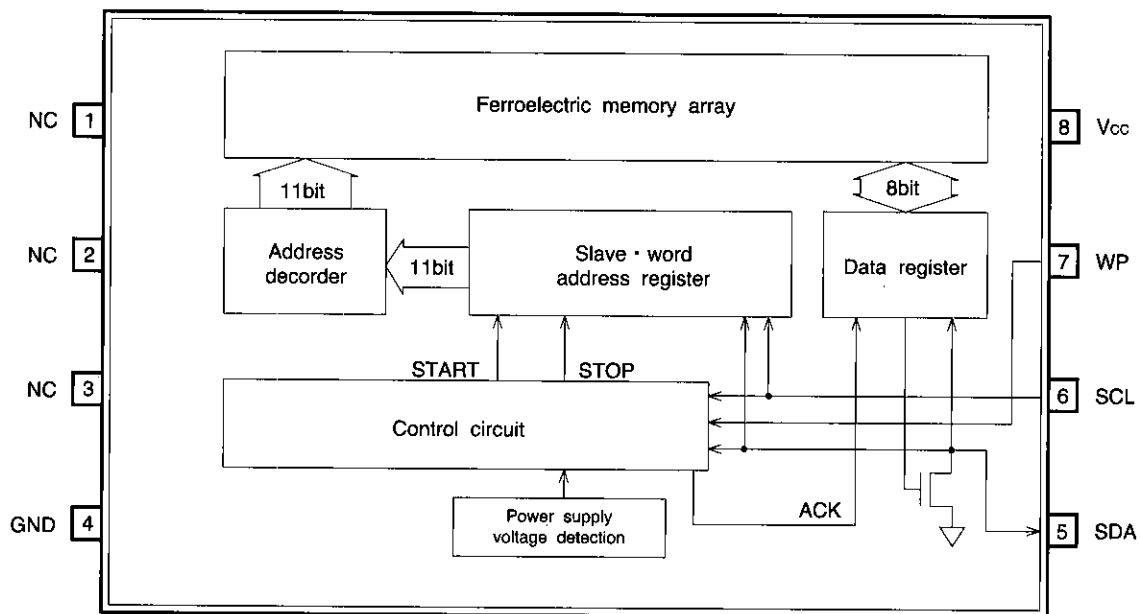
Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>CC</sub>	-0.3~7.0	V
Power dissipation	P <sub>d</sub>	350*	mW
Operating temperature	T <sub>opr</sub>	-40~85	°C
Storage temperature	T <sub>stg</sub>	-65~125	°C

\* Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

### ●Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>CC</sub>	4.5~5.5	V
Input voltage	V <sub>in</sub>	0~V <sub>CC</sub>	V

● Block diagram



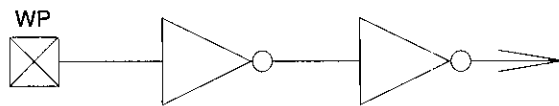
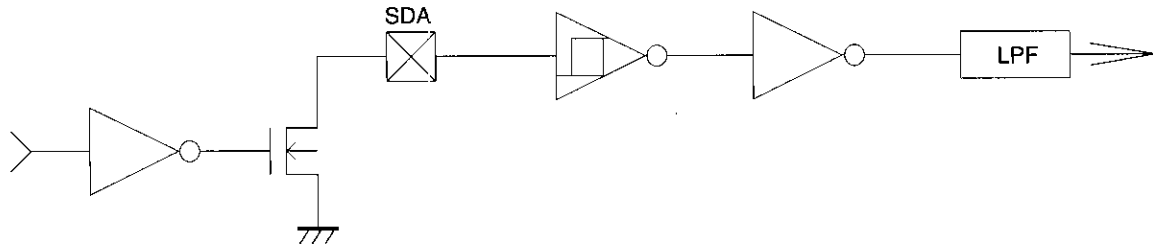
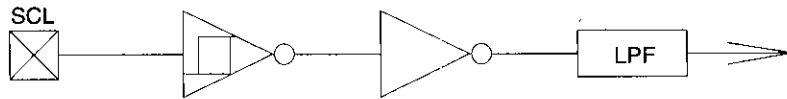
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● Pin descriptions

Pin Name	I/O	Function
Vcc	—	Power supply.
GND	—	Reference voltage for all inputs and outputs: 0 V(Ground)
SCL	Input	Serial clock input
SDA	Input/output	Slave and word address, serial data output
WP	Input	Hardware and Write Protect pin
NC	—	No connected

\* The SDA pin is Nch open drain output, so an external pull-up resistance should be added.

●Input/output equivalent circuits



●Electrical characteristics (Unless otherwise noted, Ta = -40 to 85°C, Vcc = 4.5 to 5.5V)

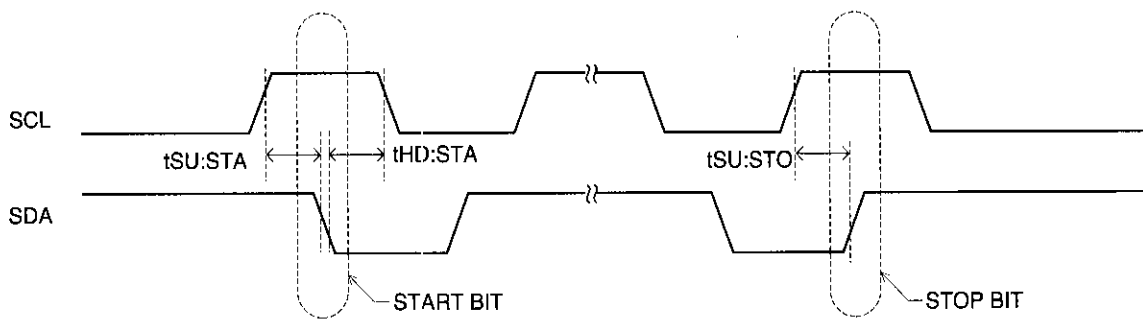
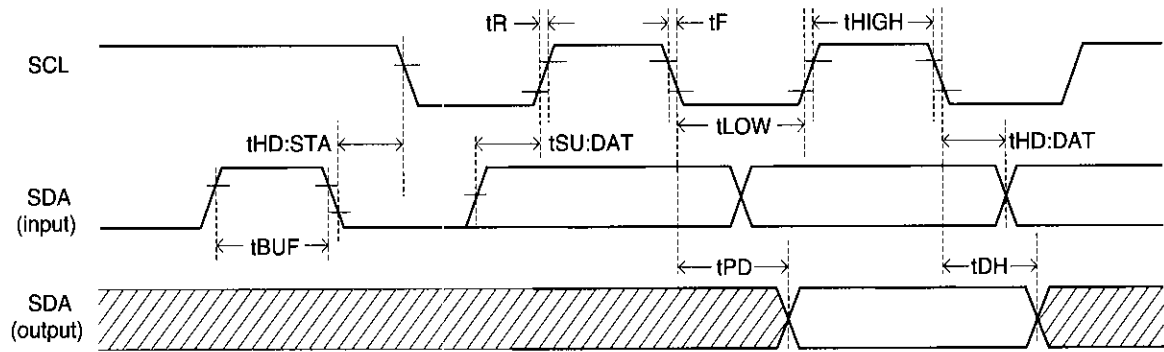
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
"H" input voltage	VIH	0.7VCC	—	—	V		
"L" input voltage	VIL	—	—	0.3VCC	V		
"L" output voltage	VOL	—	—	0.4	V	IOL=3.0mA (SDA)	Fig.1
Input leakage current	ILI	-1	—	1	μA	VIN=0V~Vcc	Fig.2
Output leakage current	ILO	-1	—	1	μA	VOUT=0V~Vcc	Fig.2
Operating current consumption	ICC	—	60	100	μA	fSCL=100kHz CMOS input	Fig.3
		—	180	300	μA	fSCL=400kHz CMOS input	Fig.3
Standby current	ISB	—	16	60	μA	SCL SDA=VCC	Fig.4
SCL frequency	fSCL	—	—	100	kHz		
		—	—	400	kHz		

● Operation timing characteristics (Unless otherwise noted,  $T_a = -40$  to  $85^\circ\text{C}$ ,  $V_{CC} = 4.5$  to  $5.5\text{V}$ )

Parameter	Symbol	fSCL=100kHz			fSCL=400kHz			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Data clock "H" time	tHIGH	4.0	—	—	0.6	—	—	$\mu\text{S}$
Data clock "L" time	tLOW	4.7	—	—	1.3	—	—	$\mu\text{S}$
SDA/SCL rise time	tR	—	—	1.0	—	—	0.3	$\mu\text{S}$
SDA/SCL fall time	tF	—	—	0.3	—	—	0.3	$\mu\text{S}$
Start condition hold time	tHD:STA	4.0	—	—	0.6	—	—	$\mu\text{S}$
Start condition setup time	tSU:STA	4.7	—	—	0.6	—	—	$\mu\text{S}$
Input data hold time	tHD:DAT	0	—	—	0	—	—	nS
Input data setup time	tSU:DAT	250	—	—	100	—	—	nS
Output data "L" delay time	tPDO	—	—	3.0	—	—	3.0	$\mu\text{S}$
Output data hold time	tDH	0	—	—	0	—	—	$\mu\text{S}$
Stop condition setup time	tSU:STO	4.0	—	—	0.6	—	—	$\mu\text{S}$
Bus release time before transmission starts	tBUF	4.7	—	—	1.3	—	—	$\mu\text{S}$
Noise reduction valid period (SCL/SDA pins)	tl	—	—	50	—	—	50	nS

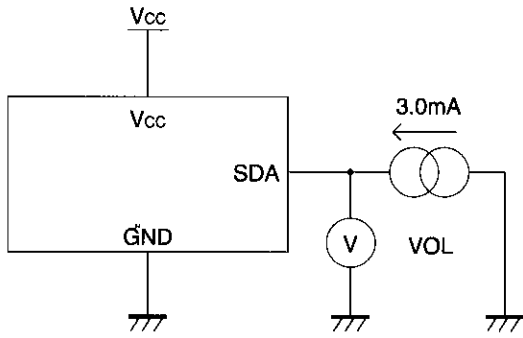
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● Synchronous data input/output timing



Reading of input data begins at the rising edge of SCL.  
Data output is synchronized to the falling edge of SCL.

● Measurement circuits



Output : L

Fig. 1 "L" output voltage measurement circuit

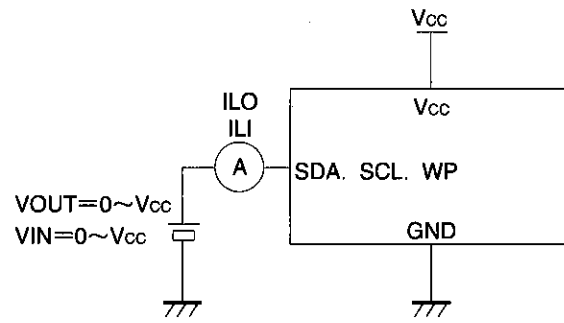


Fig. 2 Input/output leakage current measurement circuit

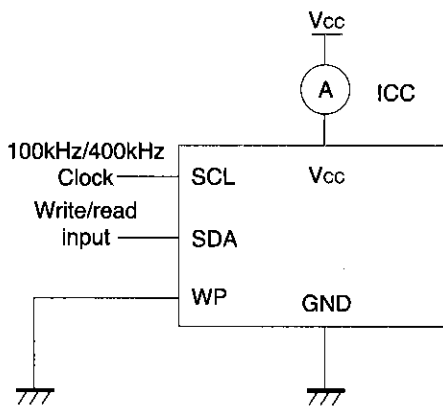


Fig.3 Current dissipation measurement circuit

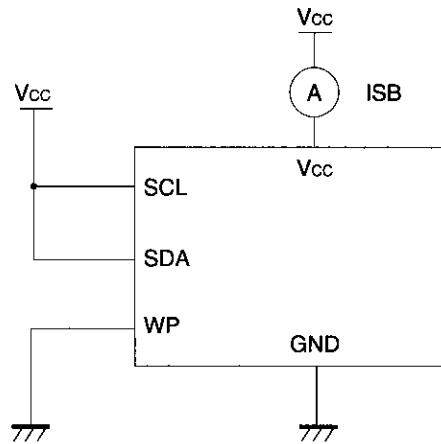


Fig.4 Standby current measurement circuit

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● Circuit operation

• Start condition (acknowledgement of start bit)

Before executing any command, a start condition (start bit) must be input. When SCL is HIGH, a start condition causes SDA to fall from HIGH to LOW. No command input will be accepted unless this start condition is input.

• Stop condition (acknowledgement of stop bit)

To stop any command, a stop condition (stop bit) is required. A stop condition is achieved when SDA goes from LOW to HIGH while SCL is HIGH.

• Precautions concerning write commands

With the Write command, writing of the data begins when the stop bit is input, after the data has been input.

• Device addressing (specifying the slave address)

Make sure the slave address is output from the master immediately after the start condition.

The upper four bits of the slave address are used to determine the device type. The device code for this IC is fixed at "1010". The next three bits of the slave address (PS2~0) are used to select the page. The 16KB memory is configured of 256 bytes × 8 pages, and the page to be accessed is selected by specifying PS2~0. The lower-most bit of the slave address (R/W) is used to set the write or read mode as follows.

R/ $\bar{W}$  set to 0.....Write or random read

R/ $\bar{W}$  set to 1.....Read

Device Type	Page Select	
1010	PS2 PS1 PS0	R / $\bar{W}$

• WP (Write Protect pin)

Setting the WP pin to V<sub>CC</sub> (HIGH) inhibits writing of data to the upper four pages (pages 4 to 7) of the eight available pages. Setting the WP pin to GND (LOW) enables normal writing operations.

- ACK signal

The acknowledge signal (ACK signal) is determined by software and is used to indicate whether or not a data transfer is proceeding normally. The transmitting device, whether the master or slave, opens the bus after an 8-bit data output (the master when a write or read command of the slave address is input; the BR24CF16F when reading data). For the receiving device during the ninth clock cycle, SDA is set to LOW and an acknowledge signal (ACK signal) is sent to indicate that it received the 8-bit data (the master when a write command or a read command is input to a slave address, the BR24CF16F when a read command is output).

When data is being written to this IC, a LOW acknowledge signal (ACK signal) is output after the receipt of each eight bits of data (word address and write data).

When data is being read from the IC, eight bits of data (read data) are output and the IC waits for a returned LOW acknowledge signal (ACK signal). When an acknowledge signal (ACK signal) is detected and a stop condition is not sent from the master side, the IC continues to output data. If an acknowledge signal (ACK signal) is not detected, the IC interrupts the data transfer and ceases reading operations after recognizing the stop condition (stop bit). The IC then enters the waiting or standby state.

(See Figure 5 for acknowledge signal (ACK signal) response.)

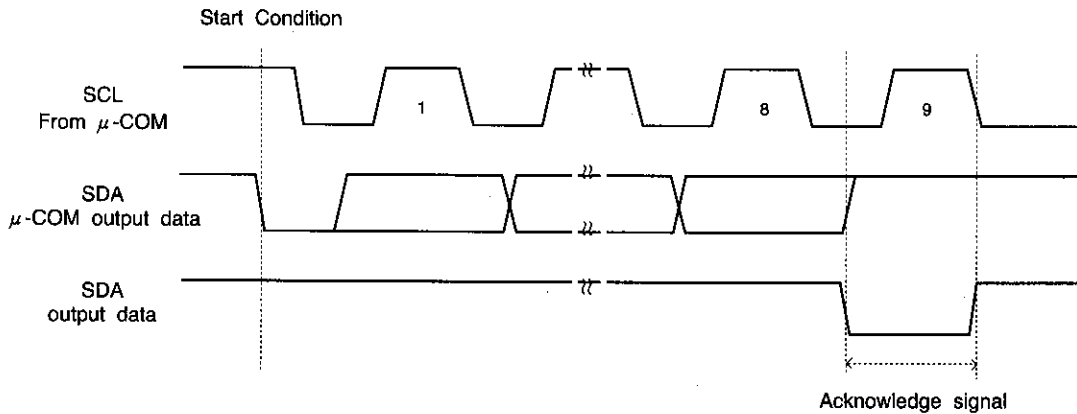


Fig.5 Acknowledge signal (ACK signal) response  
(during write and read slave address input)



## ● Timing charts

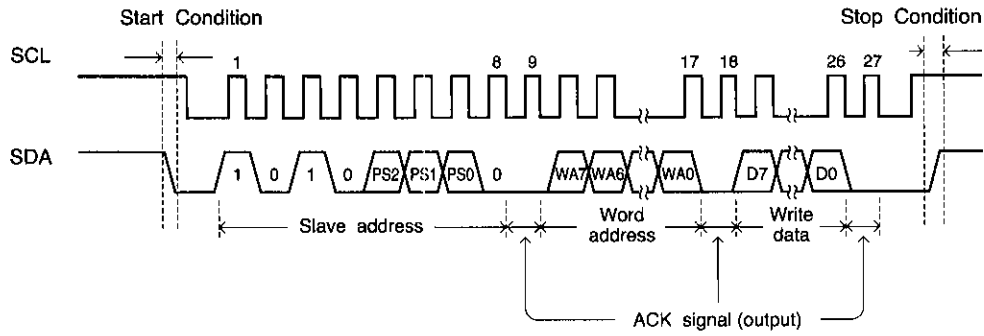


Fig. 6 Byte write cycle

- Data is written to the address designated by the WA7~WA0, on the page specified by PS2~PS0.
- After eight bits of data are input, the data is written to the memory cell by issuing the stop bit.

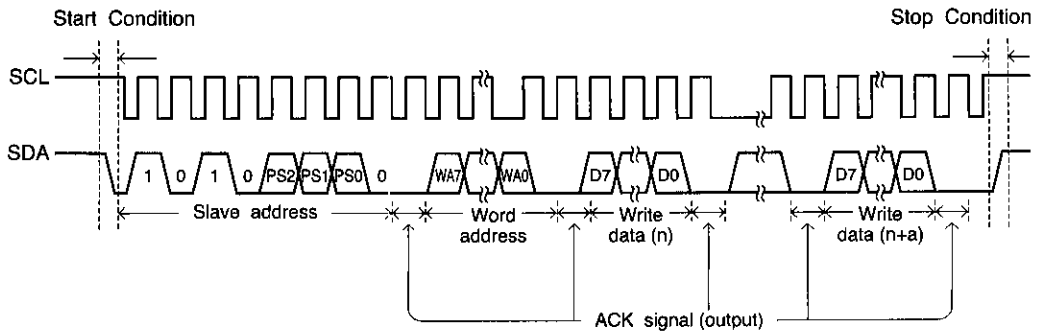


Fig. 7 Multi-byte write cycle

- To write data to consecutive addresses, the Multi Byte Write command can be used to omit input of the address.
- If data is input after the ACK signal which follows the normal Byte Write command, that data is written to the (specified address + 1) address.
- The Multi Byte Write command remains valid until a stop condition is input, with no restriction on the number of bytes.

## ● Timing charts

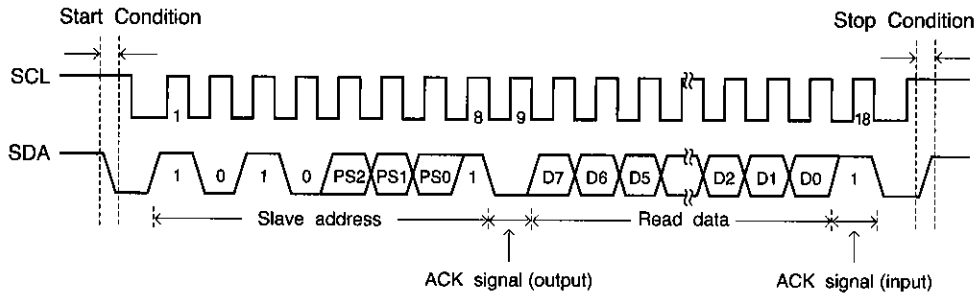


Fig. 8 Current read cycle

- This IC increments the address by one position by using the internal circuit address count. It records the final-word address ( $n$  address) of the executed write - read command.
- This command reads the data of the next word address ( $n + 1$  address) of the final write word address after the execution of the previous command.
- When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master ( $\mu$ -COM), the next word address data can be read. (See Figure 10 for the sequential read cycle.)
- This command is ended by inputting HIGH to the ACK signal after D0 and raising the SDA signal (stop condition) by setting SCL to HIGH.

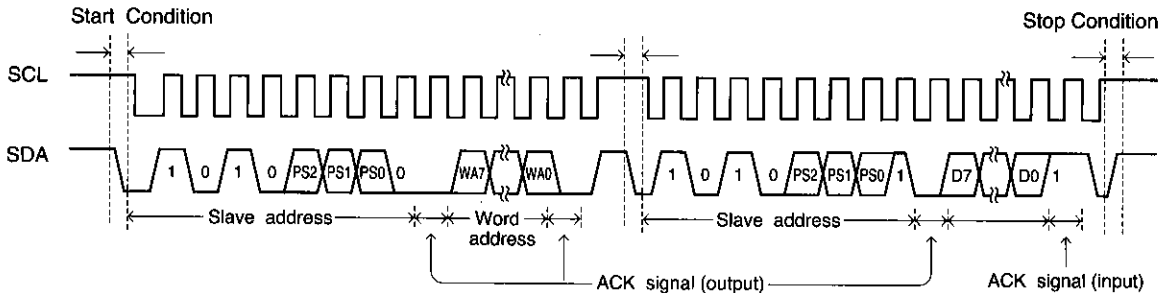


Fig. 9 Random read cycle

- This command can read the designated word address data.
- When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master ( $\mu$ -COM), the next word address data can be read. (See Figure 10 for the sequential read cycle.)
- This command is ended by inputting a HIGH signal to the ACK signal after D0 and raising the SDA signal (stop condition) by raising SCL to HIGH.

● Timing charts

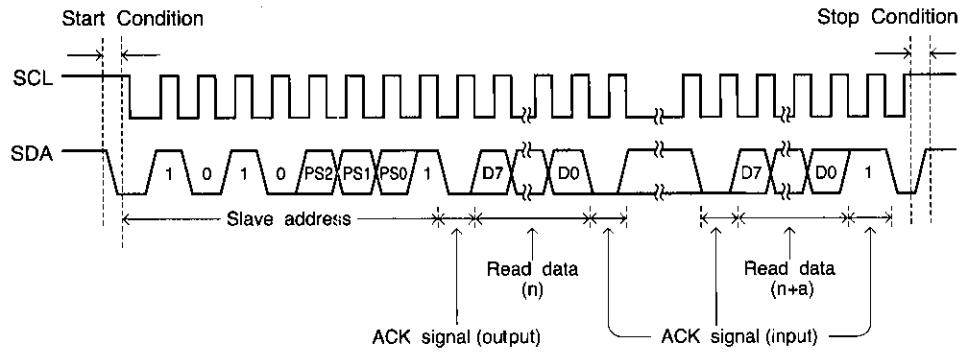
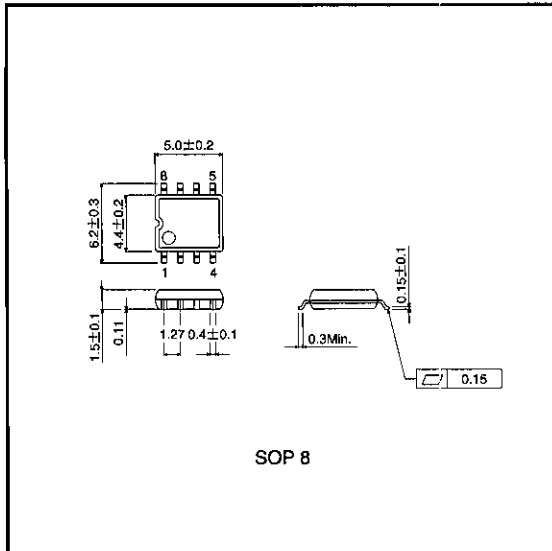


Fig. 10 Sequential read cycle  
(Example: For a current read)

- When an ACK signal LOW is detected after D0 and a stop condition is not sent from the master ( $\mu$ -COM), the next word address data can be read.
- This command is ended by inputting a HIGH signal to the ACK signal after D0 and raising the SDA signal (stop condition) using the SCL signal HIGH.
- Sequential reading can also be done with a random read.

● External dimensions (Units: mm)



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