

PLL frequency synthesizer for tuners

BU2611A/BU2611AF/BU2611AFS

BU2611 PLL frequency synthesizers work up through the FM band. They feature built-in RF amps with low power consumption and high sensitivity.

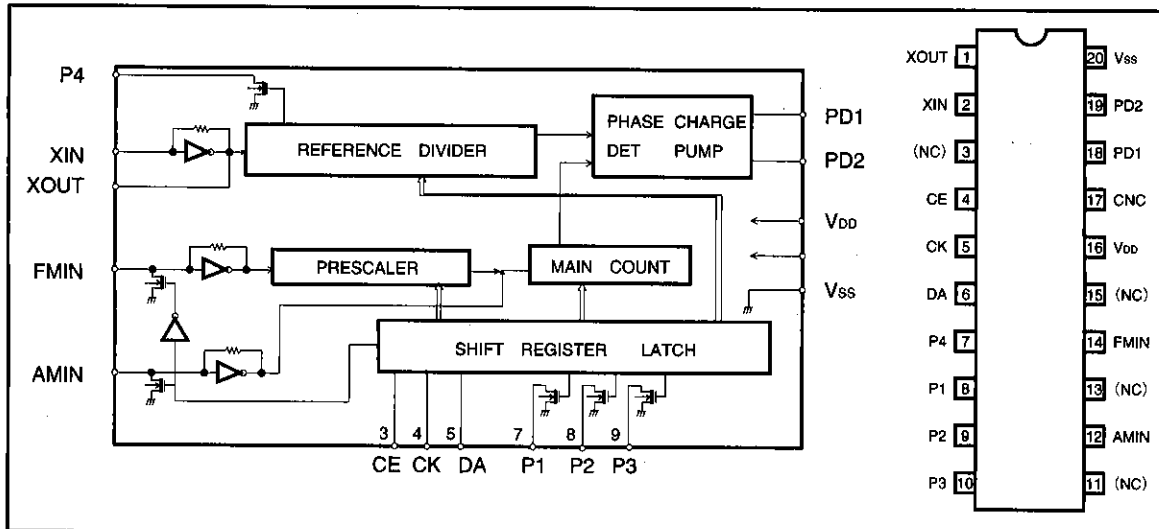
●Applications

Tuners (Mini components, radio cassette players, radio equipment, etc.)

●Features

- 1) Built-in high-speed prescaler can divide 130 MHz/VCO.
- 2) In addition to the standard FM and AM, also offers the following 7 frequencies : 100kHz, 50kHz, 25kHz, 10kHz, 9kHz, 5kHz, and 1kHz.
- 3) 3-bit output port (open drain)
- 4) Clock output (400kHz)
- 5) Time base output (8Hz)
- 6) Serial data input (CE,CK,DA)

●Block diagram



PLL frequency synthesizers

High-frequency signal processors

● Pin description

Terminal name	Function
P4	Controller clock (400 kHz) output
XIN, XOUT	Xtal oscillation (7.2 MHz)
FMIN, AMIN	Local oscillation signal input
CE, CK, DA	Data input
P1, P2, P3	Output port
V	Power supply
PD1, PD2	Phase comparison charge pump output

● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit	Conditions
Supply voltage		V _{DD}	-0.3~+7.0	V	
Maximum input voltage		V _{IN}	-0.3~V _{DD} +0.3	V	CE, CK, CA, XIN, FMIN, AMIN
Maximum output voltage 1		V _{OUT1}	-0.3~10.0	V	P1, P2, P3, P4
Maximum output voltage 2		V _{OUT2}	-0.3~V _{DD} +0.3	V	PD1, PD2
Maximum output current		I _{OUT}	0~4.0	mA	P1, P2, P3, P4
Power dissipation	BU2611A	P _D	1000 *1	mW	
	BU2611AF/BU2611AFS		500 *2		
Operating temperature		T _{opr}	-25~75	°C	
Storage temperature		T _{stg}	-55~125	°C	

*1 Reduced by 10mW for each increase in Ta of 1°C over 25°C.

*2 Reduced by 5mW for each increase in Ta of 1°C over 25°C.

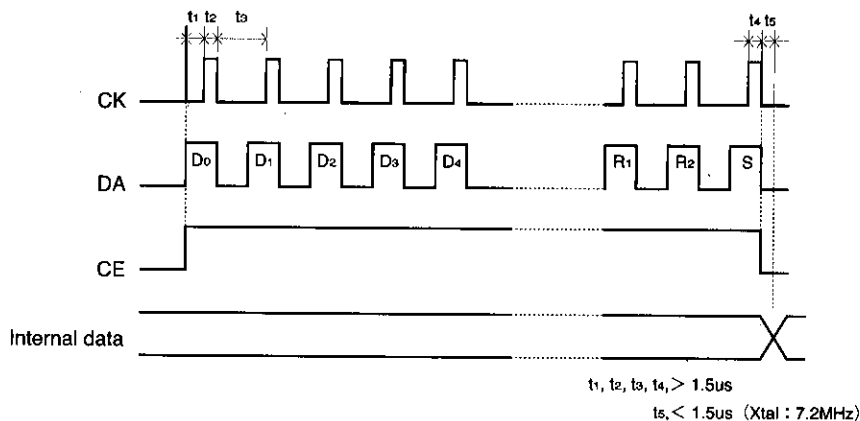
● Recommended operating conditions

Parameter	Symbol	Limits	Unit
Supply voltage	V _{DD}	4.0~6.0	V

●Electrical characteristics (unless other specified, Ta = 25°C, VDD = 5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage	IDD1		4.8		mA	F _{IN} =130MHz, 100mVrms
Circuit current w/o signal	IDD2		300		μA	No input, PLL = OFF
"H" level input voltage	V _{IH}	3.5			V	CE, CK, DA terminals
"L" level input voltage	V _{IL}			1.5	V	CE, CK, DA terminals
"L" level output voltage 1	V _{OL1}		0.4		V	P1, P2, P3, P4 I _{OUT} =2.0mA
"OFF" level leakage current 1	I _{OFF1}			1.0	μA	P1, P2, P3, P4 V _{OUT} =10V
"H" level output voltage	V _{OH}		0.25		V	PD1, PD2 I _{OUT} =-1.0mA
"L" level output voltage 2	V _{OL2}		0.15		V	PD1, PD2 I _{OUT} =1.0mA
"OFF" level leakage current 2	I _{OFF2}			100	nA	PD1, PD2 V _{OUT} =V _{DD}
"OFF" level leakage current 3	I _{OFF3}	-100			nA	PD1, PD2 V _{OUT} =V _{SS}
Input frequency 1	F _{IN1}		7.2		MHz	XIN, sine wave, C coupling
Input frequency 2	F _{IN2}	10		130	MHz	F _{MIN} , sine wave, C coupling V _{IN} = 80 mVRMS
Input frequency 3	F _{IN3}	0.5		20	MHz	A _{MIN} , sine wave, C coupling V _{IN} = 80 mVRMS
Input amplitude	F _{INMax}	0.08		1.5	Vrms	XIN, F _{MIN} , A _{MIN} , sine wave, C coupling

●Data format



D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃
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← Input done from D₀.

T ₀	T ₁	P ₀	P ₁	P ₂	T _B	R ₀	R ₁	R ₂	S
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(1) Division data : For D₀ through D₁₃ (For AMN, use D₄ through D₁₃.)

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	
1	1	0	0	1	0	1	0	0	0	1	0	0	0	→F _{MIN} frequency = 1107
X	X	X	X	0	1	1	1	1	0	0	1	1	1	→A _{MIN} frequency = 926

(2) Test data : T₀ through T₁ are taken as (0, 0).

●Data format

(3) P₀, P₁, P₂, P₃, TB : port output, time base output

Data				Port output		
P ₀	P ₁	P ₂	TB	P ₁	P ₂	P ₃
0	0	0	0	※	※	※
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	0	1	1
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	0	1	1	0
1	1	1	0	1	1	1
0	0	0	1	TB	※	※
X	1	0	1	TB	1	0
X	0	1	1	TB	0	1
X	1	1	1	TB	1	1
1	0	0	1	TB	0	0

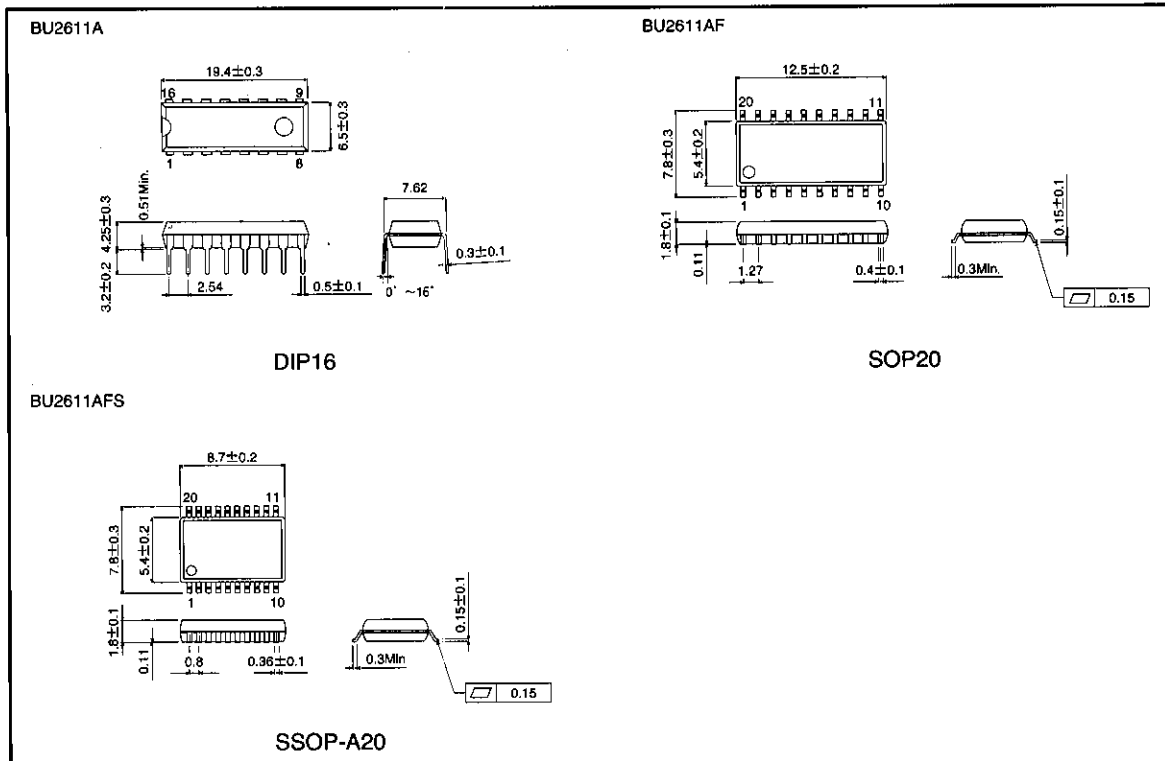
※ : Determined on the basis of R₀ - R₂.
 X : don't care
 TB: 8 Hz

(4) R₀, R₁, R₂, standard frequency data

Data			Standard frequency	Port output		
R ₀	R ₁	R ₂		P ₁	P ₂	P ₃
0	0	0	100kHz	1	1	0
0	0	1	50	1	1	0
0	1	0	25	1	1	0
0	1	1	5	0	0	1
1	0	0	10	1	0	1
1	0	1	9	1	0	1
1	1	0	1	0	1	1
1	1	1	5	0	0	1

(5) S : input selection data 1 : FMIN 0 : AMIN

●External dimensions (Unit: mm)



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