

PLL frequency synthesizer for tuners

BU2616F

BU2616F PLL frequency synthesizers work up through the FM band.

Featuring low power consumption and highly sensitive built-in RF amps, they detect intermediate frequencies.

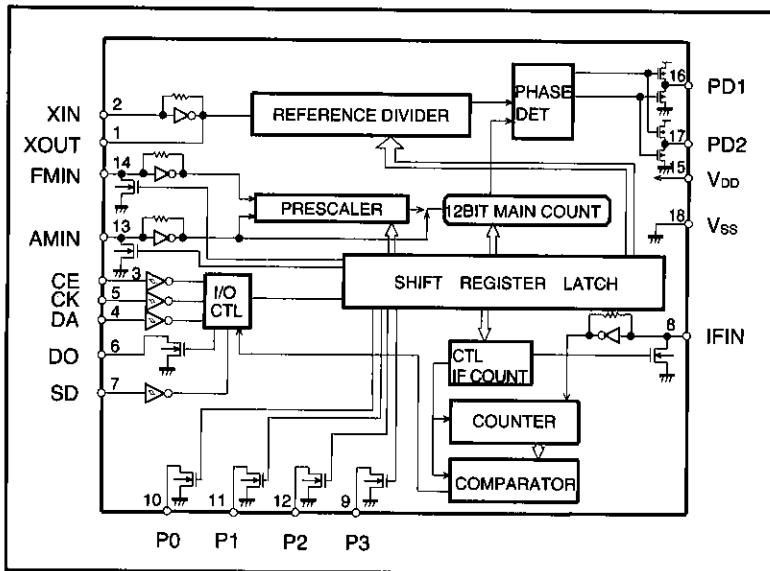
●Applications

Tuners (Mini components, radio cassette players, radio equipment, etc.)

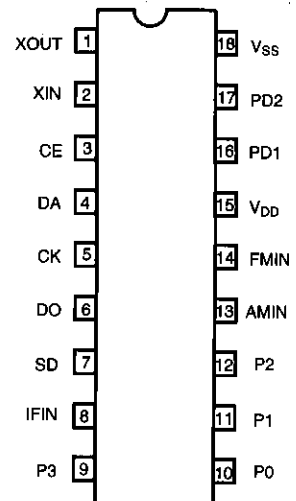
●Features

- 1) Built-in high-speed prescaler can divide 130MHzVCO.
- 2) Low power-consumption (during operation : 6mA PLL OFF 1mA)
- 3) In addition to the standard FM and AM, also offers the following 7 frequencies : 25kHz, 12.5kHz, 6.25kHz, 10kHz, 9kHz, 5kHz, and 1kHz.
- 4) SD (station detector) input circuit.
- 5) Intermediate frequency detection circuit
- 6) Charge pump output control circuit
- 7) Four output ports (Nch open drain).
- 8) Serial data input (CE.CK.DA)

●Block diagram



●Pin assignments



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●Pin description

Pin No.	Symbol	Terminal name	Function	I/O
1	XOUT	Crystal oscillation terminal	For generation of standard frequency and internal clock. Connected to 7.2 MHz crystal oscillator.	OUT
2	XIN			IN
3	CE	Chip enable	When CE is H, DA is synchronous with the rise of CK and read to the internal shift register. DA is then latched at the timing of the fall of CE. Also, output data is output from the CD terminal synchronous to the rise of CK.	IN
4	DA	Serial data		
5	CK	Clock signal		
6	DO	Data out	Comes ON during IF frequency detection or SD detection.	Nch open drain
7	SD	SD input	SD signal is input. Observed by DO terminal.	IN
8	IFIN	IF input	Input is for IF frequency.	
9	P3	Output port	Controlled on the basis of input data.	Nch open drain
10	P0			
11	P1			
12	P2			
13	AMIN	AM input	Local input for AM	IN
14	FMIN	FM input	Local input for FM	IN
15	V _{DD}	Power supply	Power supply, with 4.0V to 6.0V applied voltage.	
16	PD1	Phase comparison output	High level when value obtained by dividing local output is higher than standard frequency. Low level when value is lower. High impedance when value is same.	3-state
17	PD2			
18	V _{SS}	GROUND		

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit	Conditions
Supply voltage	V _{DD}	-0.3~7.0	V	V _{DD}
Maximum input voltage 1	V _{IN1}	-0.3~7.0	V	CE, CK, DA, SD
Maximum input voltage 2	V _{IN2}	-0.3~V _{DD} +0.3	V	XIN, FMIN, AMIN, IFIN
Maximum output voltage 1	V _{OUT1}	-0.3~10.0	V	P0, P1, P2, P3, DO
Maximum output voltage 2	V _{OUT2}	-0.3~V _{DD} +0.3	V	PD1, PD2, XOUT
Maximum output current	I _{OUT}	0~3.0	mA	P0, P1, P2, P3, DO
Power dissipation	P _d	450*	mW	
Operating temperature	T _{opr}	-10~75	°C	
Storage temperature	T _{stg}	-55~125	°C	

* Reduced by 4.5mW for each increase in Ta of 1°C over 25°C.

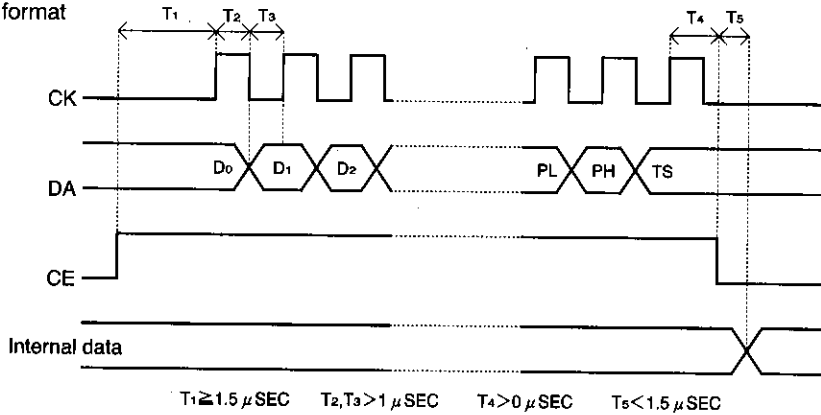
●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	V _{DD}	4.0~6.0	V

●Electrical characteristics (unless other specified, Ta = 25°C, VDD1 = VDD2 = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply current	I _{DD1}	—	6.0	10.0	mA	F _{MIN} =130MHz, 100mVrms
Quiescent circuit current	I _{DD2}	—	1.0	2.0	mA	No input, PLL=OFF
"H" level input voltage	V _{IH}	4.0	—	—	V	CE, CK, DA terminals
"L" level input voltage	V _{IL}	—	—	1.0	V	CE, CK, DA terminals
"H" level input current 1	I _{IH1}	—	—	1.0	μA	CE, CK, DA terminals V _{IN} =V _{DD}
"H" level input current 2	I _{IH2}	—	0.3	—	μA	XIN terminals V _{IN} =V _{DD}
"H" level input current 3	I _{IH3}	—	6.0	—	μA	FMIN, AMIN, IFIN terminals V _{IN} =V _{DD}
"L" level input current 1	I _{IL1}	-1.0	—	—	μA	CE, CK, DA terminals V _{IN} =V _{SS}
"L" level input current 2	I _{IL2}	—	-0.3	—	μA	XIN terminals V _{IN} =V _{SS}
"L" level input current 3	I _{IL3}	—	-6.0	—	μA	FMIN, AMIN, IFIN terminals V _{IN} =V _{SS}
"L" level output voltage 1	V _{OL1}	—	0.2	0.5	V	P ₀ , P ₁ , P ₂ , P ₃ , DO I _o =1.0mA
"OFF" level leak current 1	I _{OFF1}	—	—	1.0	μA	P ₀ , P ₁ , P ₂ , P ₃ , DO V _o =10V
"L" level output voltage 2	V _{OL2}	—	0.1	0.5	V	FMIN, AMIN, IFIN I _{OUT} =0.1mA
"H" level output voltage	V _{OH}	V _{DD} -1.0	V _{DD} -0.3	—	V	PD1, PD2 I _{OUT} =-1.0mA
"L" level output voltage	V _{OL}	—	0.2	1.0	V	PD1, PD2 I _{OUT} =-1.0mA
"OFF" level leak current 2	I _{OFF2}	—	—	100	nA	PD1, PD2 V _{OUT} =V _{DD}
"OFF" level leak current 3	I _{OFF3}	-100	—	—	nA	PD1, PD2 V _{OUT} =V _{SS}
Internal feedback resistor 1	R _{F1}	—	10	—	MΩ	XIN
Internal feedback resistor 2	R _{F2}	—	500	—	kΩ	FMIN, ANIN, IFIN
Input frequency 1	F _{IN1}	—	7.2	—	MHz	XIN, sine wave, C coupling
Input frequency 2	F _{IN2}	20	—	130	MHz	FMIN, sine wave, C coupling V _{IN} =50mVrms
Input frequency 3	F _{IN3}	0.4	—	30	MHz	AMIN 1, sine wave, C coupling V _{IN} =70mVrms
Input frequency 4	F _{IN4}	0.4	—	16	MHz	IFIN, sine wave, C coupling V _{IN} =70mVrms
Maximum input amplitude	F _{INMAX}	—	—	1.5	Vrms	XIN, FMIN, AMIN, IFIN, sine wave, C coupling
Minimum pulse width	T _W	—	1.0	—	μs	CK, DA
Input rise time	T _R	—	—	500	ns	CE, CK, DA
Input fall time	T _F	—	—	500	ns	CE, CK, DA

●Input data format



D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅
← Input done from D ₀ .															
P ₀	P ₁	P ₂	P ₃	R ₀	R ₁	R ₂	S	CT	L ₀	L ₁	GT	SW	PL	PH	TS

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● Input data format

Explanation of the data

(1) Division data : For D₀ through D₁₅ (When S = 0, use D₄ through D₁₅.)

Example : S = 0, SW = 0

When divided frequency = 1000, the actual set value is 500 since it passes through 1/2 the circuit. This translates to 1F4 (H) in HEX notation, and to (MSB) 0000 0001 1111 0100 (LSB) in binary notation. This data is used from LSB to D₀ through D₁₅.

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅
0	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0

LSB

Example : S = 1, SW = 1

When divided frequency = 1000, the actual set value is 1000 since it does not pass through 1/2 the circuit. This translates to 3E8 (H) in HEX notation, and to (MSB) 0000 0011 1110 1000 (LSB) in binary notation. This data is used from LSB to D₀ through D₁₅.

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅
0	0	0	1	0	1	1	1	1	1	0	0	0	0	0	0

Example : S = 1, SW = 0

When divided frequency = 1000, D₀ through D₃ can be anything since it does not pass through the prescaler. This translates to 3E8 (H) in HEX notation, and to (MSB) 0001 1111 0100 (LSB) in binary notation. This data is used from LSB to D₀ through D₁₅.

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅
X	X	X	X	0	0	0	1	0	1	1	1	1	1	0	0

(2) Output port control data : P₀, P₁, P₂, P₃

- 1 : Nch open drain output ON
- 0 : Nch open drain output OFF

(3) R₀, R₁, R₂, standard frequency data

Data			Standard frequency
R ₀	R ₁	R ₂	
0	0	0	25kHz
0	0	1	12.5kHz
0	1	0	6.25kHz
0	1	1	10kHz
1	0	0	5kHz
1	0	1	9kHz
1	1	0	1kHz
1	1	1	※ PLL OFF

※ FMIN = pulldown, AMIN = pulldown, PD = high impedance

(4) S : switch between FMIN and AMIN

- 0 : FMIN
- 1 : AMIN

(5) CT : Intermediate frequency measurement operation

- 1 : Begins measurement.
- 0 : Resets internal counter, IFIN goes to pull-down.

(6) L₀, L₁ : Setting of IF frequency detection amplitude

S	L ₀	L ₁	Frequency detection amplitude
0	0	0	10.70MHz±20kHz
0	0	1	10.65MHz±20kHz
0	1	0	10.75MHz±20kHz
0	1	1	*
1	0	0	450kHz±2.0kHz
1	0	1	459kHz±2.0kHz
1	1	0	450kHz±0.5kHz
1	1	1	459kHz±0.5kHz

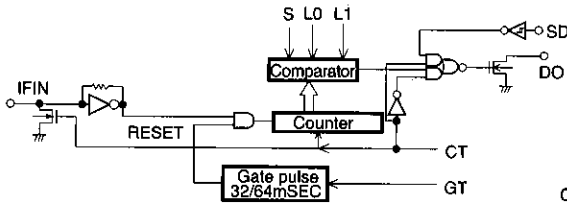
* : Not used.

- (7) GT : Control of frequency measurement time
 0 : 32mSEC
 1 : 64mSEC
- (8) SW : If this bit is set to ON while AMIN is selected, swallow counter division is possible.

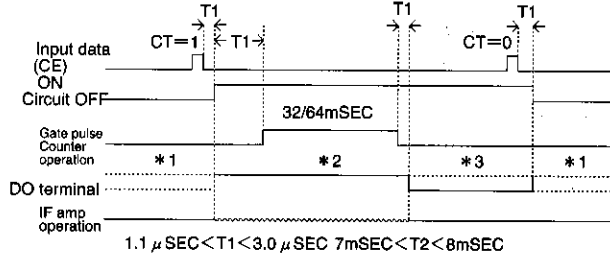
- (9) PL PH : Control of charge pump output
 PL = 0, PH = 0 PD1, PD2 go to PLL operation.
 PL = 1, PH = 0 PD1, PD2 go to LO level.
 PL = 0, PH = 1 PD1, PD2 go to HI level.
 PL = 1, PH = 1 PD1, PD2 go to LO level.
- (10) TS : Test data (0) is input

● Intermediate frequency detection circuit and the DO output terminal

(1) Structure

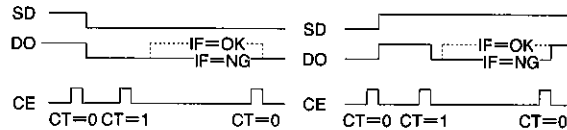
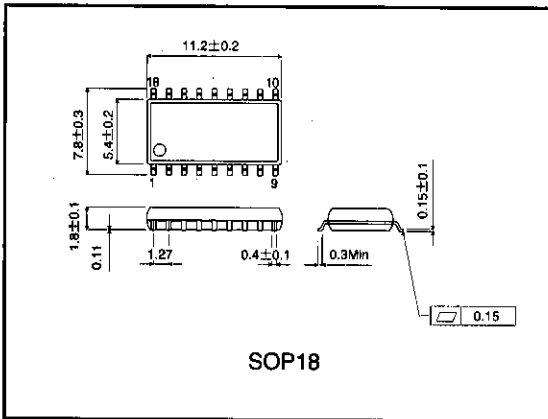


- (2) How the IF frequency detection circuit operates
 When control data CT is set to ON, the counter and the amp go into operation. When CT equals 0, the amp input pulldown counter is reset.



- (3) Explanation of the DO terminal
- *1 When the IF counter is OFF (CT = 0), SD input appears at the DO terminal.
 - *2 When the IF counter is set to ON (CT = 1), the control system keeps it at LO level until the measurement is finished.
 - *3 After the measurement is finished, it goes to HI level if it is within the range of input frequency settings, and is kept at LO level if it is beyond the range of input frequency settings. When CT = 0, it returns to the conditions described under paragraph *1.

● External dimensions (Unit: mm)



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