PLL frequency synthesizer for tuners
BU2622S

The BU2622S is a PLL frequency synthesizer IC designed for use in high-fidelity audio systems, car stereos, and CD radio cassettes. Featuring low power consumption, low superfluous radiation, a frequency measurement counter, and timer output, this chip is ideal for high-performance systems.

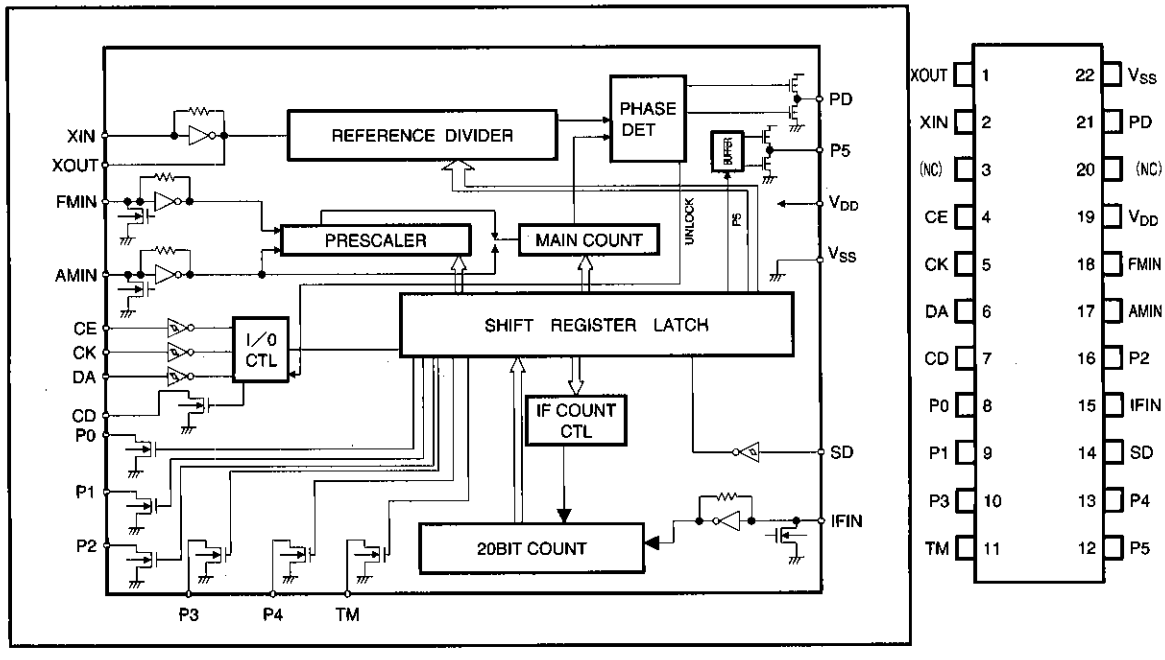
●Applications

Mini components, car stereos, radio cassettes, receivers, and other frequency generating devices

●Features

1) Built-in high-speed prescaler can divide 130MHz VCO.
2) Low power-consumption (during operation : 6.0mA PLL OFF 300 μA Typ.)
3) Seven standard frequencies : 50kHz, 25kHz, 12.5kHz, 10kHz, 9kHz, 5kHz, and 1kHz.
4) Counter for intermediate frequency detection.
5) Unlock detection circuit.
6) Six output ports.
7) SD input.
8) Timer output.
9) Serial data input (CE.CK.DA)

●Block diagram



●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit	Conditions
Supply voltage	V_{DD}	−0.3~7.0	V	V_{DD}
Maximum input voltage 1	V_{IN1}	−0.3~7.0	V	CE, CK, DA, SD
Maximum input voltage 2	V_{IN2}	−0.3~V_{DD}+0.3	V	XIN, FMIN, AMIN, IFIN
Maximum output voltage 1	V_{OUT1}	−0.3~10.0	V	P_0, P_1, P_2, P_3, P_4, TM, CD
Maximum output voltage 2	V_{OUT2}	−0.3~V_{DD}+0.3	V	PD, P_5, XOUT
Maximum output current	I_{OUT}	0~4.0	mA	P_0, P_1, P_2, P_3, P_4, TM, CD
Power dissipation	Pd	450*	mW	
Operating temperature	Topr	−25~75	℃	
Storage temperature	Tstg	−55~125	℃	

* When used with Ta at greater than 25 degrees Celsius, derate the power by 4.5 mW for every degree above 25 degrees.

●Recommended operating conditions (Ta = 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	$V_{DD}1$	4.0	—	6.0	V

●Explanation of terminals

Pin No.	Symbol	Terminal name	Function	I/O
1	XOUT	Crystal oscillation terminal	For generation of standard frequency and internal clock. Connected to 7.2 MHz crystal oscillator.	OUT
2	XIN			IN
3	NC	Unused terminal	Not related to the circuits.	
4	CE	Chip enable	When CE is H, DA is synchronous with the rise of CK and read to the internal shift register. DA is then latched at the timing of the fall of CE. Also, output data is output from the CD terminal synchronous to the rise of CK.	IN
5	CK	Clock signal		
6	DA	Serial data		
7	CD	Count data	Frequency data and unlock data are output.	Nch open drain
8	P0	Output port	Controlled on the basis of input data.	
9	P1			
10	P3			
11	TM	Timer output		
12	P5	Output port	Controlled on the basis of input data.	CMOS/3-state
13	P4			Nch open drain
14	SD	Input port		IN
15	IFIN	IF input	Intermediate frequency input	IN
16	P2	Output port	Controlled on the basis of input data.	Nch open drain
17	AMIN	AM input	Local input for AM	IN
18	FMIN	FM input	Local input for FM	IN
19	V_{DD}	Power supply	Power supply, with 4.0V to 6.0V applied voltage.	
20	NC	Unused terminal	Not related to circuits.	
21	PD	Phase comparison output	High level when value obtained by dividing local output is higher than standard frequency. Low level when value is lower. High impedance when value is same.	3-state
22	V_{SS}	GROUND		

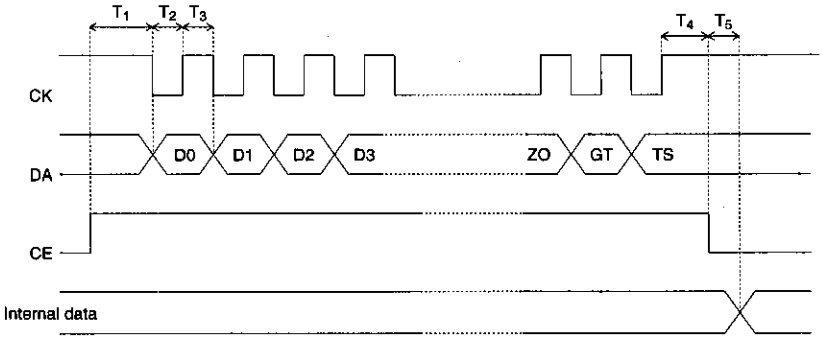
●Electrical characteristics (unless other specified, Ta = 25℃, V_{DD} = 5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply current 1	I_{DD1}	—	6.0	10.0	mA	FM_{IN}=130MHz, 100mVrms
Supply current 2	I_{DD2}	—	0.3	1.0	mA	No input,, PLL=OFF
Quiescent circuit current	V_{IH}	4.0	—	—	V	CE, CK, DA, SD
"H" level input voltage	V_{IL}	—	—	1.0	V	CE, CK, DA, SD
"L" level input voltage	I_{IH1}	—	—	1.0	μA	CE, CK, DA, SD $V_{IN}=V_{DD}$
"H" level input current 1	I_{IH2}	—	0.3	—	μA	XIN $V_{IN}=V_{DD}$
"H" level input current 2	I_{IH3}	—	6.0	—	μA	FMIN, AMIN, IFIN $V_{IN}=V_{DD}$
"H" level input current 3	I_{IL1}	−1.0	—	—	μA	CE, CK, DA, SD $V_{IN}=V_{SS}$
"L" level input current 1	I_{IL2}	—	−0.3	—	μA	XIN $V_{IN}=V_{SS}$
"L" level input current 2	I_{IL3}	—	−6.0	—	μA	FMIN, AMIN, IFIN $V_{IN}=V_{SS}$
"L" level input current 3	V_{OL1}	—	0.2	0.5	V	P_0, P_1, P_2, P_3, P_4, TM, CD I_O=1.0mA
"L" level output voltage 1	I_{OFF1}	—	—	1.0	μA	P_0, P_1, P_2, P_3, P_4, TM, CD V_O=10V
"OFF" level leak current 1	V_{OL2}	—	—	0.3	V	FMIN, AMIN, IFIN I_{OUT}=0.1mA
"L" level output voltage 2	V_{OH}	V_{DD}− 1.0	V_{DD}− 0.25	—	V	PD, P_5 I_{OUT}=−1.0mA
"H" level output voltage	V_{OL4}	—	0.15	1.0	V	PD, P_5 I_{OUT}=1.0mA
"L" level output voltage	I_{OFF2}	—	—	100	nA	PD $V_{OUT}=V_{DD}$
"OFF" level leak current 2	I_{OFF3}	−100	—	—	nA	PD $V_{OUT}=V_{SS}$
"OFF" level leak current 3	R_{F1}	—	10	—	MΩ	XIN
Internal feedback resistor 1	R_{F2}	—	500	—	kΩ	FMIN, AMIN, IFIN
Internal feedback resistor 2	F_{IN1}	—	7.2	—	MHz	XIN, sine wave, C coupling
Input frequency 1	F_{IN2}	10	—	130	MHz	FMIN,sine wave,C coupling V_{IN}=50mVrms
Input frequency 2	F_{IN3}	0.5	—	30	MHz	AMIN,sine wave,C coupling V_{IN}=70mVrms
Input frequency 3	F_{IN4}	0.5	—	15	MHz	AMIF,sine wave,C coupling V_{IN}=50mVrms
Input frequency 4	F_{IN5}	0.4	—	16	MHz	IFIN,sine wave,C coupling V_{IN}=70mVrms
Maximum input amplitude	F_{INMAX}	—	—	1.5	Vrms	XIN,FMIN,AMIN,IFIN,sine wave,C coupling
Minimum pulse width	TW	—	1.0	—	μs	CK, DA
Input rise time	TR	—	—	500	ns	CE, CK, DA
Input fall time	TF	—	—	500	ns	CE, CK, DA

◎ Not designed for radiation resistance.

●Circuit operation

Input data format



$T_1 \geqq 1.5\,\mu SEC$ $T_2, T_3 > 0\,\mu SEC$ $T_4 > 0\,\mu SEC$ $T_5 > 1.5\,\mu SEC$

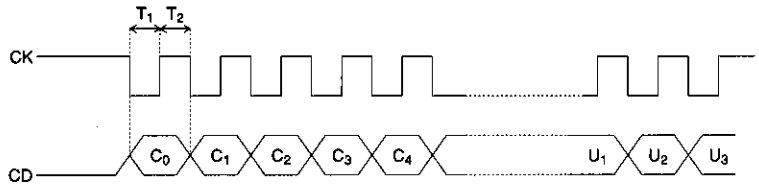
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

← —— Input from D_0.

P_0	P_1	P_2	P_3	P_4	P_5	*	CT	R_0	R_1	R_2	S	PS	Z0	GT	TS

* : (0) is input.

Output data format CE output is set to LO.



Figures for output assume the presence of pullup resistance. $T_1, T_2 > 1\,\mu SEC$

Output data format

C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

C_{16}	C_{17}	C_{18}	C_{19}	U_0	U_1	U_2	U_3

← —— Input done from C_0.

* Data is output only when CT = 1 or GT = 1.

Explanation of the data

(1) Division data : For D_0 through D_{15} (When S = 1, use D_4 through D_{15}.)

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

Examples:

Divided frequency = 1106 (D) ÷2=553 (D) =229 (H) S=0

1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0

Divided frequency = 1107 (D) =453 (H) S=1, PS=1

1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0

Divided frequency = 926 (D) =39E (H) S=1, PS=0

×	×	×	×	0	1	1	1	1	0	0	1	1	1	0	0

(2) CT : Frequency measurement beginning data
1 : Begins measurement.
0 : Resets internal counter, IFIN goes to pull-down.

(3) Output port control data : P_0, P_1, P_2, P_3, P_4, P_5
1 : Open drain output ON (P5 is LO)
2 : Open drain output OFF (P5 is HI)

(4) Z0 : P_5 is set to high impedance.

(5) R_0, R_1, R_2, standard frequency data

Data			Standard frequency
R_0	R_1	R_2	
0	0	0	25kHz
0	0	1	12.5kHz
0	1	0	50kHz
0	1	1	10kHz
1	0	0	5kHz
1	0	1	9kHz
1	1	0	1kHz
1	1	1	* PLL OFF

* FMIN = pulldown, AMIN = pulldown, PD = high impedance

(6) S : switch between FMIN and AMIN
0 : FMIN
1 : AMIN

(7) PS : If this bit is set to ON while AMIN is selected, swallow counter division is possible.

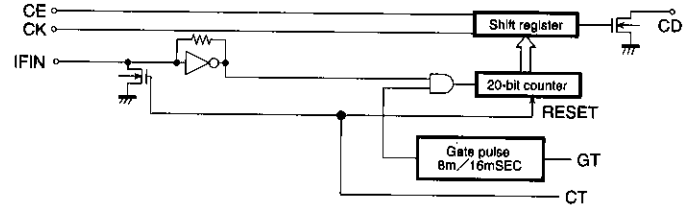
(8) GT : Frequency measurement time and unlock detection ON/OFF

CT	GT	Frequency measurement	Unlock detection	Data output
0	0	OFF	OFF	NG
0	1	OFF	ON	OK
1	0	ON Gate time = 8 mSEC	ON	
1	1	ON Gate time = 16 mSEC	ON	

(9) TS : Test data (0) is input

Frequency counter

(1) Structure



(2) How the frequency counter operates

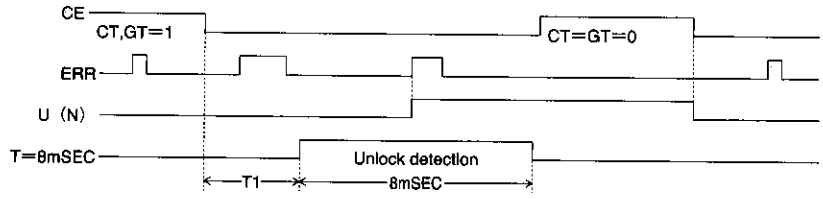
When control data CT equals 1, the 20-bit counter and the amp go into operation. When CT equals 0, amp input goes to pulldown and the counter is reset. Measuring time (gate pulse) is selected (8mSEC/16mSEC) on the basis of control data GT. When control data CT equals 0, the counter is reset.

(3) Explanation of output data

C_0 : LSB C_{19} : MSB

Unlock detection

When control data GT equals 1, or CT equals 1, the unlock detection circuit goes into operation for 8mSEC. When CT equals 1, the unlock detection circuits stops operating before the frequency counter gate pulse is emitted. When CT equals 0, or GT equals 0, the unlock detection circuit is reset.



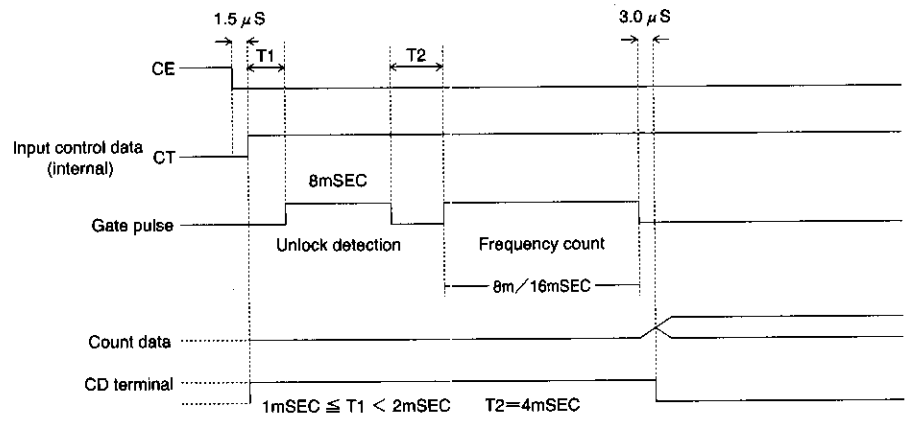
1mSEC≦T1<2mSEC

Explanation of the output data

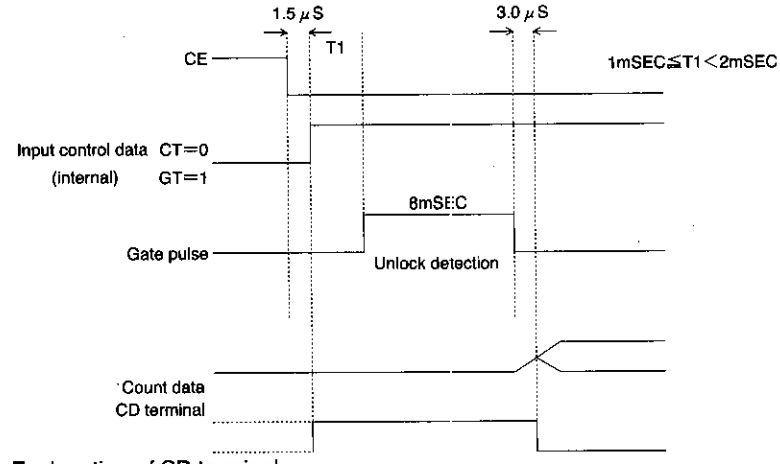
U0	U1	U2	U3					
0	0	0	0			ERR	<	1.1 μSEC
1	0	0	0	1.1 μSEC	<	ERR	<	2.2 μSEC
1	1	0	0	2.2 μSEC	<	ERR	<	3.3 μSEC
1	1	1	0	3.3 μSEC	<	ERR	<	4.4 μSEC
1	1	1	1	4.4 μSEC	<	ERR		

Frequency counter and unlock detection

(1) When CT = 1 : Frequency count and unlock detection are carried out.

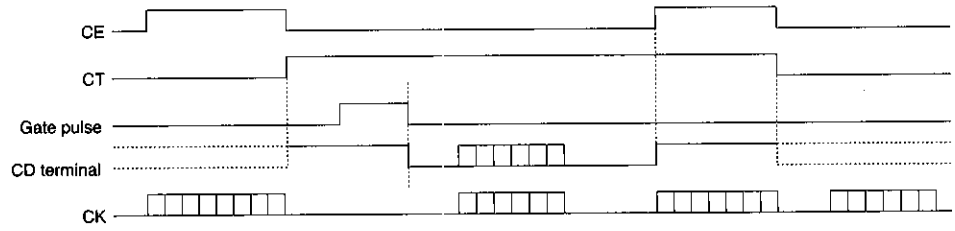


(2) When CT = 0 and GT = 1 : Only unlock detection is carried out.

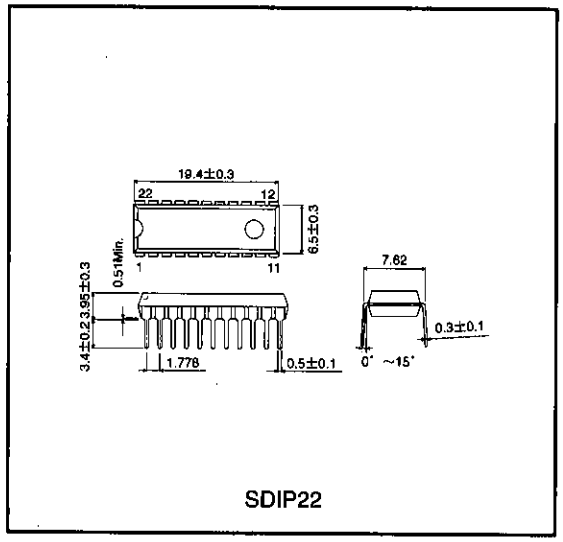


Explanation of CD terminal

While frequency measurement or unlock detection is in progress, the CD terminal goes to HI. When either of these operations finishes, it goes to LO. When the control data is such that CT = 0 and GT = 0, the SD terminal input is displayed in reverse video.



●External dimensions (Unit: mm)



SDIP22

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