PLL frequency synthesizer for tuners
BU2624AF

The BU2624AF is a PLL frequency synthesizer IC designed for use in car stereos, high-fidelity audio systems, and CD radio cassettes.
Featuring low current dissipation, low superfluous radiation, two frequency measurement counter systems, and two phase comparison outputs, this chip is ideal for high-performance multi-band systems.

●Applications
Car stereos, high-fidelity audio systems, radio cassettes, receivers, and other frequency generating devices

●Features
1) Built-in high-speed prescaler can divide 130MHzVCO.
2) Low current dissipation (during operation: 6.0mA, PLL OFF: 300μA Typ.)
3) Seven standard frequencies: 50kHz, 25kHz, 12.5kHz, 10kHz, 9kHz, 5kHz, and 1kHz.
4) Two counters for intermediate frequency detection
5) Unlock detection circuit
6) Five output ports (open drain)
7) SD input port
8) Two charge pump outputs
9) Serial data input (CE, CK, DA)
10) Control of phase comparison output

●Absolute maximum ratings (Ta = 25°C)

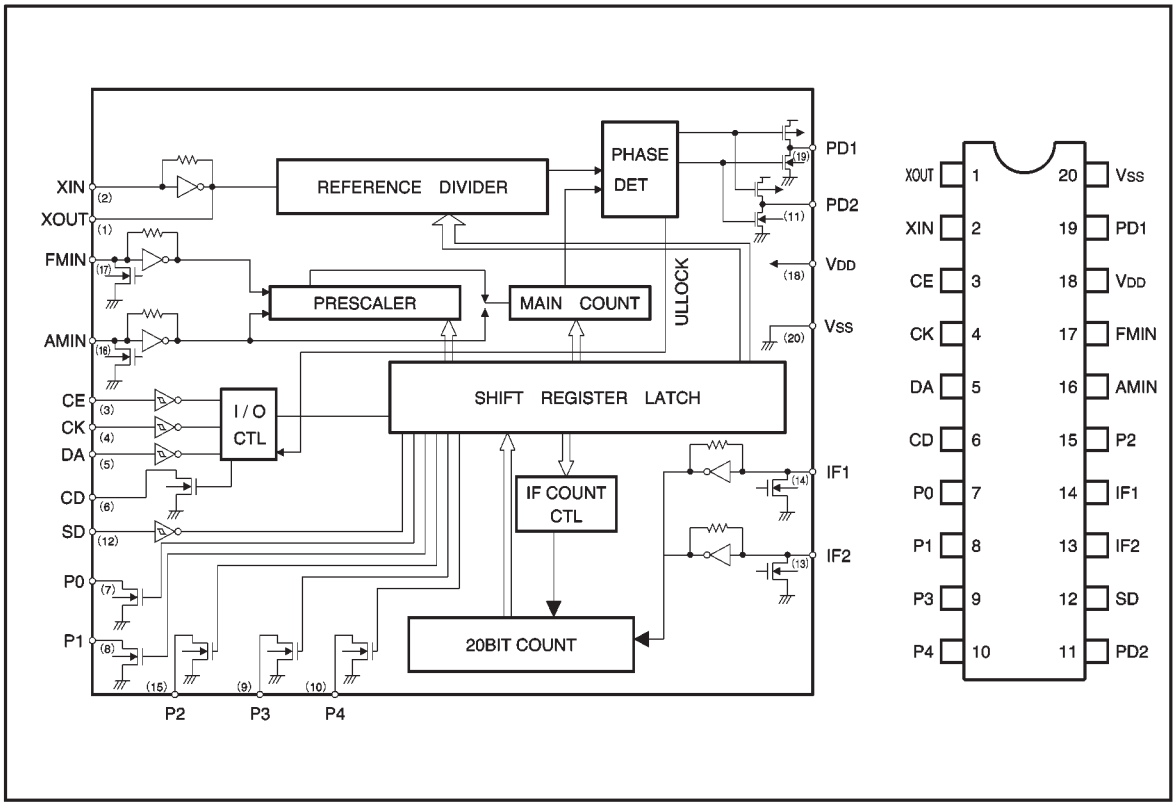
Parameter	Symbol	Limits	Unit	Conditions
Power supply voltage	V_{DD}	−0.3～+7.0	V	V_{DD}
Maximum input voltage 1	V_{IN1}	−0.3～+7.0	V	CE,CK,DA,SD
Maximum input voltage 2	V_{IN2}	−0.3～V_{DD}+0.3	V	XIN,FMIN,AMIN,IF1,IF2,SD
Maximum output voltage 1	V_{OUT1}	−0.3～+10.0	V	P0, P1, P2, P3, P4, CD
Maximum output voltage 2	V_{OUT2}	−0.3～V_{DD}+0.3	V	PD1, PD2, XOUT
Maximum output current	I_{OUT}	0～4.0	mA	P0, P1, P2, P3, P4, CD
Power dissipation	Pd	450*	mW	
Operating temperature	Topr	−40～+85	℃	
Storage temperature	Tstg	−55～+125	℃	

* Reduced by 0mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.0	—	6.0	V

●Block diagram



●Pin descriptions

Pin No.	Symbol	Pin name	Function	I / O
1	XOUT	Crystal oscillation	For generation of standard frequency and internal clock. Connected to 7.2 MHz crystal resonator.	OUT
2	XIN			IN
3	CE	Chip enable Clock signal Serial data	When CE is H, DA (which is generated when CK starts) goes to the internal shift register, and is latched according to the timing of CE shutdown. Also, output data is generated from the CD terminal when CK starts up.	IN
4	CK			
5	DA			
6	CD	Count data	Frequency data and unlock data are output.	Nch open drain
7	P0	Output port	Controlled on the basis of input data.	
8	P1			
9	P3			
10	P4			
11	PD2	Phase comparison output	Operates in the same ways as PD1	3-state
12	SD	Input port	Output to the CD.	Schmidt input
13	IF2	IF2 input	Intermediate frequency input Selected on the basis of input data.	IN
14	IF1	IF1 input		
15	P2	Output port	Controlled on the basis of input data.	Nch open drain
16	AMIN	AM input	Local input for AM	IN
17	FMIN	FM input	Local input for FM	IN
18	V_{DD}	Power supply	Power supply, with 4.0V to 6.0V applied voltage.	
19	PD1	Phase comparison output	High level when value obtained by dividing local output is higher than standard frequency. Low level when value is lower. High impedance when value is same.	3-state
20	V_{SS}	GROUND		

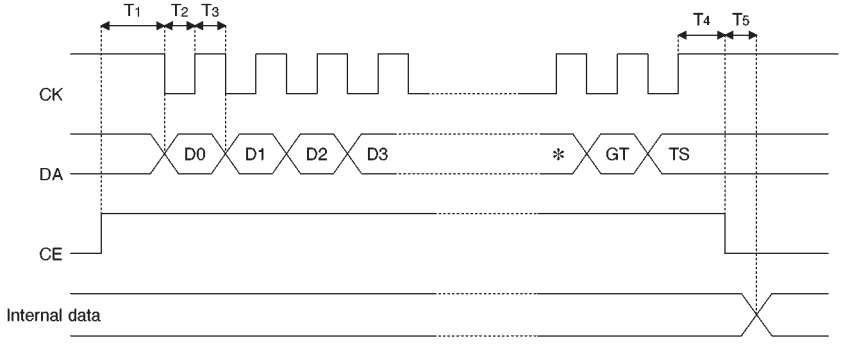
●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply current 1	I_{DD1}	—	6.0	10.0	mA	FM_{IN}=130MHz, 100mV_{rms}
Quiescent current	I_{DD2}	—	0.3	1.0	mA	No input, PLL=OFF
Input high level voltage	V_{IH}	0.8V_{DD}	—	—	V	CE, CK, DA, SD
Input low level voltage	V_{IL}	—	—	0.2V_{DD}	V	CE, CK, DA, SD
Input high level current 1	I_{IH1}	—	—	1.0	μA	CE, CK, DA, SD V_{IN}=V_{DD}
Input high level current 2	I_{IH2}	—	0.3	—	μA	XIN V_{IN}=V_{DD}
Input high level current 3	I_{IH3}	—	6.0	—	μA	FMIN, AMIN, IF1, IF2 V_{IN}=V_{DD}
Input low level current 1	I_{IL1}	−1.0	—	—	μA	CE, CK, DA, SD V_{IN}=V_{SS}
Input low level current 2	I_{IL2}	—	−0.3	—	μA	XIN V_{IN}=V_{SS}
Input low level current 3	I_{IL3}	—	−0.6	—	μA	FMIN, AMIN, IF1, IF2 V_{IN}=V_{SS}
Output low level voltage 1	V_{OL1}	—	0.2	0.5	V	P0, P1, P2, P3, P4, CD I_O=1.0mA
Off level leakage current 1	I_{OFF1}	—	—	1.0	μA	P0, P1, P2, P3, P4, CD V_O=10V
Output low level voltage 2	V_{OL2}	—	—	0.3	V	FMIN, AMIN, IF1, IF2 I_{OUT}=0.1mA
Output high level voltage	V_{OH}	V_{DD} 1.0	V_{DD} 0.25	—	V	PD1, PD2 I_{OUT}=−1.0mA
Output low level voltage 3	V_{OL3}	—	0.15	1.0	V	PD1, PD2 I_{OUT}=1.0mA
Off level leakage current 2	I_{OFF2}	—	—	100	nA	PD1, PD2 V_{OUT}=V_{DD}
Off level leakage current 3	I_{OFF3}	−100	—	—	nA	PD1, PD2 V_{OUT}=V_{SS}
Internal feedback resistor 1	R_{F1}	—	10	—	MΩ	XIN
Internal feedback resistor 2	R_{F2}	—	500	—	kΩ	FMIN, AMIN, IF1, IF2
Input frequency 1	F_{IN1}	—	7.2	—	MHz	XIN, Sine wave, C coupling
Input frequency 2	F_{IN2}	10	—	130	MHz	FMIN, Sine wave, C coupling V_{IN}=50mV_{rms}
Input frequency2-1	F_{IN2-1}	20	—	180	MHz	FMIN, Sine wave, C coupling V_{IN}=100mV_{rms}
Input frequency 3	F_{IN3}	0.5	—	30	MHz	AMIN, Sine wave, C coupling V_{IN}=70mV_{rms}
Input frequency 4	F_{IN4}	0.4	—	16	MHz	IF1, IF2, Sine wave, C couplingV_{IN}=70mV_{rms}
Input amplitude 1	F_{IN1}	50	—	1.5	V_{rms}	FMIN, Sine wave, C coupling 10～130MHz
Input amplitude 1-2	F_{IN1-2}	100	—	1.5	V_{rms}	FMIN, Sine wave, C coupling 130～180MHz
Input amplitude 2	F_{IN2}	70	—	1.5	V_{rms}	AMIN, IF1, IF2, Sine wave, C coupling
Minimum pulse width	TW	1.0	—	—	μs	CK, DA
Input rise time	TR	—	—	500	ns	CE, CK, DA
Input fall time	TF	—	—	500	ns	CE, CK, DA

◎Not designed for radiation resistance.

●Circuit operation

Input data format



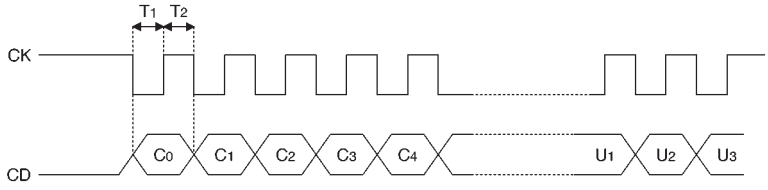
$T_1 \geqq 1.5\,\mu s$ $T_2,\ T_3 > 1\,\mu s$ $T_4 > 0\,\mu s$ $T_5 < 1.5\,\mu s$

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

← Input from D0.

P_0	P_1	P_2	P_3	P_4	PH	PL	CT	R_0	R_1	R_2	S	PS	IFS	GT	TS

Output data format CE output is set to LO.



Figures for output assume the presence of pullup resistance. $T_1,\ T_2 > \mu s$

Output data format

C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

← Input done from C_0.

C_{16}	C_{17}	C_{18}	C_{19}	U_0	U_1	U_2	U_3

✻ Data is output only when CT = 1 or GT = 1.

Explanation of the data

(1) Division data: For D_0 through D_{15} (When S = 1, use D_4 through D_{15}.)

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

Examples:

Divide ratio=1106(D) 1106(D)÷2=553(D)=229(H) S=0

1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0

Divide ratio=1107(D)=453(H) S=1, PS=1

1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0

Divide ratio=926(D)=39E(H) S=1, PS=0

×	×	×	×	0	1	1	1	1	0	0	1	1	1	0	0

(2) CT: Frequency measurement beginning data 1: Begins measurement.
0: Resets internal counter, IF1 and IF2 go to pul down.

(3) Output port control data: P0, P1, P2, P3, P4

(4) PL PH: Control of charge pump output
PH = 0, PL = 0 PLL operation
PH = 0, PL = 1 PD1 PD2 LO level
PH = 1, PL = 0 PD1 PD2 HI level
PH = 1, PL = 1 PD1 PD2 LO level

(5) R_0, R_1, R_2, standard frequency data

Data			
R_0	R_1	R_2	Standard frequency
0	0	0	25kHz
0	0	1	12.5kHz
0	1	0	50kHz
0	1	1	10kHz
1	0	0	5kHz
1	0	1	9kHz
1	1	0	1kHz
1	1	1	✻ PLL OFF

✻ FMIN = pulldown, AMIN = pulldown, PD = high impedance

(6) S: switch between FMIN and AMIN 0: FMIN 1: AMIN

(7) PS: If this bit is set to ON while AMIN is selected, swallow counter division is possible.

(8) IFS: Selection between IF1 and IF2 during IF count 0: IF1 1: IF2

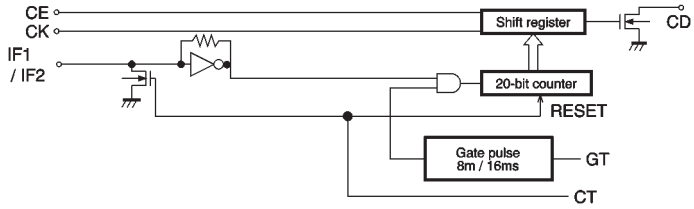
(9) GT: Frequency measurement time and unlock detection ON/OFF

CT	GT	Frequency measurement	Unlock detection	Data output
0	0	OFF	OFF	NG
0	1	OFF	ON	OK
1	0	ON Gate time = 8 ms	ON	
1	1	ON Gate time = 16 ms	ON	

(10) TS: Test data (0) is input

Frequency counter

(1) Structure



(2) How the frequency counter operates

When control data CT equals 1, the 20-bit counter and the amp go into operation. When CT equals 0, amp input goes to pulldown and the counter is reset.

Measuring time (gate pulse) is selected (8 ms / 16 ms) on the basis of control data GT.

When control data CT equals 0, the counter is reset.

(3) Explanation of output data

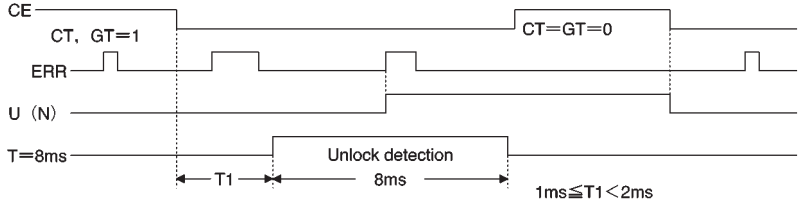
D0: LSB D19: MSB

Unlock detection

When control data GT equals 1, or CT equals 1, the unlock detection circuit goes into operation for 8ms.

When CT equals 1, the unlock detection circuits stops operating before the frequency counter gate pulse is emitted.

When CT equals 0, or GT equals 0, the unlock detection circuit is reset.

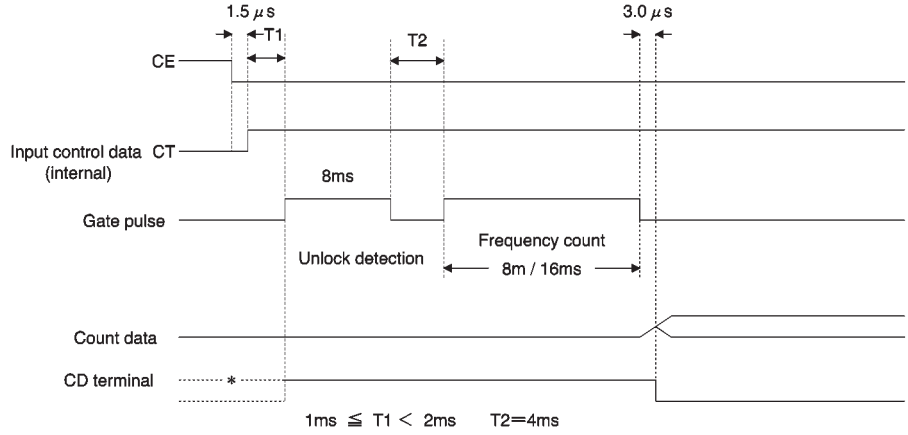


Explanation of the output data

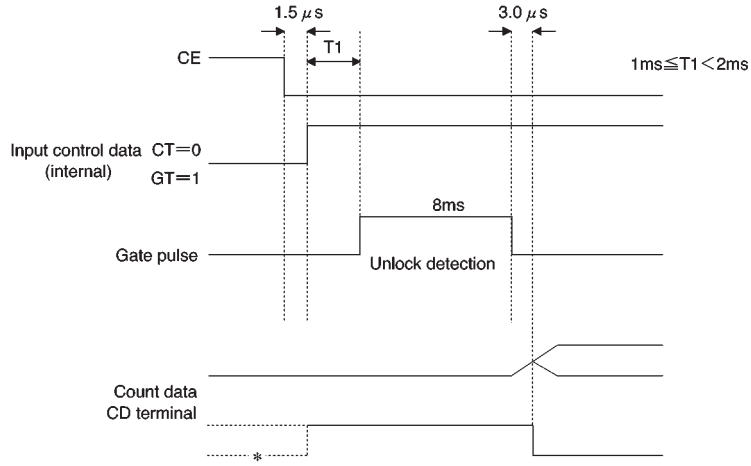
U0	U1	U2	U3					
0	0	0	0			ERR	<	1.1 μs
1	0	0	0	1.1 μs	<	ERR	<	2.2 μs
1	1	0	0	2.2 μs	<	ERR	<	3.3 μs
1	1	1	0	3.3 μs	<	ERR	<	4.4 μs
1	1	1	1	4.4 μs	<	ERR		

Frequency counter and unlock detection

(1) When CT = 1: Frequency count and unlock detection are carried out.



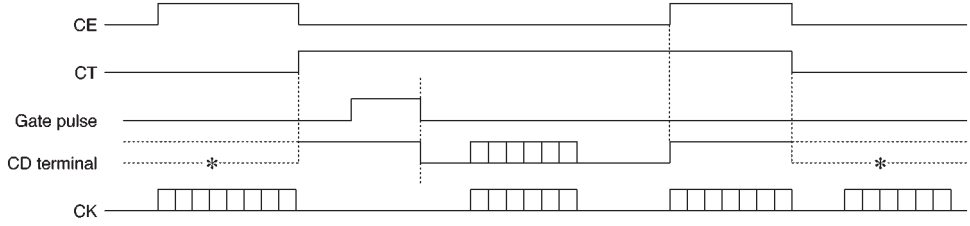
(2) When CT = 0 and GT = 1: Only unlock detection is carried out.



Explanation of CD terminal

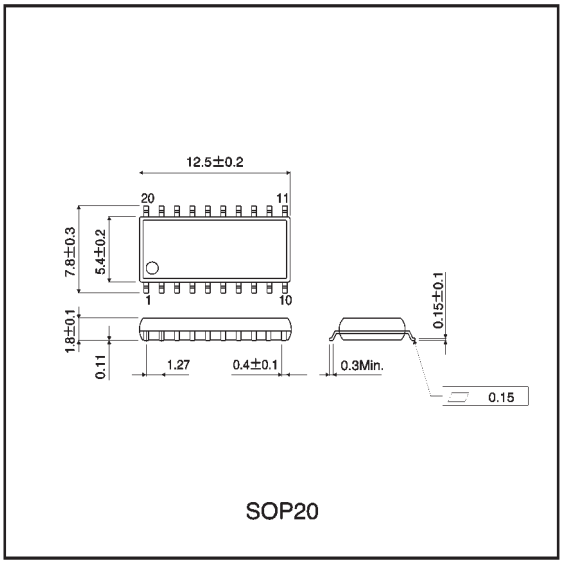
When frequency measurement or unlock detection is finished, the CD terminal goes to LO to indicate that the count and unlock detection have finished.

It also synchronizes with CK to output counter data. When the next data is input, it goes to HI.



* : When CT or GT = 0, the logic for the SD (12-pin) terminal is displayed.

●External dimensions (Units: mm)



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