Picture cell driver for STN (LCD driver) for low voltage power supplies

BU9718KV

The BU9718KV is a driver IC designed for the character-type STN liquid crystal panels which are ideal for applications such as portable devices. The number of display segments includes 32 output segments and 3 common outputs, enabling drive of up to 96 segments. A compact 48-pin QFP package with a pitch of 0.5mm is used, enabling compact size for the set as a whole.

●Applications

Portable terminals (POS, ECR, PDA, and others), movie projectors, cameras, telephones (cordless handheld telephone units), and others Low-voltage power supply sets

●Features

1) Operates on 3V power supply.
2) Low current consumption. (0.1 μA in low power mode (actual value))
3) Compact package. (molded section is 7.0mm□)
4) Up to 32 segment output pins and 3 common output pins are provided, enabling a total display of up to 96 segments.
5) 1/3 duty display.
6) Either 1/2 or 1/3 bias can be selected for power supply for LCD display.

●Absolute maximum ratings (Ta=25℃, V_{SS}=0V)

Parameter	Symbol	Pin	Limits	Unit
Power supply voltage *1	V_{DD}	V_{DD}	−0.3~7.0	V
Input voltage *1	V_{IN}	OSC, CS, CK, DI, RES	−0.3~V_{DD}+0.3	V
Output voltage *1	V_{OUT}	OSC	−0.3~V_{DD}+0.3	V
Output current	I_{SO}	S_1~S_{32}	300	μA
	I_{CO}	COM_1~COM_3	3	mA
Power dissipation	Pd	—	400 *2	mW
Storage temperature	Tstg	—	−55~125	℃

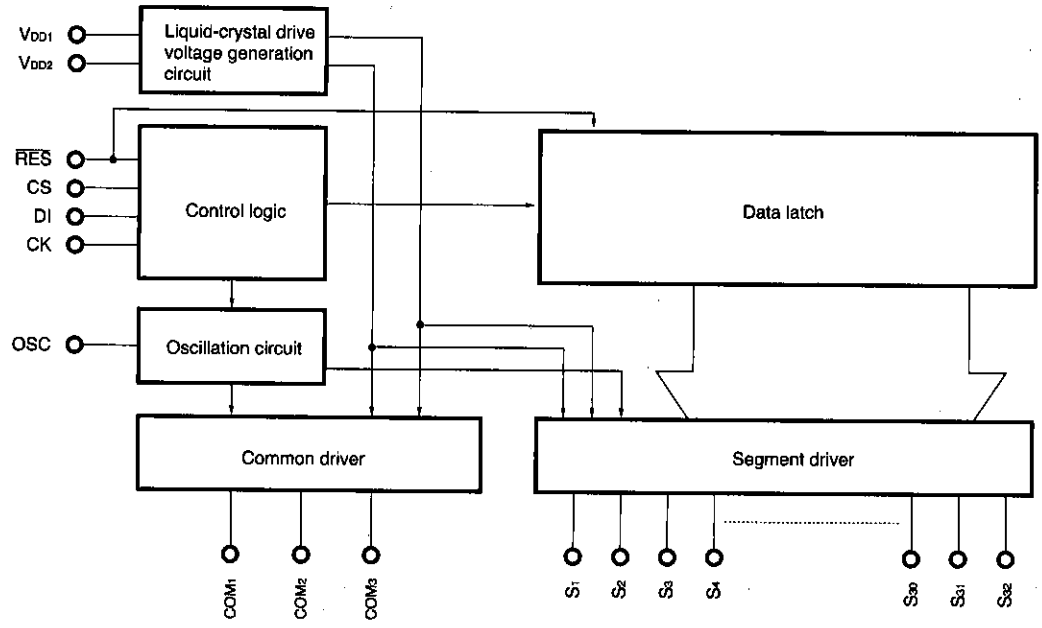
*1 Max. voltage that can be applied with a Vss pin
*2 When using at temperatures of Ta=25 ℃ or higher, reduce power by -4.0 mW for each 1℃ above 25℃.

●Recommended operating conditions (Ta=25℃)

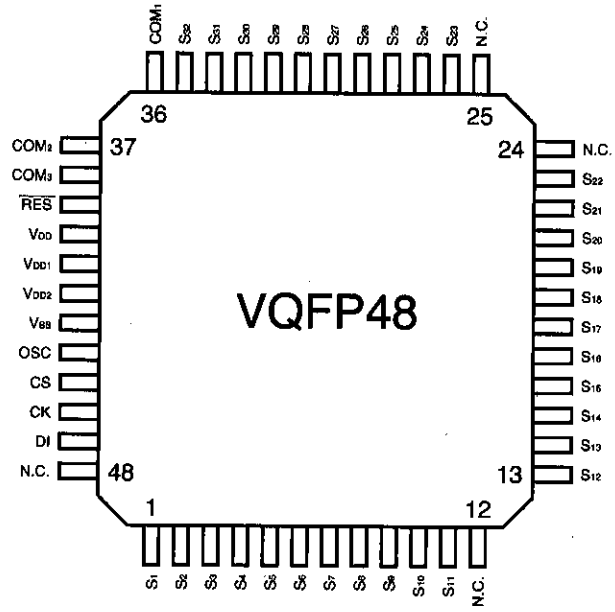
Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit
Power supply voltage*	V_{DD}	V_{DD}	2.7	—	3.5	V
Input voltage*	V_{DD1}	V_{DD1}	0	2/3 V_{DD}	V_{DD}	V
	V_{DD2}	V_{DD2}	0	1/3 V_{DD}	V_{DD}	V
Oscillation freq., with external input	fosc	OSC	—	38	100	kHz
External resistance	R	OSC	—	47	—	kΩ
External capacitance	C	OSC	—	1000	—	pF
Operating temperature	Topr	—	−40	—	85	℃

* Indicates the max. voltage that can be applied with a Vss pin.

●Block diagram



●Pin layout



●Pin descriptions

Pin No.	Name	I/O	Function	Processing when not in use
1—11 13—23 26—35	S_1—S_{11} S_{12}—S_{22} S_{23}—S_{32}	O	Segment data output pin; outputs LCD drive voltage that matches COM_1 - COM_3 compatible data	OPEN
36 37 38	COM_1 COM_2 COM_3	O	Common drive output; frame freq. fc = (fosc/384) Hz	V_{SS}
39	$\overline{RES}$	I	Reset input; when $\overline{RES}$ = L, resets internal data (include. control data)	V_{DD}
44	OSC	—	Oscillation pin (for common, segment alternation waves)	V_{SS}
45	CS	I	Chip segment input; when CS = H, data can be transferred	V_{SS}
46	CK	I	Synchronous clock input for serial data transfer	V_{SS}
47	DI	I	Serial data input	V_{SS}
41	V_{DD1}	—	Internal standard voltage for liquid-crystal drive; when using 1/2 bias mode, connects to V_{DD2}	OPEN
42	V_{DD2}	—	Internal standard voltage for liquid-crystal drive; when using 1/2 bias mode, connects to V_{DD1}	OPEN

●Electrical characteristics (Unless otherwise noted, Ta=25℃, V_{DD}=2.7V to 3.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Pin
"H" level input voltage	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	—	CS, CK, DI, $\overline{RES}$
"L" level input voltage	V_{IL}	0	—	0.2 V_{DD}	V	—	CS, CK, DI, $\overline{RES}$
"H" level input current	I_{IH}	0	—	6.0	μA	V_I=V_{DD}	CS, CK, DI, $\overline{RES}$
"L" level input current	I_{IL}	0	—	6.0	μA	V_I=V_{SS}	CS, CK, DI, $\overline{RES}$
"H" level output voltage	V_{SOH}	—	V_{DD}−1.0	—	V	I_O=−20 μA	S_1~S_{32}
	V_{COH}	—	V_{DD}−1.0	—	V	I_O=−100 μA	COM_1~COM_3
"L" level output voltage	V_{SOL}	—	1.0	—	V	I_O=20 μA	S_1~S_{32}
	V_{COL}	—	1.0	—	V	I_O=100 μA	COM_1~COM_3
Medium-level output voltage	V_{CM1}	—	1/2 V_{DD} ±1.0	—	V	1/2bias	COM_1~COM_3
	V_{SM1}	—	2/3 V_{DD} ±1.0	—	V	1/3bias	S_1~S_{32}
	V_{CM2}	—	2/3 V_{DD} ±1.0	—	V	1/3bias	COM_1~COM_3
	V_{SM2}	—	1/3 V_{DD} ±1.0	—	V	1/3bias	S_1~S_{32}
	V_{CM3}	—	1/3 V_{DD} ±1.0	—	V	1/3bias	COM_1~COM_3
Power supply current	I_Q	—	0.1	30	μA	Low-power mode	—
	I_{DD}	—	100	300	μA	fosc=38kHz	—

●AC characteristics (Unless otherwise noted, Ta=25℃, V_{DD}=2.7V to 3.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Pin
Guaranteed oscillation range	fosc	10	38	80	kHz	C=1000pF R=47kΩ	OSC
Operating frequency	fosc	—	—	100	kHz	External input	OSC
Data set-up time	tDS	200	—	—	ns		CK, DI
Data hold time	tDH	200	—	—	ns		CK, DI
CS set-up time	tCS	200	—	—	ns		CS, CK
CS hold time	tCH	200	—	—	ns		CS, CK
CK "H" level pulse width	tCKH	200	—	—	ns		CK
CK "L" level pulse width	tCKL	200	—	—	ns		CK
Rise time	tr	—	—	100	ns		CS, CK, DI
Fall time	tf	—	—	100	ns		CS, CK, DI

●AC timing waveform

1. When CK is stopped at "L"

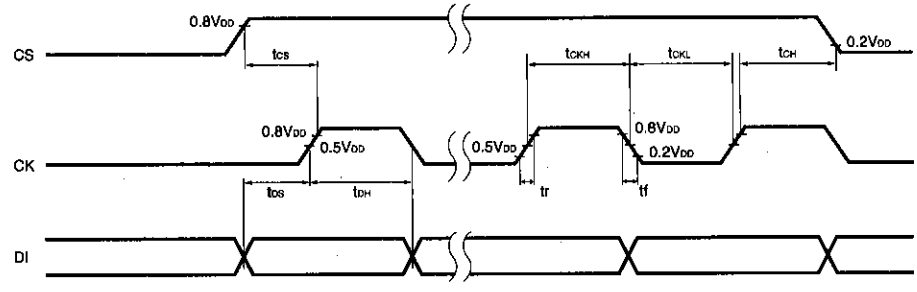


Fig.1

2. When CK is stopped at "H"

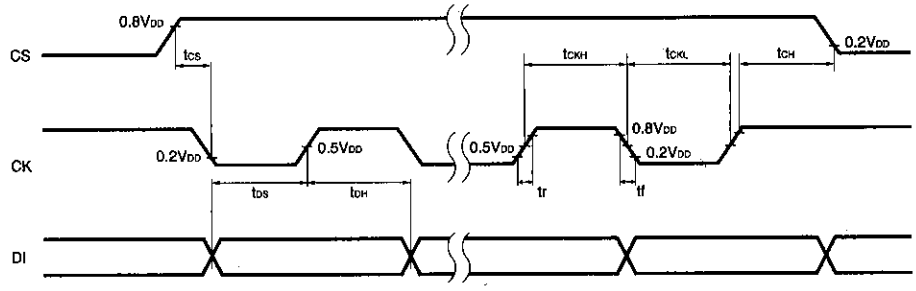


Fig.2

●Timing charts

1. When CK is stopped at "L"

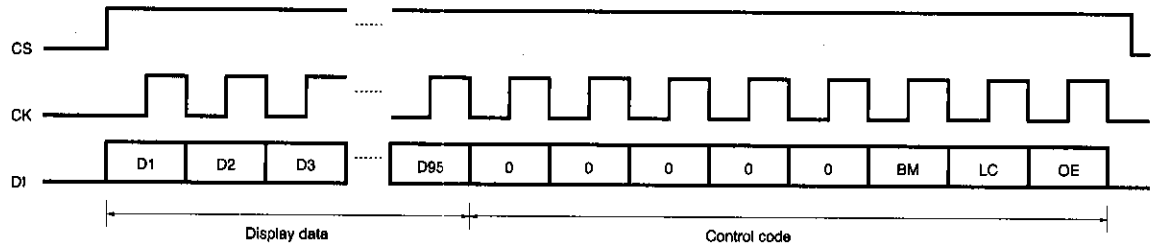


Fig.3

When CS is HIGH, data can be transferred. Data is sent to the shift register at the rising edge of CK. After all of the DI data has been transferred, CS should be set to LOW. The voltage corresponding to the display data transferred at the falling edge of CS is output.

2. When CK is stopped at "H"

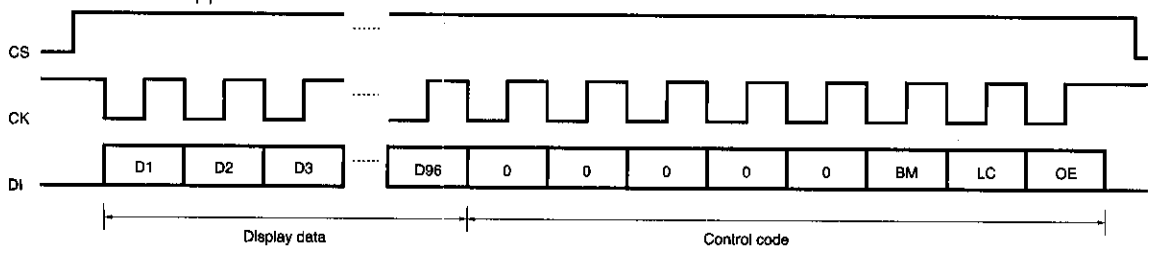


Fig.4

●Control code table

OE	Output enable control
0	Normal operation
1	No display; all display data = 0 (internal oscillation circuit is operating)

LC	Low-power mode control
0	Normal operation
1	Low-power mode = internal oscillation circuit has stopped; segment and common output = 0

BM	Bias mode control
0	1/3 bias
1	1/2 bias

●Correspondence between display data input and segments Segment

Segment	COM_3	COM_2	COM_1
S_1	D_1	D_2	D_3
S_2	D_4	D_5	D_6
S_3	D_7	D_8	D_9
S_4	D_{10}	D_{11}	D_{12}
S_5	D_{13}	D_{14}	D_{15}
S_6	D_{16}	D_{17}	D_{18}
S_7	D_{19}	D_{20}	D_{21}
S_8	D_{22}	D_{23}	D_{24}
S_9	D_{25}	D_{26}	D_{27}
S_{10}	D_{28}	D_{29}	D_{30}
S_{11}	D_{31}	D_{32}	D_{33}
S_{12}	D_{34}	D_{35}	D_{36}
S_{13}	D_{37}	D_{38}	D_{39}
S_{14}	D_{40}	D_{41}	D_{42}
S_{15}	D_{43}	D_{44}	D_{45}
S_{16}	D_{46}	D_{47}	D_{48}
S_{17}	D_{49}	D_{50}	D_{51}
S_{18}	D_{52}	D_{53}	D_{54}
S_{19}	D_{55}	D_{56}	D_{57}
S_{20}	D_{58}	D_{59}	D_{60}
S_{21}	D_{61}	D_{62}	D_{63}
S_{22}	D_{64}	D_{65}	D_{66}
S_{23}	D_{67}	D_{68}	D_{69}
S_{24}	D_{70}	D_{71}	D_{72}
S_{25}	D_{73}	D_{74}	D_{75}
S_{26}	D_{76}	D_{77}	D_{78}
S_{27}	D_{79}	D_{80}	D_{81}
S_{28}	D_{82}	D_{83}	D_{84}
S_{29}	D_{85}	D_{86}	D_{87}
S_{30}	D_{88}	D_{89}	D_{90}
S_{31}	D_{91}	D_{92}	D_{93}
S_{32}	D_{94}	D_{95}	D_{96}

●Output waveforms

COM1

COM2

COM3

LCD driver output, when all LCD segments for COM1, 2 and 3 are out

LCD driver output, when only the LCD segment for COM1 is lit up

LCD driver output, when only the LCD segment for COM2 is lit up

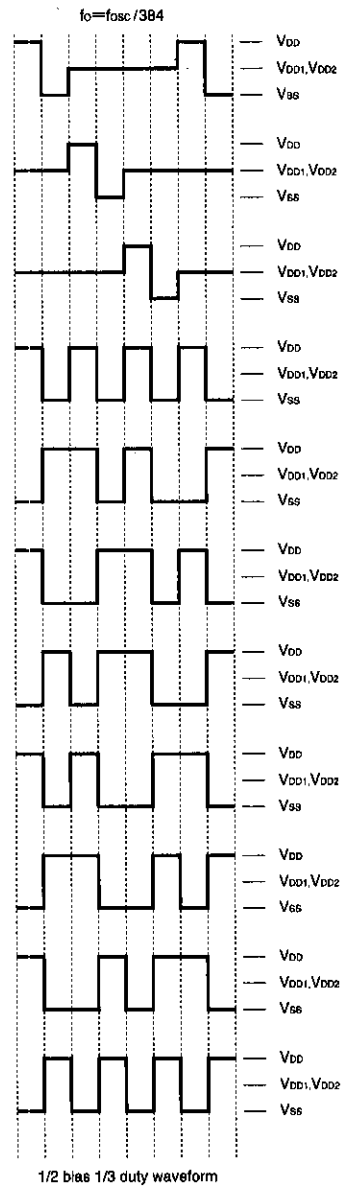
LCD driver output, when the LCD segments for COM1 and 2 are lit up

LCD driver output, when the LCD segment for COM3 is lit up

LCD driver output, when the LCD segments for COM1 and 3 are lit up

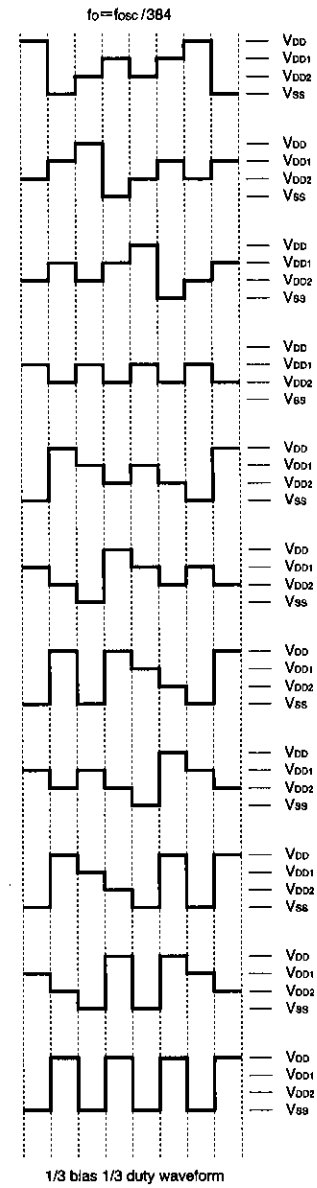
LCD driver output, when the LCD segments for COM2 and 3 are lit up

LCD driver output, when the all LCD segments for COM1, 2 and 3 are lit up



1/2 bias 1/3 duty waveform

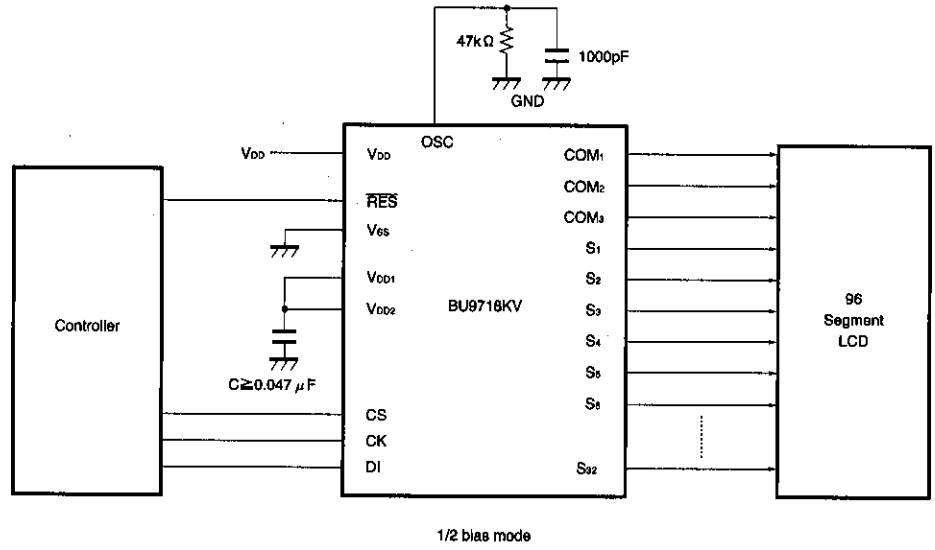
Fig.5



1/3 bias 1/3 duty waveform

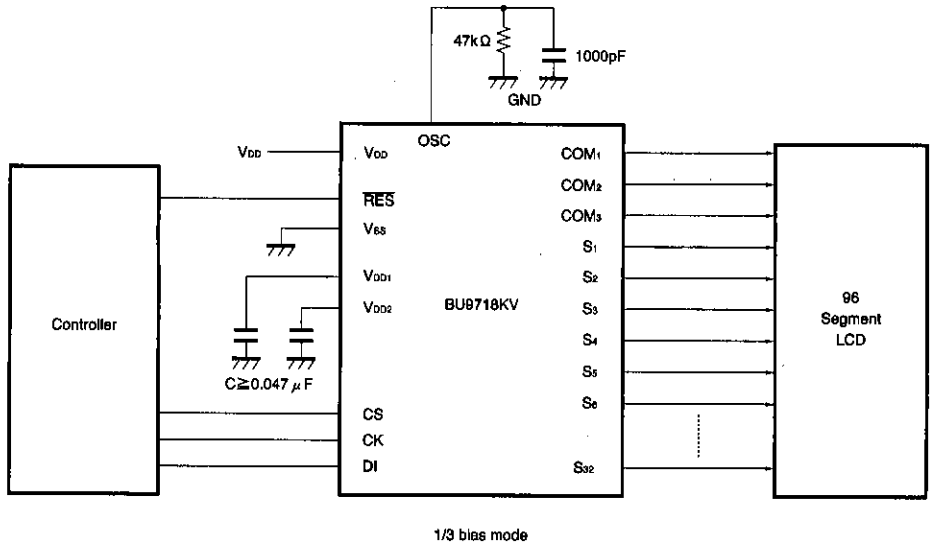
Fig.6

●Recommended Circuit Example 1



1/2 bias mode

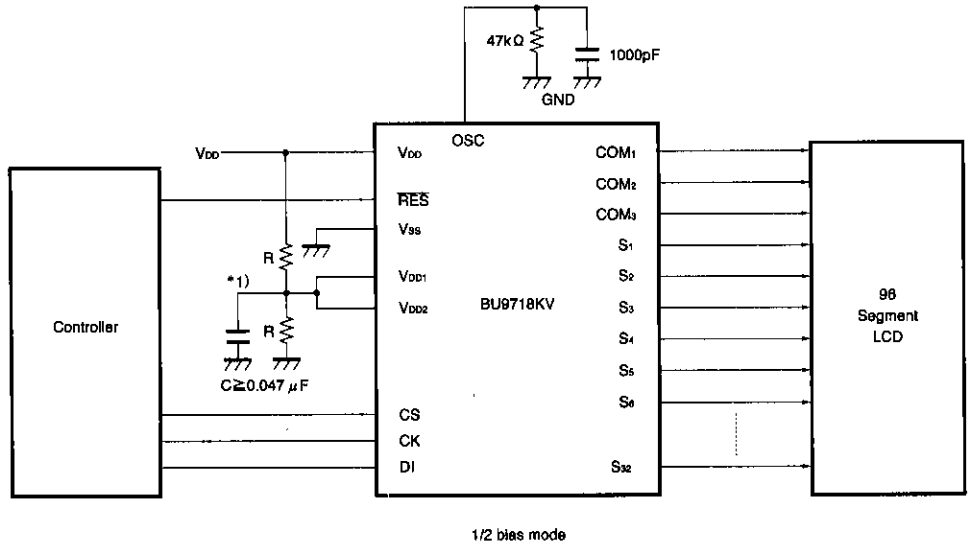
Fig.7



1/3 bias mode

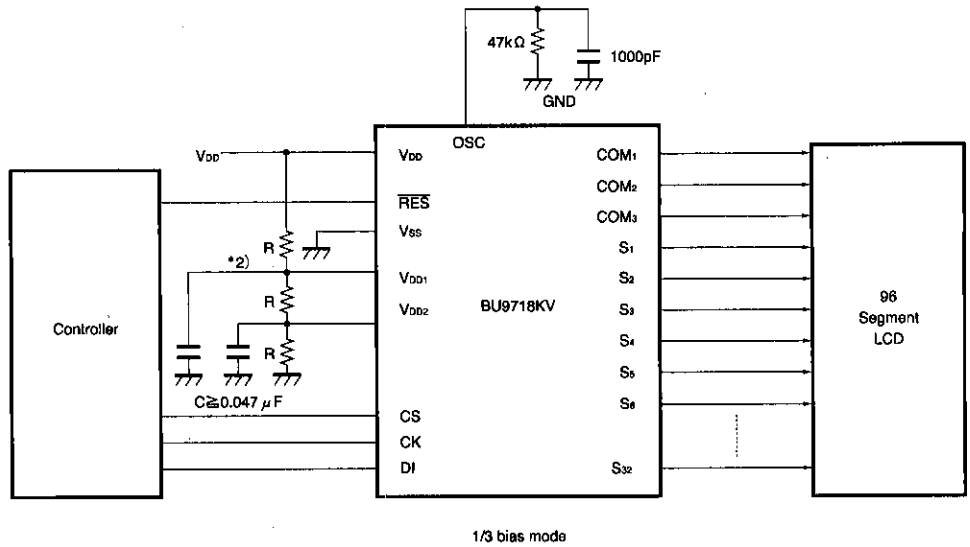
Fig.8

●Recommended Circuit Example 2



1/2 bias mode

Fig.9

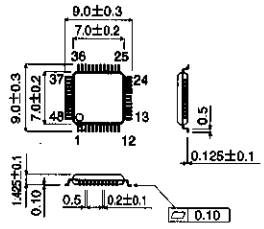


1/3 bias mode

Fig.10

Note: The resistance values and capacitance for *1 and *2 should be set to match the LCD panel, and should be checked using test operation.

●External dimensions (Units: mm)



VQFP48

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