Product Brief

C-3e NETWORK PROCESSOR

MOTOROLA
intelligence everywhere™

Freescale Semiconductor, Inc.

FEATURES

- *Operating frequency of 180MHz with power consumption 5.5W at 1.2V typical*
- *3Gbps of bandwidth and more than 3000 MIPs of computing power*
- *Highly-integrated 728 pin Ball Grid Array (BGA) package*
- *17 programmable RISC Cores for cell/packet forwarding*
- *32 programmable Serial Data Processors for processing bit streams*
- *Best-in-class, on-chip classification coprocessor supporting over 42 million IPv4 lookups/second*
- *Flexible interfaces supporting virtually any protocol and individual port data rate from DS1 (1.544Mbps) to Gigabit Ethernet*
- *External Traffic Management Coprocessors for advanced QoS*
- *Simple and efficient programming in C-language with robust APIs*

As more and more intelligent services are being deployed at the access area of the network, network equipment vendors are seeking more programmable and easy to develop solutions for implementing these services. The **C-3e™ Network Processor (NP)** is a highly integrated, flexible, and functionally-rich processor that extends the reach of the C-Port™ network processor family to lower bandwidth, lower power access applications.

With its 3Gbps of bandwidth and more than 3000 MIPs of computing power, the C-3e NP more than satisfies the demanding communications requirements for intelligent access network services, such as classification, traffic management, and interworking functions. Like the other members of the C-Port family, the C-3e NP provides complete programmability of forwarding plane tasks using a standard Applications Programming Interface (API) and C programming languages. Consequently, the C-3e NP is fully software compatible with the C-Port family, enabling a common programming model across a vast range of bandwidth options.

The C-3e NP is backed by a comprehensive development environment and third-party support from Motorola's Smart Networks Alliance. This platform approach can simplify and speed the development of full-featured networking applications today, enable faster development within and across product families, and provide a smooth migration path to future product generations.

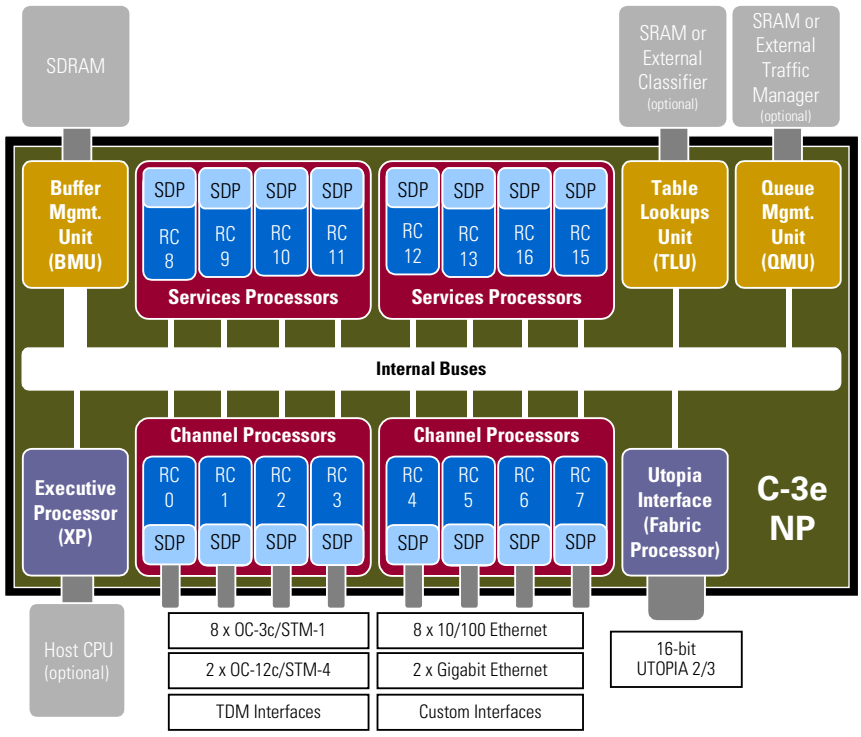
SOFTWARE-OPTIMIZED NPU ARCHITECTURE

Within a single, integrated architecture, the C-3e NP combines channel processing, services processing, and specialized coprocessing to provide highly efficient and flexible line-rate processing of access applications. In addition, the C-3e NP architecture was designed from the ground up to provide a simple and robust programming model. It enables full programmability of forwarding plane tasks using C-language and a standard API. To support this programming model, the interactions among subsystems of the architecture are very efficient with integrated coprocessor acceleration for common tasks.

Flexible, High-Density Line Interfaces

Traffic typically enters the C-3e NP through its eight Channel Processors (CPs), each of which can accommodate up to an OC-3's worth of bandwidth. Each CP contains a transmit and receive Serial Data Processor (SDP), which operates like a VLIW engine, and a RISC Core that is used for any application-specific purpose. The SDPs control programmable external pin logic, allowing them to implement a wide variety of Layer 1 interfaces including connection to T/E-Carrier framers, 10/100 Ethernet PHY (RMII), Gigabit Ethernet PHY (GMII or TBI), OC-3/STM-1 PHY, and OC-12/STM-4 PHY. Ethernet MACs and SONET framers are embedded in the SDP architecture.

At Layer 2, the SDPs can be independently configured to support Ethernet, Packet over SONET (PoS), HDLC streams, ATM, Frame Relay, FibreChannel, or virtually any format, including MPLS and other encapsulations. The programmability of the SDPs supports the diversity of media access control (MAC) interfaces, as well as data parsing requirements, and can support different protocol implementations on a port-by-port basis.



Highly-integrated NPU architecture provides programming efficiencies for advanced services in access applications

For aggregating even lower speed interfaces, the C-3e NP's Channel Processors can be connected to Motorola's TDM channel adapter products to provide highly cost-effective interface densities, without sacrificing functionality. For example, the TDM channel adapters will aggregate multiple T1/E1 lines consisting of multiple, independent, logical channels into a single C-3e NP Channel Processor.

The RISC Cores, programmed in C-language, are dedicated to the advanced services that benefit the most from high-level language implementations. For example, the RISC Cores focus on higher-level forwarding tasks such as final forwarding decision making, scheduling, and statistics gathering. The RISC Cores are also responsible for maintaining the context of the on-chip operations to ensure efficient delivery of traffic to the egress ports with appropriate service levels applied.

Advanced Services Processing

The C-3e NP dedicates eight of the CPs as Services Processors to help support the simultaneous, multi-protocol processing and interworking that is characteristic of access applications. As Services Processors, these CPs recirculate data processing internally and augment the usual packet/cell data parsing and protocol transformation with additional programming capacity in serial or parallel with other Channel Processor activities. They would typically assist with more advanced functions such as SARing, traffic management, and encapsulated protocol processing, enabling the C-3e NP to achieve line-rate performance, even in highly channelized designs.

Although there are sixteen RISC Cores in the CPs, each RISC Core is independently programmable, avoiding the limitations typical of traditional symmetric multi-processor designs.

High-Performance Coprocessing

The C-3e NP's coprocessors are shared among the CPs and are each optimized for a specific network processing function such as table lookups, queue management, buffer management, fabric interfacing, and supervisory processing.

The C-3e NP's fully integrated Table Lookup Unit (TLU) is a high-speed, flexible classification engine that enables a wide range of traffic classification with its various search algorithms. Typical lookups that the TLU supports include IPv4/IPv6 Longest Prefix Match, ATM VCI/VPIs, Ethernet MAC/VLANs, and Multiprotocol Label Switching (MPLS), among others. For example, the TLU can achieve more than 42 million IPv4 lookups per second due to its extensively pipelined architecture.

The C-3e NP's Queue Management Unit (QMU), when in internal mode, can support up to 512 queues to satisfy the traffic management requirements of a variety of access applications. However, using the QMU's external mode, the C-3e NP can be gluelessly coupled to one of Motorola's traffic management solutions for powerful ATM and IP QoS management.

Other coprocessing functions are handled by the:

- Buffer Management Unit (BMU) for storing payload
- Fabric Processor for Utopia 2/3 ATM fabric or framer connections
- Executive Processor for overall chip management and communicating with an external host processor during run-time when control plane interaction is required

C-3e NETWORK PROCESSOR PRODUCT HIGHLIGHTS

PROCESSING POWER	Core Clock Rate	180MHz
	RISC MIPs for C programmable Services	>3000 MIPs
	VLIW MIPs for interface / fabric programming	>16,000 MIPs
COMPUTING ELEMENTS	Channel Processors, each consisting of a 32-bit RISC core + dual VLIW Serial Data Processor	8, implementing external programmable interfaces
	Services Processors, each consisting of a 32-bit RISC core + dual VLIW Serial Data Processor	8, internal only
	Executive Processor, supporting PCI interface and serial I/O	1
PROGRAMMABLE INTERFACES	Integrated 10/100 Ethernet MACs (RMII)	Up to 8, using 1 Channel Processor per interface
	Integrated Gigabit Ethernet MACs (GMII, TBI)	Up to 2, using 4 Channel Processors per interface
	Integrated OC-3c/STM-1 SONET/SDH framers	Up to 8, using 1 Channel Processor per interface
	Integrated OC-12/OC-12c/STM-4 SONET/SDH framers	Up to 2, using 4 Channel Processors per interface
	Configurable serial (T-Carrier) / proprietary interfaces	Direct connection up to 8 lines, > 256 x T1/E1 with TDM channel adapters
	Integrated FibreChannel MACs (TBI)	Up to 2, using 4 Channel Processors per interface
	Utopia Interface	16 bit Utopia 2 / 3
	PCI Interface	32 bit, 66Mhz
CLASSIFICATION	Integrated Table Lookup Unit: Table type supported	Hash-Trie-Key, Data, Longest Prefix Match, Chained Index, and Chained Hash
	Longest Prefix Match Performance	~ 42M lookups/second (IPv4, ~256K routes, MAE West model, average)
	Number of independent table types	32
	Memory Interface	64-bit, ZBT SRAM, up to 125MHz
BUFFER MANAGEMENT	Memory Pools	Up to 30
	Multicast buffer support	Yes
	Memory Interface	128 bits, SDRAM, up to 125Mhz
TRAFFIC MANAGEMENT	Internal Queue Management Unit	512 Queues
	With Q-5 Traffic Management Coprocessor	128k Queues
INTERNAL MEMORY	Channel Processor Cluster IMEM / DMEM	32 / 48 KB
	Executive Processor IMEM / DMEM	48 / 32 KB
OTHER	Operating Temperature Range (Tj)	-40 to +125C
	Package	728 pin (27 pins x 27 pins) Ball Grid Array (BGA)

For more information about Motorola's network processor solutions, please contact your local Motorola sales representative or call (800) 521-6274. You can also visit Motorola's Smart Networks Web site at:

www.motorola.com/networkprocessors

EASY TO PROGRAM AND REPROGRAM

Like the rest of the C-Port family, the C-3e NP uses the same simple programming model comprised of robust Application Programming Interfaces (APIs), C-language programmability, and a comprehensive development environment. Not only does this programming model enable greater development productivity, it also provides a common software architecture for scaling applications within and across product lines to support a wide range of bandwidths.

Similar to APIs in the computing world, the C-Ware™ APIs abstract the underlying hardware architecture of the C-3e NP and support the most common network task building blocks, such as physical interface management, data forwarding, table lookups, buffer management, queuing operations, and so on. Programming to the C-Ware APIs ensures software compatibility and scalability from generation to generation of the C-Port family network processors.

With the flexibility provided by the C-3e NP architecture, it is a straight-forward task to write C-language software for the RISC Cores to perform a given function. The SDPs are programmed in microcode, which is provided by Motorola for the vast majority of applications (including Ethernet, IP and ATM over SONET, T/E carrier serial data streams, and so on). All the tools necessary for equipment vendors to program the SDPs (including assembler and simulator support) are available. Support for MAC level diversity is available without any user coding.

The programming task is significantly enhanced by the comprehensive C-Port family development environment that consists of the following components:

- **C-Ware Applications Library (CAL)** — Comprehensive set of reference applications for building networking systems based on Motorola's C-Port family. The CAL significantly accelerates customer software development by providing extensive reference source code that is instrumented for and tested with the C-Ware Software Toolset (CST). The product-quality Wireless Network Interface (WNI) reference software is part of the CAL.
- **C-Ware Software Toolset (CST)** — Functional and performance accurate simulation environment, standard GNU-based compiler and debugger, GUI performance analysis tool, traffic scripting tools, and comprehensive C-Ware APIs.
- **C-Ware Development System (CDS)** — Compact PCI chassis with Motorola MPC750 Host Application Module, which can also include Network Processor Switch Modules, TMC Daughter Cards, and various Physical Interface Modules (PIMS). Complete hardware reference designs are also available.

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