CLC402

CLC402 Low-Gain Op Amp with Fast 14-bit Settling

Literature Number: SNOS850

National Semiconductor

CLC402
Low-Gain Op Amp with Fast 14-Bit Settling

General Description

The CLC402 is an operational amplifier designed for low-gain applications (±1 to ±8), requiring fast, accurate settling and superior DC accuracy. Settling to 0.0025% in 25ns (32ns guaranteed over temperature), the CLC402 is ideal as the input amplifier in high accuracy (up to 14-bits) A/D systems. Unlike most other high-speed op amps, the CLC402 is free of thermally induced tails in the settling response.

The CLC402 is an upgrade to and pin compatible with the industry standard CLC400. Constructed using a unique, proprietary design and an advanced complementary bipolar process, it offers performance far beyond ordinary monolithic op amps. In addition, unlike many other high-speed op amps, the CLC402 offers both high performance and stability without the need for compensation circuitry – even at a gain of +1.

Supporting the CLC402's excellent pulse performance are improved DC characteristics. The CLC402's input offset voltage is typically 0.5mV and is guaranteed to be less than 1.6mV at +25°C. The input offset voltage drift is typically only 3μV/°C.

The CLC402 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC402AJP	-40°C to +85°C	8-pin plastic DIP
CLC402AJE	-40°C to +85°C	8-pin plastic SOIC
CLC402A8B	-55°C to +125°C	8-pin hermetic CERDIP, MIL-STD-833, Level B
CLC402ALC	-40°C to +85°C	dice
CLC402AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B

DESC SMD number: 5962-92033

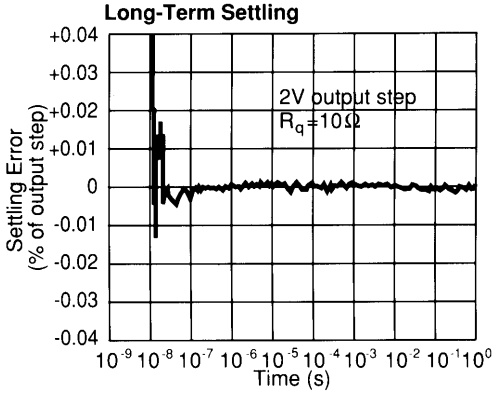
Features

- 0.0025% settling in 25ns (32ns max)
- 0.5mV input offset voltage, 3μV/°C drift
- ±1 to ±8 closed-loop gain range
- Low power, 150mW
- 0.01%/0.05° differential gain/phase

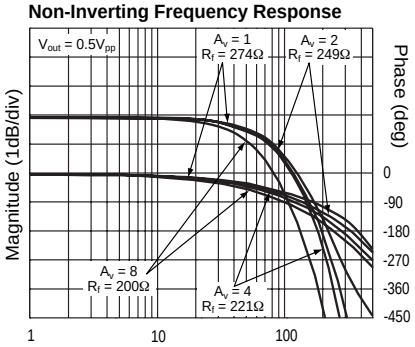
Applications

- High-accuracy A/D systems (12-14 bits)
- High-accuracy D/A converters
- High-speed communications
- IF processors
- Video distribution

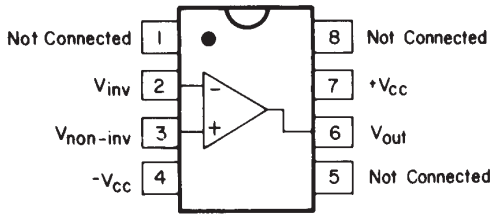
Long-Term Settling



Non-Inverting Frequency Response



Pinout
DIP & SOIC



Printed in the U.S.A.

CLC402 Electrical Characteristics (A_V = +2, V_{cc} = ±5V, R_L = 100Ω, R_f = 250Ω; unless specified)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC402AJ	+25°C	−40°C	+25°C	+ 85°C		
FREQUENCY DOMAIN PERFORMANCE							
-3dB bandwidth	V_{out}<0.5V_{pp}	195	>120	>130	>120	MHz	SSBW
	V_{out}<5V_{pp}	80	>50	>50	>50	MHz	LSBW
gain flatness[2]	V_{out}<0.5V_{pp}						
peaking	DC to 25MHz	0	<0.4	<0.3	<0.4	dB	GFPL
peaking	>25MHz	0	<0.7	<0.5	<0.7	dB	GFPH
rolloff	DC to 50MHz	0.5	<1.0	<1.0	<1.0	dB	GFR
linear phase deviation	DC to 50MHz	0.4	<1.2	<1.0	<1.2	°	LPD
TIME DOMAIN PERFORMANCE							
rise and fall time	0.5V step	2.0	<2.9	<2.7	<2.9	ns	TRS
	5V step	5.0	<8	<8	<8	ns	TRL
settling time to ±0.0025%	2Vstep	25	<32	<32	<32	ns	TS14
±0.01%	2V step	18	<25	<25	<25	ns	TSP
±0.1%	2V step	10	<15	<15	<15	ns	TSS
overshoot	0.5V step	0	<10	<10	<10	%	OS
slew rate		800	>500	>500	>500	V/μs	SR
DISTORTION AND NOISE PERFORMANCE							
2nd harmonic distortion	2V_{pp}, 20MHz	−50	<−38	<−43	<−43	dBc	HD2
3rd harmonic distortion	2V_{pp}, 20MHz	−60	<−53	<−53	<−50	dBc	HD3
equivalent input noise							
noise floor	>1MHz	−157	<−155	<−155	<−155	dBm(1Hz)	SNF
integrated noise	1MHz to 150MHz	40	<49	<49	<49	μV	INV
differential gain[1]		0.01	—	—	—	%	DG
differential phase[1]		0.05	—	—	—	°	DP
STATIC, DC PERFORMANCE							
*input offset voltage		0.5	<2.6	<1.6	<2.8	mV	VIO
average temperature coefficient		3	<12	—	<12	μV/°C	DVIO
*input bias current	noninverting	10	<45	<25	<35	μA	IBN
average temperature coefficient		100	<250	—	<100	nA/°C	DIBN
*input bias current	inverting	10	<50	<30	<40	μA	IBI
average temperature coefficient		100	<250	—	<100	nA/°C	DIBI
power supply rejection ratio		68	>55	>60	>60	dB	PSRR
common mode rejection ratio		65	>55	>60	>60	dB	CMRR
*supply current	no load	15	<20	<20	<20	mA	ICC
MISCELLANEOUS PERFORMANCE							
noninverting input	resistance	150	>50	>85	>85	kΩ	RIN
	capacitance	3.5	<5.5	<5.5	<5.5	pF	CIN
output impedance	at DC	0.02	<0.1	<0.1	<0.1	Ω	RO
common mode input range		±3.0	>±2.0	>±2.5	>±2.5	V	CMIR
output voltage range	no load	±3.5V	>±3.0	>±3.2	>±3.2	V	VO
output current		±55	>±25	>±45	>±45	mA	IO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} output is short circuit protected to ground, but, maximum reliability will be obtained if I_{out} does not exceed...	70mA
input voltage	±V_{cc}
junction temperature	+175°C
operating temperature range AJ:	− 40°C to +85°C
storage temperature range	− 65°C to +150°C
lead solder duration (+300°C)	10 sec
ESD rating (human body model)	2000V

Reliability Information

Transistor count	37

Miscellaneous Ratings

recommended gain range: ±1 to ±8

Notes:

* AJ 100% tested at +25°C.

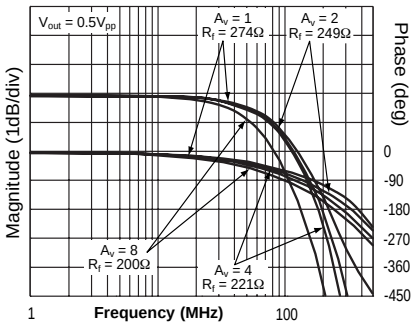
note 1: Differential gain and phase measured at A_v = +2V, R = 250Ω, R_L = 150Ω, 1V_{pp} equivalent video signal 0-100 IRE, 40 IRE_{pp}, 0IRE = 0 volts, 75Ω load and 3.58 MHz.

Package Thermal Resistance

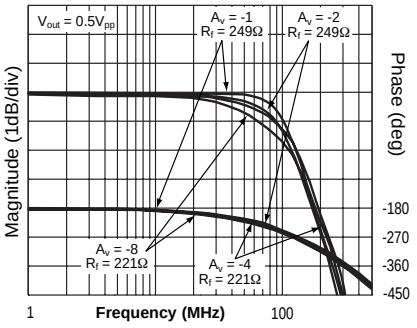
Package	θ_{JC}	θ_{JA}
AJP	70°C/W	125°C/W
AJE	65°C/W	145°C/W
CERDIP	45°C/W	135°C/W

CLC402 Typical Performance Characteristics (T_A = 25°, A_V = +2, V_{CC} = ±5V, R_L = 100Ω, Rf = 250Ω; unless specified)

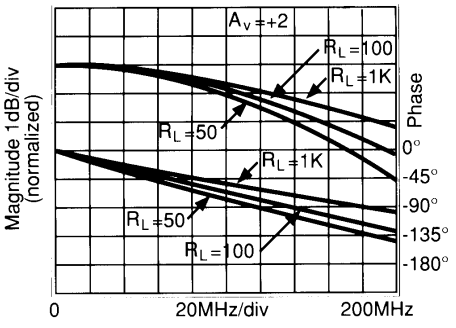
Non-Inverting Frequency Response



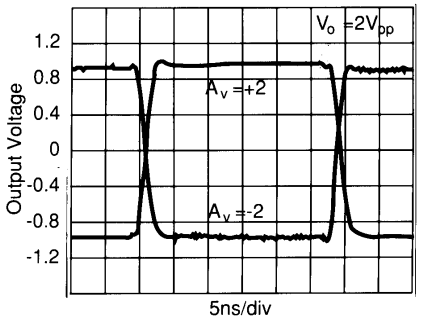
Inverting Frequency Response



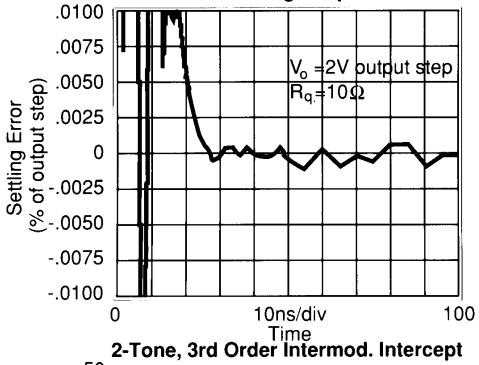
Frequency Response vs. Load (R_L)



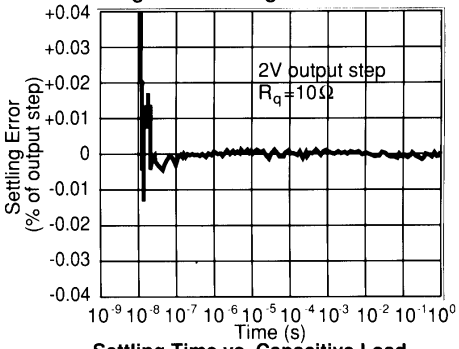
Small Signal Pulse Response



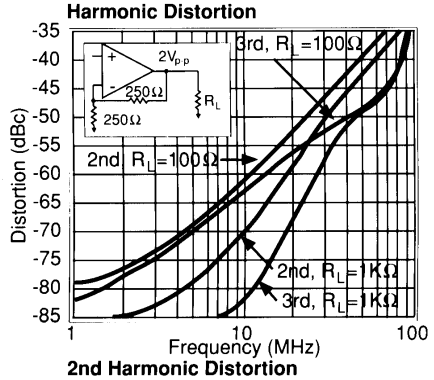
Short Term Settling Response



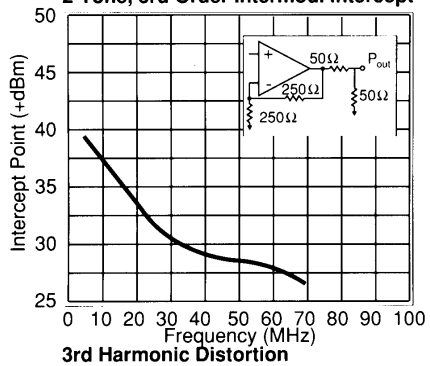
Long-Term Settling



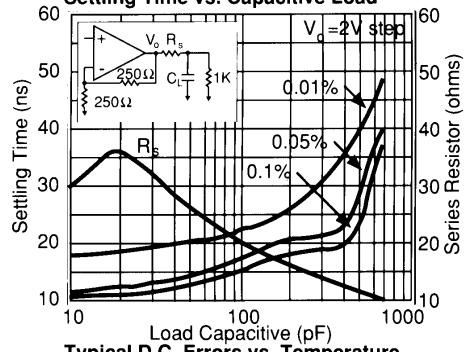
Harmonic Distortion



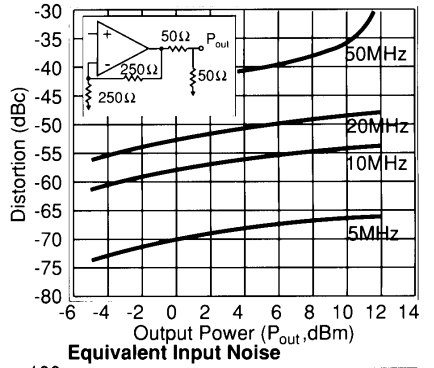
2-Tone, 3rd Order Intermod. Intercept



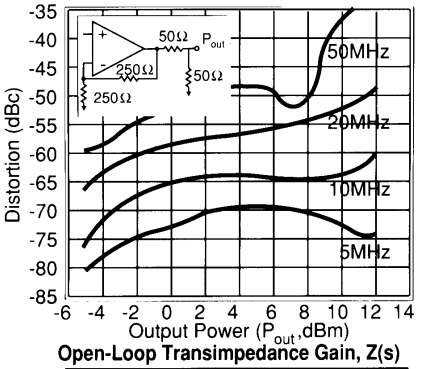
Settling Time vs. Capacitive Load



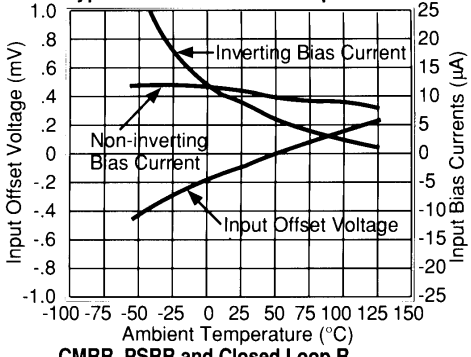
2nd Harmonic Distortion



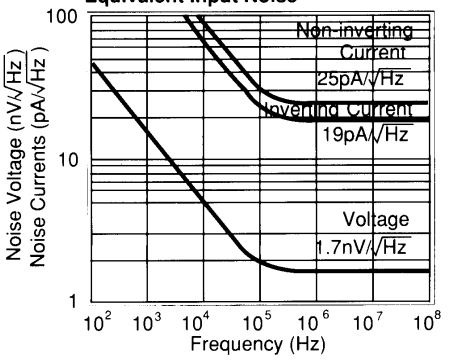
3rd Harmonic Distortion



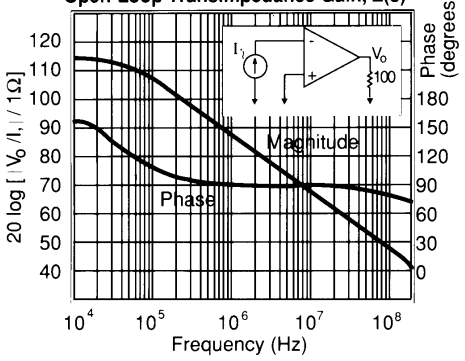
Typical D.C. Errors vs. Temperature



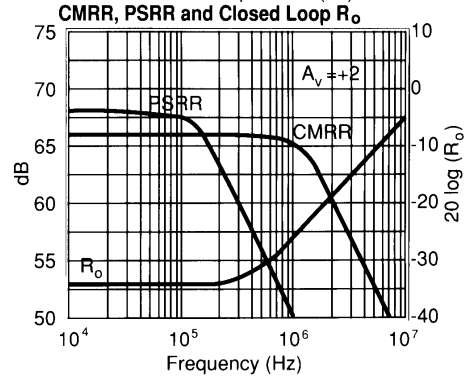
Equivalent Input Noise



Open-Loop Transimpedance Gain, Z(s)



CMRR, PSRR and Closed Loop R_o



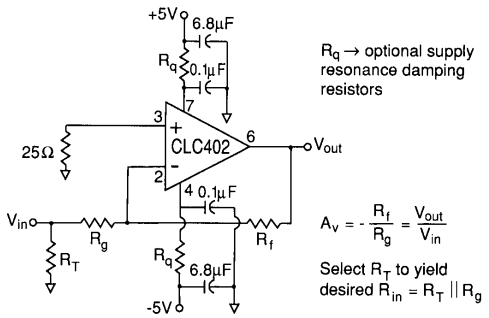


Figure 1: recommended inverting gain circuit

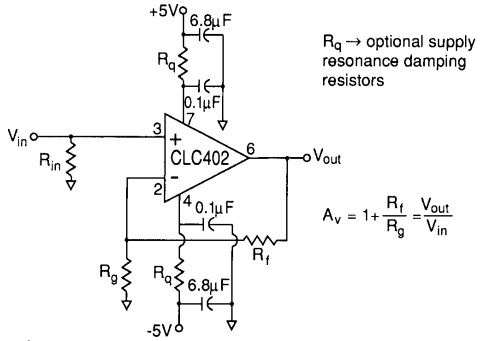


Figure 2: recommended non-inverting gain circuit

Feedback Resistor

The CLC402 achieves its excellent pulse response by using the current feedback topology pioneered by Comlinear Corporation. The loop gain for a current feedback op amp, and hence the frequency response, is predominantly set by the feedback resistor value. The CLC402 is optimized for use with a 250Ω feedback resistor. Using lower values can lead to excessive ringing in the pulse response while a higher value will limit the bandwidth. Application Note OA-13 discusses this in detail along with occasions where a different R_f might be advantageous.

Optimizing Settling Time

The CLC402 is capable of extremely fast pulse settling times to very fine scale accuracies (.0025% in 25ns typical). It is also virtually free of any measurable thermal tail effects as shown in the long-term settling time plot on the previous page. Careful attention to parasitic effects is critical to achieving this level of performance.

Generally, open any ground and/or power planes around the device while providing an adjacent ground plane for the 0.1µf ceramic decoupling caps. These caps should be very near the power pins. Connecting the ground return point for the electrolytic capacitors near the load ground point is also very useful. Similarly, for non-inverting applications, connecting R_g to ground near the input terminating resistor ground connection will improve performance. These suggestions become particularly pertinent for fastest settling to lower than 0.1% accuracies.

Using Supply Resistors, R_q

Figures 1 and 2 show a series resistor in the supply leads between the electrolytic and ceramic capacitors. This optional resistor is intended to de-Q any self-resonance between those capacitors and the power supply trace inductance. Any large output voltage step into a significant load, either resistive or capacitive, will necessarily pull a current surge through the supply de-coupling capacitors. This can cause a very low level, high frequency ringing on the power supplies that may not be effectively rejected by the PSRR of the CLC402. This can, in turn, show up at the output as a ringing that will preclude high speed settling to very fine scale accuracies.

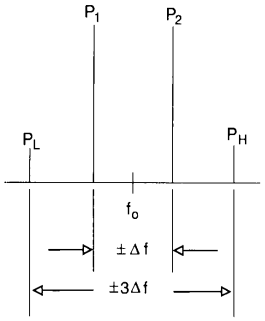
Adding R_q will increase the amplitude of this signal at the supplies but will lower the frequency content to where the CLC402's PSRR can effectively reject it. An R_q of 5 to 10Ω will yield excellent settling performance with minimal impact on other performance parameters.

Driving Capacitive Loads

Either parasitic or load capacitance directly on the output pin can quickly lead to unacceptable levels of ringing in the pulse response. Adding a series resistor, as shown in the plot of R_s vs. C_L on the previous page, will resolve this problem. Parasitic capacitances less than 2pF can be driven without the series resistor. See Application Note OA-15 for additional discussion.

Distortion Performance

The distortion plots show the harmonic distortions and 3rd order intermodulation intercepts under a variety of load, power, and frequency conditions. Generally, going to higher frequencies will degrade the distortion performance as the amplifier loop gain decreases. Further distortion improvements at low frequencies are observed when driving higher impedance loads. The 3rd order intermodulation intercept plot may be used to predict the 3rd order spurious levels given the power levels at the load for two closely spaced signal frequencies. Figure 3 shows the signal and spurious level definitions along with equations for predicting the spurious powers from the intercept value and the two signal powers.



P_1, P_2 – test powers at load

P_L, P_H – 3rd order spurious powers (all in dBm)

IM3 – 3rd order intercept (from datasheet plot)

$P_L = P_2 - 2\,(IM3 - P_1)$

$P_H = P_1 - 2\,(IM3 - P_2)$

Figure 3: 3rd order spurious calculations

DC Accuracy and Noise

The CLC402 offers an improved offset voltage over the comparable CLC400 low gain amplifier. The offset adjustment available on the CLC400 was therefore not included in this part. Figure 4 shows the output offset computational equation for the non-inverting configuration with an example using the typical bias current and offset specifications for $A_v = +2$.

Output Offset

$$V_o = \left(\pm I_{bn} R_{in} \pm V_{io}\right)\left(1 + \frac{R_f}{R_g}\right) \pm I_{bi}\, R_f$$

Example computation for $A_v = +2$, $R_f = 250\Omega$

$V_o = (\pm 10\mu A\,(50\Omega) \pm 0.5mV)\,(2) \pm 10\mu A\,(250\Omega) = \pm 3.5mV$

Figure 4: Output DC offset calculation

This low output offset voltage is a marked improvement over earlier very high speed amplifiers. Further improvement in the output offset voltage and drift is possible using the composite amplifiers described in Application Note OA-7.

The equivalent input noise plot shows that the CLC402 offers a low 1.7nV/√Hz input noise voltage. A low non-inverting source impedance should be used for lowest noise performance due to the relatively high current noise at that input. See Application Note OA-12 for a full discussion of noise calculations for current feedback amplifiers.

Printed Circuit Layout

Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC402 are available. This board can be easily modified to include the R_q resistors discussed above. Further layout suggestions may be found in Application Note OA-15.

This page intentionally left blank.

Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at **1-800-272-9959** or fax **1-800-737-7018**.

Life Support Policy

National's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of National Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
E-mail: europe.support.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Francais Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block
Ocean Centre, 5 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265