National Semiconductor

Comlinear CLC408
High-Speed, Low-Power Line Driver

General Description

The Comlinear CLC408 delivers high output drive current (96mA), but consumes minimal quiescent supply current (1.5mA). Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels.

The CLC408 offers superior dynamic performance with a 130MHz small-signal bandwidth, 350V/µs slew rate and 4.6ns rise/fall times ($2V_{pp}$). The combination of low quiescent power, high output drive current, and high-speed performance make the CLC408 a great choice for many portable and battery-powered personal communication and computing systems.

The CLC408 drives low-impedance loads, including capacitive loads, with little change in performance. Into a 100Ω load, it delivers -85/-64dBc second/third harmonic distortion (A_V = +2, V_o = $2V_{pp}$, f = 1MHz). With a 25Ω load, and the same conditions, it produces only -67/-62dBc second/third harmonic distortion. It is also an excellent choice for driving high currents into single-ended transformers and coils.

When driving the input of high resolution A/D converters, the CLC408 provides excellent -85/-75dBc second/third harmonic distortion and fast settling time (A_V = +2, V_o = $2V_{pp}$, f = 1MHz, R_L =1kΩ).

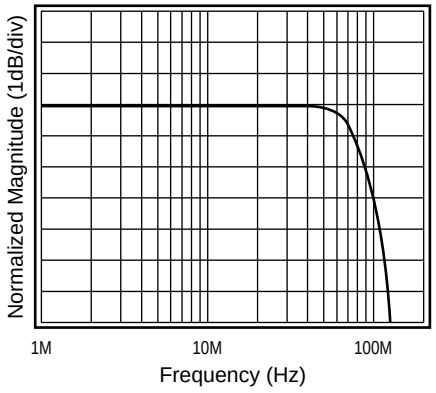
Features

- 96mA output current
- 1.5mA supply current
- 130MHz bandwidth (Av = +2)
- -85/-75dBc HD2/HD3 (1MHz)
- 15ns settling to 0.2%
- 350V/µs slew rate
- Dual version available (CLC418)

Applications

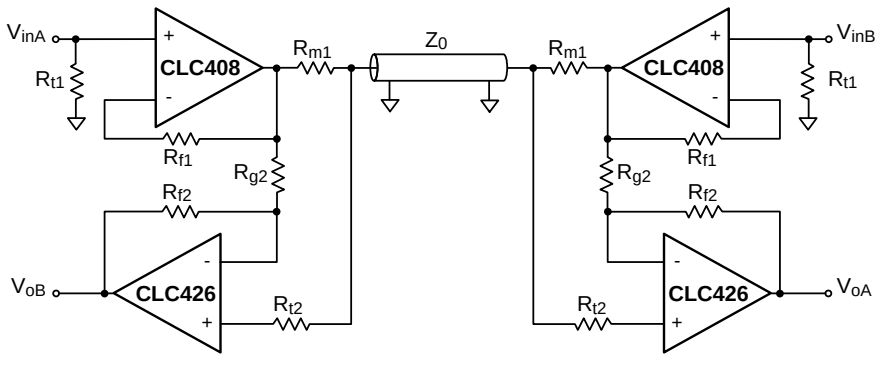
- Coaxial cable driver
- Twisted pair driver
- Transformer/coil driver
- High capacitive load driver
- Video line driver
- ADSL/HDSL driver
- Portable/battery-powered line driver
- A/D driver

Non-Inverting Frequency Response
(A_V = +2V/V, R_L = 25Ω)



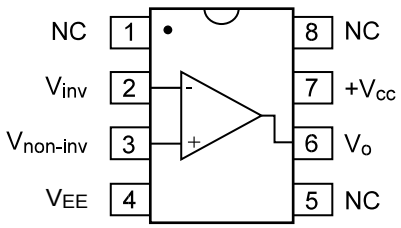
Typical Application Diagram

Full Duplex Cable Driver



Pinout

DIP & SOIC



CLC408 Electrical Characteristics (A_v = +2, R_f = 1kΩ, R_L = 100Ω, V_{CC} = ± 5V, unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
Ambient Temperature	CLC408AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 1.0V_{pp}	130	90	80	75	MHz	B
	V_{out} < 4.0V_{pp}	45	33	29	28	MHz	
-0.1dB bandwidth	V_{out} < 1.0V_{pp}	60	30	25	25	MHz	
gain flatness	V_{out} < 1.0V_{pp}						
peaking	DC to 200MHz	0.1	0.5	0.9	1.0	dB	B
rolloff	<30MHz	0	0.1	0.25	0.25	dB	B
linear phase deviation	<30MHz	0.2	0.4	0.5	0.5	deg	
differential gain	NTSC, R_L=150Ω	0.1	–	–	–	%	
differential phase	NTSC, R_L=150Ω	0.4	–	–	–	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	4.6	7.0	7.5	8.0	ns	
settling time to 0.2%	2V step	15	30	38	40	ns	
overshoot	2V step	5	12	12	12	%	
slew rate A_V = +2	2V step	350	260	225	215	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz	-85	–	–	–	dBc	
	2V_{pp}, 1MHz; RL = 1kΩ	-85	–	–	–	dBc	
	2V_{pp}, 5MHz	-65	-60	-58	-58	dBc	B
3rd harmonic distortion	2V_{pp}, 1MHz	-64	–	–	–	dBc	
	2V_{pp}, 1MHz; RL = 1kΩ	-75	–	–	–	dBc	
	2V_{pp}, 5MHz	-50	-45	-44	-44	dBc	B
equivalent input noise							
voltage (e_{ni})	>1MHz	5	6.3	6.6	6.7	nV/√Hz	
non-inverting current (i_{bn})	>1MHz	1.4	1.8	1.9	2.3	pA/√Hz	
inverting current (i_{bi})	>1MHz	13	16	17	18	pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		2	8	11	11	mV	A
average drift		25	–	35	40	µV/°C	
input bias current (non-inverting)		2	8	11	15	µA	A
average drift		60	–	80	110	nA/°C	
input bias current (inverting)		2	10	18	20	µA	A
average drift		20	–	90	110	nA/°C	
power supply rejection ratio	DC	55	50	48	48	dB	B
common-mode rejection ratio	DC	52	48	46	46	dB	
supply current	R_L= ∞	1.5	1.7	1.8	1.8	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance (non-inverting)		5	3	2.5	1	MΩ	
input capacitance (non-inverting)		1	2	2	2	pF	
common mode input range		±2.7	±2.3	±2.2	±2.0	V	
output voltage range	R_L = 100Ω	± 3.3	±2.9	±2.8	±2.6	V	
output voltage range	R_L = ∞	±4.0	±3.8	±3.7	±3.5	V	
output current		96	96	96	60	mA	C
output resistance, closed loop	DC	0.03	0.15	0.2	0.3	Ω	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

supply voltage	±7V
output current (see note C)	96mA
common-mode input voltage	±V_{CC}
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C
ESD rating (human body model)	2000V

Notes

A) J-level: spec is 100% tested at +25°C, sample tested at +85°C. LC/MC-level: spec is 100% wafer probed at +25°C.
B) J-level: spec is sample tested at +25°C.
C) The output current sourced or sunk by the CLC408 can exceed the maximum safe output current.

Ordering Information

Model	Temperature Range	Description
CLC408AJP	-40°C to +85°C	8-pin PDIP
CLC408AJE	-40°C to +85°C	8-pin SOIC
CLC408AJE-TR	-40°C to +85°C	8-pin SOIC, 750pc reel
CLC408AJE-TR13	-55°C to +125°C	8-pin SOIC, 2500pc reel
CLC408ALC	-40°C to +85°C	dice (commercial)

Package Thermal Resistance

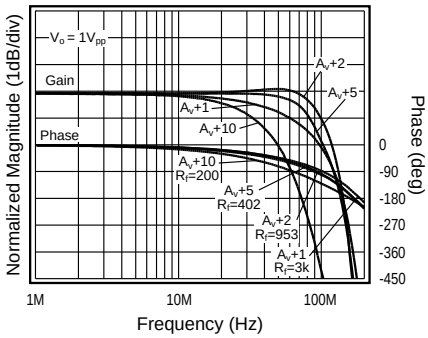
Package	θ_{JC}	θ_{JA}
Plastic (AJP)	115°C/W	125°C/W
Surface Mount (AJE)	130°C/W	150°C/W

Reliability Information

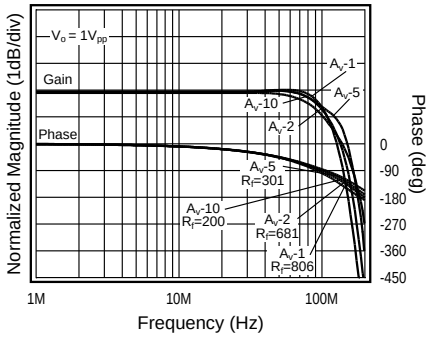
Transistor Count	38
MTBF (based on limited test data)	46Mhr

Typical Performance Characteristics (A_v = +2, R_f = 1kΩ, R_L = 100Ω, V_{CC} = +5V, T = 25°C, CLC408AJ; unless specified)

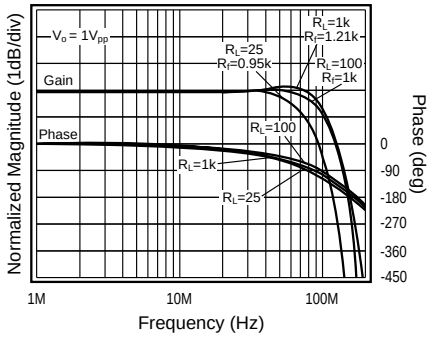
Non-Inverting Frequency Response



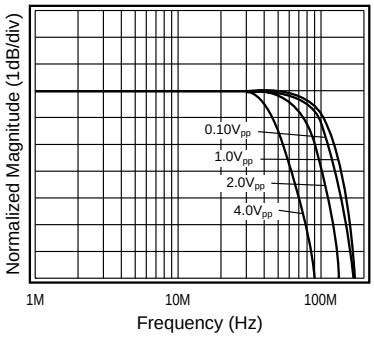
Inverting Frequency Response



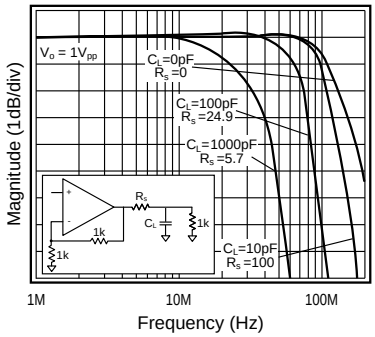
Frequency Response vs. R_L



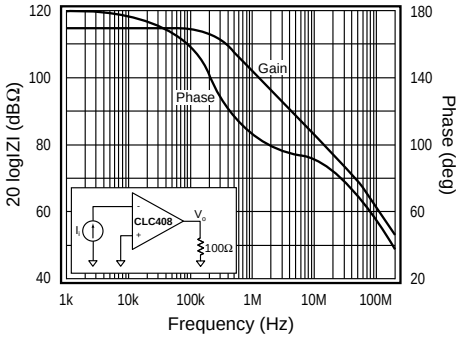
Frequency Response vs. V_{out}



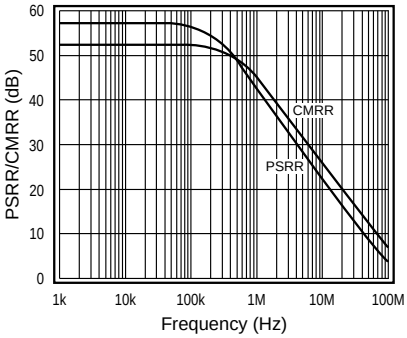
Frequency Response vs. Capacitive Load



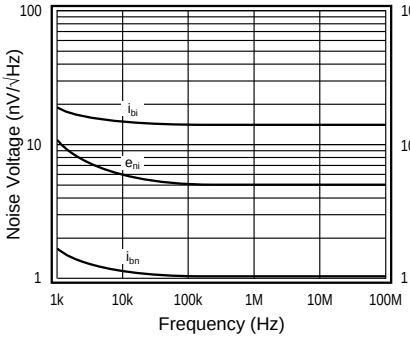
Open Loop Transimpedance Gain, Z(s)



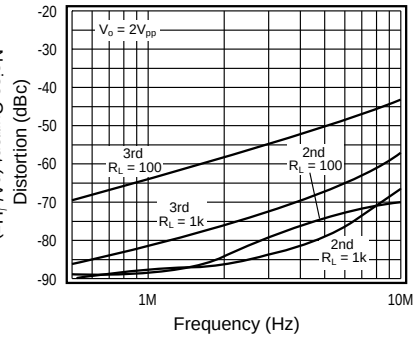
PSRR and CMRR



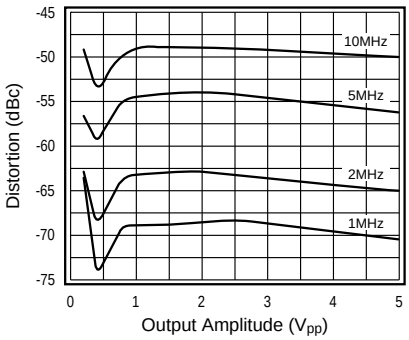
Equivalent Input Noise



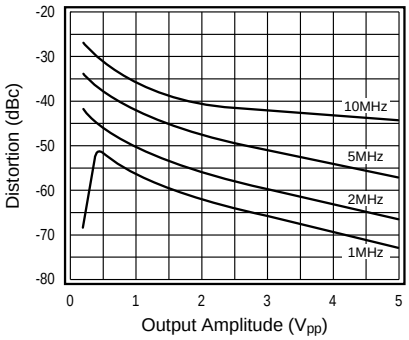
2nd & 3rd Harmonic Distortion



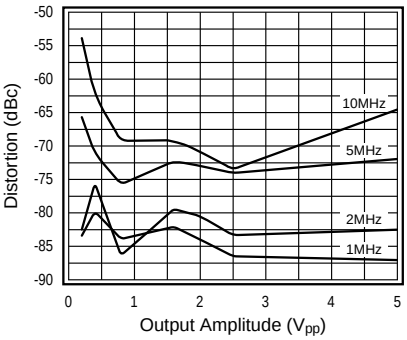
2nd Harmonic Distortion, R_L = 25Ω



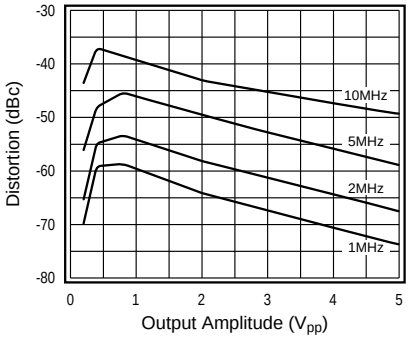
3rd Harmonic Distortion, R_L = 25Ω



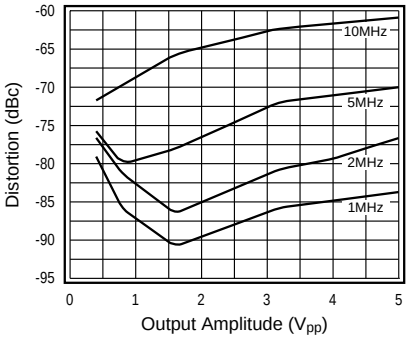
2nd Harmonic Distortion, R_L = 100Ω



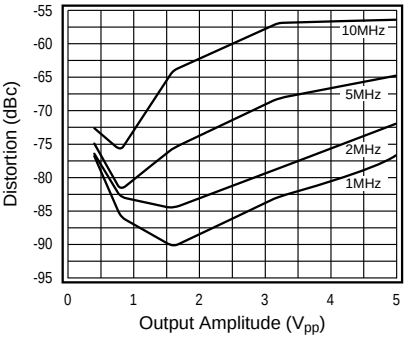
3rd Harmonic Distortion, R_L = 100Ω



2nd Harmonic Distortion, R_L = 1kΩ

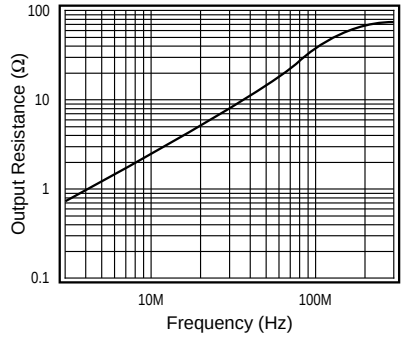


3rd Harmonic Distortion, R_L = 1kΩ

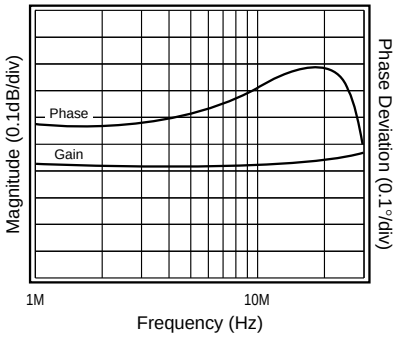


Typical Performance Characteristics (A_v = +2, R_f = 1kΩ, R_L = 100Ω, V_{CC} = +5V, T = 25°C, CLC408AJ; unless specified)

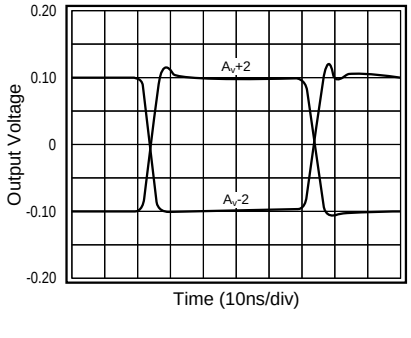
Closed Loop Output Resistance



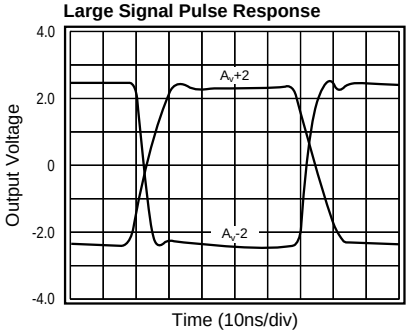
Gain Flatness & Linear Phase Deviation



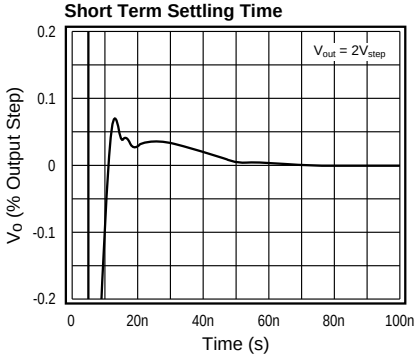
Small Signal Pulse Response



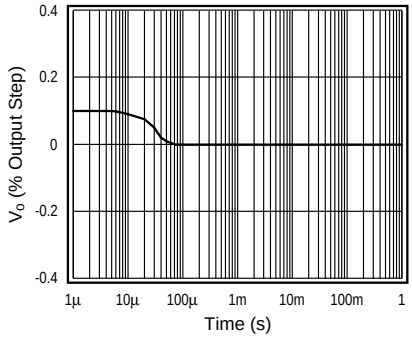
Large Signal Pulse Response



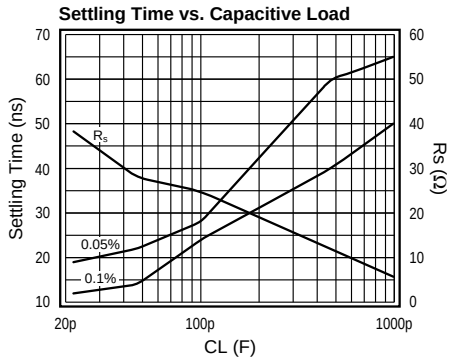
Short Term Settling Time



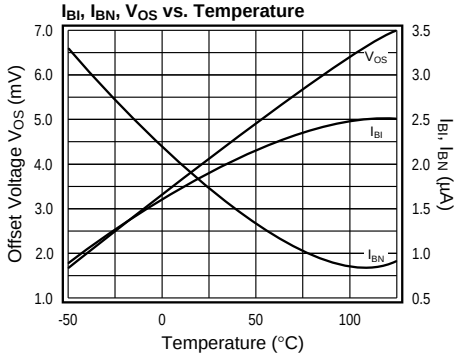
Long Term Settling Time



Settling Time vs. Capacitive Load



I_{BI}, I_{BN}, V_{OS} vs. Temperature



CLC408 OPERATION

The CLC408 has a current-feedback (CFB) architecture built in an advanced complementary bipolar process. The key features of current-feedback are:

- AC bandwidth is independent of voltage gain
- Inherently unity-gain stability
- Frequency response may be adjusted with feedback resistor (R_f in Figures 1-3)
- High slew rate
- Low variation in performance for a wide range of gains, signal levels and loads
- Fast settling

Current-feedback operation can be explained with a simple model. The voltage gain for the circuits in Figures 1 and 2 is approximately:

$$\frac{V_o}{V_{in}} = \frac{A_v}{1 + \frac{R_f}{Z(j\omega)}}$$

where:

- A_v is the DC voltage gain
- R_f is the feedback resistor
- $Z(j\omega)$ is the CLC408's open-loop transimpedance gain
- $\frac{Z(j\omega)}{R_f}$ is the loop gain

The denominator of the equation above is approximately 1 at low frequencies. Near the -3dB corner frequency, the interaction between R_f and $Z(j\omega)$ dominates the circuit performance. Increasing R_f does the following:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

CLC408 DESIGN INFORMATION

Standard op amp circuits work with CFB op amps. There are 3 unique design considerations for CFB:

- The feedback resistor (R_f in Figures 1-3) sets AC performance
- R_f cannot be replaced with a short or a capacitor
- The output offset voltage is not reduced by balancing input resistances

The following sub-sections cover:

- Design parameters, formulas and techniques
- Interfaces
- Application circuits
- Layout techniques
- SPICE model information

DC Gain (non-inverting)

The non-inverting DC voltage gain for the configuration shown in Figure 1 is: $A_v = 1 + \frac{R_f}{R_g}$

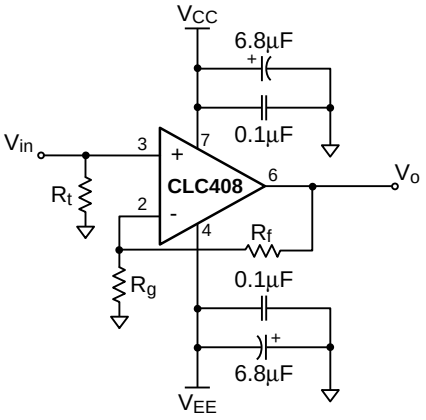


Figure 1: Non-Inverting Gain

The normalized gain plots in the ***Typical Performance Characteristics*** section show different feedback resistors (R_f) for different gains. These values of R_f are recommended for obtaining the highest bandwidth with minimal peaking. The resistor R_t provides DC bias for the non-inverting input.

For A_v < 6, use linear interpolation on the nearest A_v values to calculate the recommended value of R_f. For $A_v \geq 6$, the minimum recommended R_f is 200Ω.

Select R_g to set the DC gain: $R_g = \frac{R_f}{A_v - 1}$

DC gain accuracy is usually limited by the tolerance of R_f and R_g.

DC Gain (unity gain buffer)

The recommended R_f for unity gain buffers is 3kΩ. R_g is left open. Parasitic capacitance at the inverting node may require a slight increase of R_f to maintain a flat frequency response.

DC Gain (inverting)

The inverting DC voltage gain for the configuration shown in Figure 2 is: $A_v = -\frac{R_f}{R_g}$

The normalized gain plots in the ***Typical Performance Characteristics*** section show different feedback resistors (R_f) for different gains. These values of R_f are recommended for obtaining the highest bandwidth with minimal peaking. The resistor R_t provides DC bias for the non-inverting input.

For $|A_v|$ < 6, use linear interpolation on the nearest A_v values to calculate the recommended value of R_f. For $|A_v| \geq 6$, the minimum recommended R_f is 200Ω.

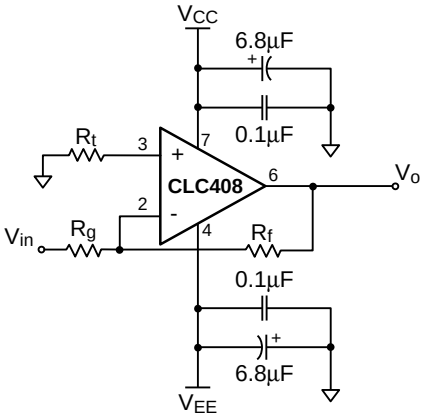


Figure 2: Inverting Gain

Select R_g to set the DC gain: $R_g = \frac{R_f}{|A_v|}$. At large gains, R_g becomes small and will load the previous stage. This can be solved by driving R_g with a low impedance buffer like the CLC111, or increasing R_f and R_g. See the ***AC Design (small signal bandwidth)*** sub-section for the tradeoffs.

DC gain accuracy is usually limited by the tolerance of R_f and R_g.

DC Gain (transimpedance)

Figure 3 shows a transimpedance circuit where the current I_{in} is injected at the inverting node. The current source's output resistance is much greater than R_f.

The DC transimpedance gain is: $A_R = \frac{V_o}{I_{in}} = -R_f$

The recommended R_f is 3kΩ. Parasitic capacitance at the inverting node may require a slight increase of R_f to maintain a flat frequency response.

DC gain accuracy is usually limited by the tolerance of R_f.

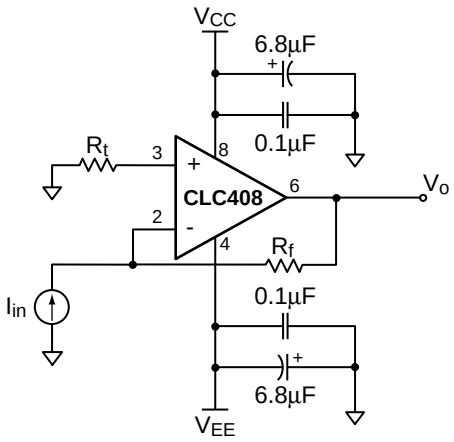


Figure 3: Transimpedance Gain

DC Design (level shifting)

Figure 4 shows a DC level shifting circuit for inverting gain configurations. V_{ref} produces a DC output level shift of $-V_{ref} \cdot \frac{R_f}{R_{ref}}$, which is independent of the DC output produced by V_{in}.

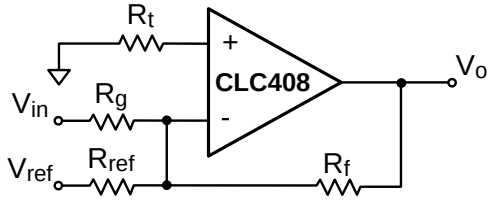


Figure 4: Level Shifting Circuit

DC Design (DC offsets)

The DC offset model shown in Fig. 5 is used to calculate the output offset voltage. The equation for output offset voltage is:

$$V_o = -\left(V_{os} + I_{BN} \cdot R_{eq1}\right) \cdot \left(1 + \frac{R_f}{R_{eq2}}\right) + \left(I_{BI} \cdot R_f\right)$$

The current offset terms, I_{BN} and I_{BI}, ***do not track each other***. The specifications are stated in terms of magnitude only. Therefore, the terms V_{os}, I_{BN}, and I_{BI} can have either polarity. Matching the equivalent resistance seen at both input pins does not reduce the output offset voltage.

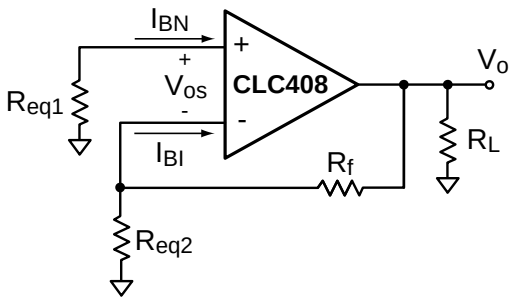


Figure 5: DC Offset Model

DC Design (output loading)

R_L, R_f, and R_g load the op amp output. The equivalent load seen by the output in Figure 5 is:

$$R_{L(eq)} = \begin{cases} R_L \parallel (R_f + R_{eq2}), \text{ non-inverting gain} \\ R_L \parallel R_f, \text{ inverting and transimpedance gain} \end{cases}$$

The equivalent output load ($R_{L(eq)}$) needs to be large enough so that the output current can produce the required output voltage swing.

AC Design (small signal bandwidth)

The CLC408 current-feedback amplifier bandwidth is a function of the feedback resistor (R_f), not of the DC voltage gain (A_V). The bandwidth is approximately proportional to $\frac{1}{R_f}$. As a rule, if R_f doubles, the bandwidth is cut in half.

Other AC specifications will also be degraded. Decreasing R_f from the recommended value increases peaking, and ***for very small values of R_f oscillation will occur.***

AC Design (minimum slew rate)

Slew rate influences the bandwidth of large signal sinusoids. To determine an approximate value of slew rate necessary to support a large sinusoid, use the following equation:

$$SR > 5 \cdot f \cdot V_{peak}$$

where V_{peak} is the peak output sinusoidal voltage.

The slew rate of the CLC408 in inverting gains is always higher than in non-inverting gains.

AC Design (linear phase/constant group delay)

The recommended value of R_f produces minimal peaking and a reasonably linear phase response. To improve phase linearity when $|A_v| < 6$, increase R_f approximately 50% over its recommended value. Some adjustment of R_f may be needed to achieve phase linearity for your application. See the ***AC Design (small signal bandwidth)*** sub-section for other effects of changing R_f.

Propagation delay is approximately equal to group delay. Group delay is related to phase by this equation:

$$\tau_{gd}(f) = -\frac{1}{360^\circ} \cdot \frac{d\phi(f)}{df} \approx -\frac{1}{360^\circ} \cdot \frac{\Delta\phi(f)}{\Delta f}$$

where $\phi(f)$ is the phase in degrees. Linear phase implies constant group delay. The technique for achieving linear phase also produces a constant group delay.

AC Design (peaking)

Peaking is sometimes observed with the recommended R_f. If a small increase in R_f does not solve the problem, then investigate the possible causes and remedies listed below:

- Capacitance across R_f
  - ***Do not place a capacitor across*** R_f
  - Use a resistor with low parasitic capacitance for R_f
- A capacitive load
  - Use a series resistor between the output and a capacitive load (see the ***Settling Time vs. C_L*** plot)
- Long traces and/or lead lengths between R_f and the CLC408
  - Keep these traces as short as possible

For non-inverting and transimpedance gain configurations:

- Extra capacitance between the inverting pin and ground (C_g)
  - See the ***Printed Circuit Board Layout*** sub-section below for suggestions on reducing C_g
  - Increase R_f if peaking is still observed after reducing C_g

For inverting gain configurations:

- Inadequate ground plane at the non-inverting pin and/or long traces between non-inverting pin and ground
  - Place a 50 to 200Ω resistor between the non-inverting pin and ground (see R_t in Figure 2)

Capacitive Loads

Capacitive loads, such as found in A/D converters, require a series resistor (R_s) in the output to improve settling performance. The ***Settling Time vs. Capacitive Load*** plot in the ***Typical Performance Characteristics*** section provides the information for selecting this resistor.

Using a resistor in series with a reactive load will also reduce the load's effect on amplifier loop dynamics. For instance, driving coaxial cables without an output series resistor may cause peaking or oscillation.

Transmission Line Matching

One method for matching the characteristic impedance of a transmission line is to place the appropriate resistor at the input or output of the amplifier. Figure 6 shows the typical circuit configurations for matching transmission lines.

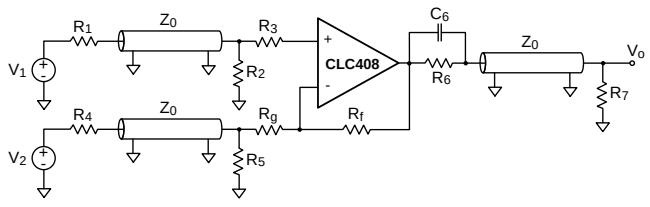


Figure 6: Transmission Line Matching

In non-inverting gain applications, R_g is connected directly to ground. The resistors R_1, R_2, R_6, and R_7 are equal to the characteristic impedance, Z_o, of the transmission line or cable. Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

In inverting gain applications, R_3 is connected directly to ground. The resistors R_4, R_6, and R_7 are equal to Z_o. The parallel combination of R_5 and R_g is also equal to Z_o.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. It compensates for the increase of the op amps output impedance with frequency.

Thermal Design

To calculate the power dissipation for the CLC408, follow these steps:

1) Calculate the no-load op amp power:
   $P_{amp} = I_{CC} \cdot (V_{CC} - V_{EE})$
2) Calculate the output stage's RMS power:
   $P_o = (V_{CC} - V_{load}) \cdot I_{load}$, where V_{load} and I_{load} are the RMS voltage and current across the external load
3) Calculate the total op amp RMS power:
   $P_t = P_{amp} + P_o$

To calculate the maximum allowable ambient temperature, solve the following equation: $T_{amb} = 175 - P_t \cdot \theta_{JA}$, where θ_{JA} is the thermal resistance from junction to ambient in °C/W, and T_{amb} is in °C. The ***Package Thermal Resistance*** section contains the thermal resistance for various packages.

Dynamic Range (input /output protection)

ESD diodes are present on all connected pins for protection from static voltage damage. For a signal that may exceed the supply voltages, we recommend using diode clamps at the amplifier's input to limit the signals to less than the supply voltages.

The CLC408's output current can exceed the maximum safe output current. To limit the output current to < 96mA:

- Limit the output voltage swing with diode clamps at the input
- Make sure that $\left|R_L\right| \geq \frac{V_{o(max)}}{I_{o(max)}}$

$V_{o(max)}$ is the output voltage swing limit, and $I_{o(max)}$ is the maximum safe output current.

Dynamic Range (input /output levels)

The ***Electrical Characteristics*** section specifies the Common-Mode Input Range and Output Voltage Range; these voltage ranges scale with the supplies. Output Current is also specified in the ***Electrical Characteristics*** section.

Unity gain applications are limited by the Common-Mode Input Range. At greater non-inverting gains, the Output Voltage Range becomes the limiting factor. Inverting gain applications are limited by the Output Voltage Range (and by the previous amplifier's ability to drive R_g). For transimpedance gain applications, the sum of the input currents injected at the inverting input pin of the op amp needs to be: $|I_{in}| \leq \frac{V_{max}}{R_f}$, where V_{max} is the Output Voltage Range (see the ***DC Gain (transimpedance)*** sub-section for details).

The equivalent output load needs to be large enough so that the output current can produce the required output voltage swing. See the ***DC Design (output loading)*** sub-section for details.

Dynamic Range (noise)
The output noise defines the lower end of the CLC408's useful dynamic range. Reduce the value of resistors in the circuit to reduce noise.

See the App Note ***Noise Design of CFB Op Amp Circuits*** for more details. Our SPICE models support noise simulations.

Dynamic Range (distortion)
The distortion plots in the ***Typical Performance Characteristics*** section show distortion as a function of load resistance, frequency, and output amplitude. Distortion places an upper limit on the CLC408's dynamic range.

The CLC408's output stage combines a voltage buffer with a complementary common emitter current source. The interaction between the buffer and the current source produces a small amount of crossover distortion. This distortion mechanism dominates at low output swing and low resistance loads. To avoid this type of distortion, use the CLC408 at high output swing.

Realized output distortion is highly dependent upon the external circuit. Some of the common external circuit choices that can improve distortion are:

- Short and equal return paths from the load to the supplies
- De-coupling capacitors of the correct value
- Higher load resistance

Printed Circuit Board Layout
High frequency op amp performance is strongly dependent on proper layout, proper resistive termination and adequate power supply decoupling. The most important layout points to follow are:

- Use a ground plane
- Bypass power supply pins with:
  - monolithic capacitors of about 0.1µF place less than 0.1" (3mm) from the pin
  - tantalum capacitors of about 6.8µF for large signal current swings or improved power supply noise rejection; we recommend a minimum of 2.2µF for any circuit
- Minimize trace and lead lengths for components between the inverting and output pins
- Remove ground plane underneath the amplifier package and 0.1" (3mm) from all input/output pads
- For prototyping, use flush-mount printed circuit board pins; ***never use high profile DIP sockets***.

Evaluation Board
Separate evaluation boards are available for proto-typing and measurements. Additional information is available in the evaluation board literature.

SPICE Models
SPICE models provide a means to evaluate op amp designs. Free SPICE models are available that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The ***readme*** file that accompanies the models lists the released models, and provides a list of modeled parameters. The application note ***Simulation SPICE Models for Comlinear's Op Amps*** contains schematics and detailed information.

CLC408 Applications

The circuit shown in the ***Typical Application*** schematic on the front page operates as a full duplex cable driver which allows simultaneous transmission and reception of signals on one transmission line. The circuit on either side of the transmission line uses the CLC408 as a cable driver, and the CLC426 as a receiver. V_{oA} is an attenuated version of V_{inA}, while V_{oB} is an attenuated version of V_{inB}.

R_{m1} is used to match the transmission line. R_{f2} and R_{g2} set the DC gain of the CLC426, which is used in a difference mode. R_{t2} provides good CMRR and DC offset. The CLC408 is shown in a unity gain configuration because it consumes the least power of any gain, for a given load. For proper operation we need $R_{f2} = R_{g2}$.

The receiver output voltages are:

$$V_{outA(B)} \approx V_{inA(B)} \cdot A + \frac{V_{inB(A)}}{2} \cdot \left(1 - \frac{R_{f2}}{R_{g2}} + \frac{Z_{o(408)}(j\omega)}{R_{m1}}\right)$$

where A is the attenuation of the cable, $Z_{o(408)}(j\omega)$ is the output impedance of the CLC408 (see the ***Closed-Loop Output Resistance*** plot), and $|Z_{o(408)}(j\omega)| << R_{m1}$.

We selected the component values as follows:

- R_{f1} = 3.0kΩ, for unity gain of the CLC408
- $R_{m1} = Z_o$ = 50Ω, the characteristic impedance of the transmission line
- $R_{f2} = R_{g2}$ = 100Ω ≥ R_{m1}, the recommended value for the CLC426 at A_V = 2
- $R_{t2} = (R_{f2} \,||\, R_{g2}) - \frac{R_{m1}}{2} = 25\Omega$

These values give excellent isolation from the other input:

$$\frac{V_{oA(B)}}{V_{inB(A)}} \approx -38\text{dB},\ f = 5.0\text{MHz}$$

The CLC408 provides large output current drive, while consuming little supply current, at the nominal bias point. It also produces low distortion with large signal swings and heavy loads. These features make the CLC408 an excellent choice for driving transmission lines. The CLC426 was used as the receiver because it has good high frequency CMRR.

Precision, Low 1/f Noise Composite Amplifier

The circuit in Figure 7 has the DC precision and low-frequency performance of U1, and the high-frequency performance of U2. This means that the 1/f noise performance is dominated by U1, not U2. Vin needs to be a low impedance source to minimize the impact of U2's non-inverting bias current (I_{BN}) and current noise (i_{bn}). R_1 is an optional resistor that terminates the source. The potentiometer R_7 allows the gain at low frequencies to be manually matched to the gain at high frequencies.

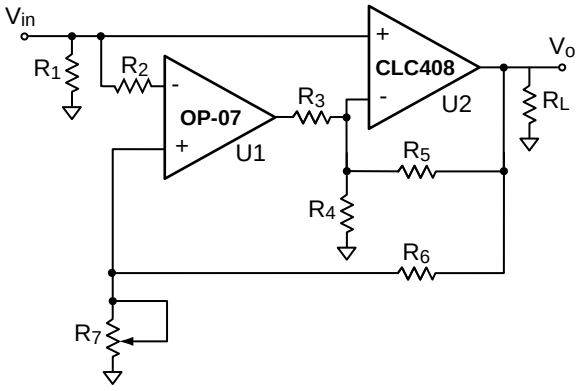


Figure 7: Precision, Low-Noise Composite Amplifier

U1 needs to be an op amp with the following features: voltage-feedback, low bandwidth (compared to U2), low DC offsets and low 1/f noise. National Semiconductor's OP-07 meets all of these requirements.

U2 is a high-frequency op amp that meets your high-frequency requirements. This application circuit will assume a current-feedback op amp (the CLC408) for U2. This circuit also works well when U2 is a high-frequency, voltage-feedback op amp (such as the CLC425 or CLC428).

The transfer function is:

$$\frac{V_o}{V_{in}} = \frac{\left(1+\frac{R_5}{R_3}+\frac{R_5}{R_4}\right)+A_{U1}(j\omega)\cdot\left(\frac{R_5}{R_3}\right)}{\left(1+\frac{R_5}{Z_{U2}(j\omega)}\right)+A_{U1}(j\omega)\cdot\left(\frac{R_5}{R_3}\cdot\frac{R_7}{R_6+R_7}\right)}$$

$$\approx 1+\frac{R_5}{R_3},\ |A_{U1}(j\omega)| >> 1$$

$$\approx \frac{1+\frac{R_5}{R_3}+\frac{R_5}{R_4}}{1+\frac{R_5}{Z_{U2}(j\omega)}},\ |A_{U1}(j\omega)| << 1$$

where $A_{U1}(j\omega)$ is the open-loop voltage gain of U1, and $Z_{U2}(j\omega)$ is the open-loop transimpedance gain of U2. The approximations hold when the bandwidth of U1 is much less than the bandwidth of U2. Now the gain of the composite amplifier can be selected:

$$A_V = 1+\frac{R_6}{R_7} = 1+\frac{R_5}{R_3}+\frac{R_5}{R_4}$$

A_v must be within the stable gain range of U1.

Make R_2, R_6 and R_7 small so that they produce little thermal noise, but large enough to not overload the output of U2. Minimize the input offset voltage by making $R_2 = (R_6 \,||\, R_7)$:

$$R_6 = A_v R_2$$

$$R_7 \approx \frac{R_6}{A_v - 1}\text{, the value for gain flatness}$$

The potentiometer should have a maximum value about double the value calculated for R_7. Use a potentiometer with multiple turn capability, and low parasitics. Replace R_7 with a resistor when AC gain and step response flatness are not a concern.

Set R_5 to the recommended feedback resistor value for the CLC408 at a gain of A_v.

Select R_3 and R_4 so that the high-frequency gain is correct, and so that any change in output impedance of U1 has a minimal impact:

$$\frac{R_3}{R_4} >> 1$$

$$R_3 = \frac{R_5}{A_v}\cdot\left(1+\frac{R_3}{R_4}\right)$$

The selection of R_3 and R_4 affects the frequency where U2 starts to dominate the performance of the composite amplifier. This frequency is approximately:

$$f_{UG} \approx \frac{R_5}{R_3}\cdot\frac{R_7}{R_6+R_7}\cdot GBWP_{U1}$$

where $GBWP_{U1}$ is the Gain-Bandwidth Product of U1. As R_3 is made larger, f_{UG} becomes smaller. f_{UG} should be large enough so that U2's 1/f noise does not significantly impact the output noise.

Adjust R_7 so that the gain at $f << f_{UG}$ matches the gain at $f >> f_{UG}$.

Precision Half-Wave Rectifier

Figure 8 shows a precision half-wave rectifier. When $V_{in} > 0$, D_1 is on and D_2 is off. When $V_{in} < 0$, D_1 is off and D_2 is on. The second amplifier (U2) buffers V_o from the variable output impedance of the rectifier.

The output voltage is:

$$V_o = \begin{cases} 0, V_{in} < 0 \\ -\frac{R_2}{R_1} \cdot \left(1 + \frac{R_6}{R_5}\right) \cdot V_{in}, V_{in} > 0 \end{cases}$$

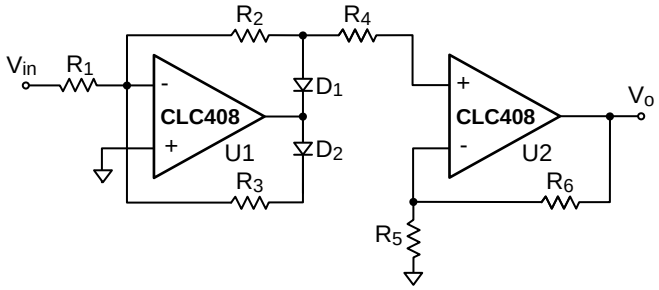


Figure 8: Precision Half-Wave Rectifier

Diodes D_1 and D_2 need to be Schottky or PIN diodes to minimize delay.

Set $R_2 = R_3$ to the recommended feedback resistor value for the gain $A_v = -R_2/R_1$. R_2 and R_3 may need to be increased slightly to compensate for the delays through D_1 and D_2.

Set R_6 to the recommended feedback resistor value for the gain $A_v = (1 + R_6/R_5)$.

R_4 is an optional resistor; it helps isolate U2's input from the changing output impedance of U1.

Other configurations are possible:

1) Connect U2's input between R_3 and D_2 so that $V_o \neq 0$ for $V_{in} < 0$.
2) Use an inverting gain configuration for U2 to change the polarity of V_o.

Pick the combination that best suits your needs.

This page intentionally left blank.

Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at **1-800-272-9959** or fax **1-800-737-7018**.

Life Support Policy

National's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of National Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
E-mail: europe.support.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Francais Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block
Ocean Centre, 5 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408