CLC426

CLC426 Wideband, Low Noise, Voltage Feedback Op Amp

Texas Instruments

Literature Number: SNOS821D

National Semiconductor

July 2001

CLC426
Wideband, Low Noise, Voltage Feedback Op Amp

General Description

The National CLC426 combines an enhanced voltage feedback architecture with an advanced complimentary bipolar process to provide a high speed op amp with very low noise ($1.6nV/\sqrt{Hz}$ & $2.0pA/\sqrt{Hz}$) and distortion (−62dBc/−68dBc 2nd/3rd harmonics at $1V_{PP}$ and 10MHz).

Providing a wide 230MHz gain bandwidth product, a fast 400V/µs slew rate and very quick 16ns settling time to 0.05%, the CLC426 is the ideal choice for high speed applications requiring a very wide dynamic range such as an input buffer for high resolution analog-to-digital converters.

The CLC426 is internally compensated for gains ≥ 2V/V and can easily be externally compensated for unity gain stability in applications such as wideband low noise integrators. The CLC426 is also equipped with external supply current adjustment which allows the user to optimize power, bandwidth, noise and distortion performance for each application.

The CLC426's combination of speed, low noise and distortion and low dc errors will allow high speed signal conditioning applications to achieve the highest signal-to-noise performance. To reduce design times and assist board layout, the CLC426 is supported by an evaluation board and SPICE simulation model available from National.

For even higher gain-bandwidth voltage-feedback op amps see the 1.9GHz CLC425 (A_V ≥10V/V) or the 5.0GHz CLC422 (A_V ≥ 30V/V).

Enhanced Solutions (Military/Aerospace

SMD Number: 5962-94597

*Space level versions also available.

*For more information, visit http://www.national.com/mil

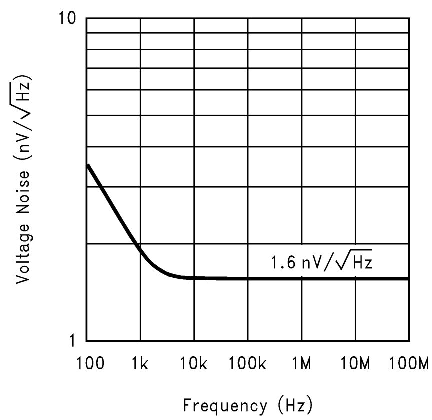
Features

- Wide gain-bandwidth product: 230MHz
- Ultra low input voltage noise: $1.6nV/\sqrt{Hz}$
- Very low harmonic distortion: −62/−68dBc
- Fast slew rate: 400V/µs
- Adjustable supply current
- Dual ±2.5 to ±5V or single 5 to 12V supplies
- Externally compensatable

Applications

- Active filters & integrators
- Ultrasound
- Low power portable video
- ADC/DAC buffer
- Wide dynamic range amp
- Differential amps
- Pulse/RF amp

Input Voltage Noise Density



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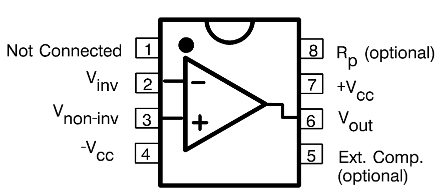
Connection Diagram



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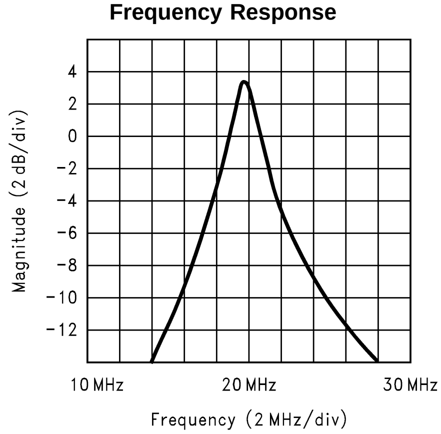
Pinout
DIP & SOIC

Frequency Response



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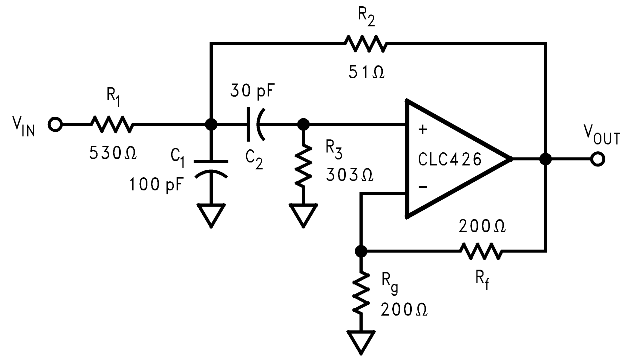
Typical application



Wide Dynamic Range Sallen-Key Band Pass Filter 2nd-Order (20MHz, Q = 10, G = 2)

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-Pin Plastic DIP	−40˚C to +85˚C	CLC426AJP	CLC426AJP	N08E
8-Pin Plastic SOIC	−40˚C to +85˚C	CLC426AJE	CLC426AJE	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±7V
Short Circuit Current	(Note 6)
Common-Mode Input Voltage	$\pm V_{cc}$
Differential Input Voltage	±10V
Maximum Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering 10 sec)	+300˚C
ESD	2000V

Electrical Characteristics

(V_{CC} = ±5; A_V = +2V/V; R_f = 100Ω; R_L = 100Ω; unless noted)

Notes	Parameters	Conditions	Typ	Max/Min Ratings (Note 2)			Units
	Ambient Temperature	CLC426	+25˚C	+25˚C	0 to+70˚C	−40 to+85˚C	
Frequency Domain Response							
	Gain Bandwidth Product	V_{OUT} < $0.5V_{PP}$	230	170	120	100	MHz
(Note 4), (Note 5), (Note 8)	−3dB Bandwidth, A_V = +2	V_{OUT} < $0.5V_{PP}$	130	90	70	55	MHz
		V_{OUT} < $5.0V_{PP}$	50	25	22	20	MHz
	Gain Flatness	V_{OUT} < $0.5V_{PP}$					
(Note 4), (Note 8)	Peaking	DC to 200MHz	0.6	1.5	2.2	2.5	dB
(Note 4), (Note 8)	Rolloff	DC to 30MHz	0.0	0.6	1.0	1.0	dB
	Linear Phase Deviation	DC to 30MHz	0.2	1.0	1.5	1.5	deg
Time Domain Response							
	Rise and Fall Time	1V Step	2.3	3.5	5.0	6.5	ns
	Settling Time	2V Step to 0.05%	16	20	24	24	ns
	Overshoot	1V Step	5	15	15	18	%
	Slew Rate	5V Step	400	300	275	250	V/µs
Distortion And Noise Response							
(Note 3)	2nd Harmonic Distortion	$1V_{PP}$,10MHz	−62	−52	−47	−45	dBc
(Note 3)	3rd Harmonic Distortion	$1V_{PP}$,10MHz	−68	−58	−54	−54	dBc
	Equivalent Input Noise	Op Amp Only					
	Voltage	1MHz to 100MHz	1.6	2.0	2.3	2.6	$nV/\sqrt{Hz}$
	Current	1MHz to 100MHz	2.0	3.0	3.6	4.6	$pA/\sqrt{Hz}$
Static DC Performance							
	Open-Loop Gain	DC	64	60	54	54	dB
(Note 3)	Input Offset Voltage		1.0	2.0	2.8	2.8	mV
	Average Drift		3	–	10	10	µV/˚C
(Note 3)	Input Bias Current		5	25	40	65	µA
	Average Drift		90	–	600	700	nA/˚C
(Note 3)	Input Offset Current		0.3	3	5	5	µA
	Average Drift		5	–	25	50	nA/˚C
(Note 4)	Power-Supply Rejection Ratio	DC	73	65	60	60	dB
	Common-Mode Rejection Ratio	DC	70	62	57	57	dB
(Note 3)	Supply Current	Pin #8 Open, $R_L = \infty$	11	12	13	15	mA
Miscellaneous Performance							
	Input Resistance	Common-Mode	500	250	125	125	kΩ
		Differential-Mode	750	200	50	25	kΩ
	Input Capacitance	Common-Mode	2.0	3.0	3.0	3.0	pF
		Differential-Mode	2.0	3.0	3.0	3.0	pF

Electrical Characteristics (Continued)

(V_{CC} = ±5; A_V = +2V/V; R_f = 100Ω; R_L = 100Ω; unless noted)

Notes	Parameters	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Miscellaneous Performance							
	Output Resistance	Closed Loop	0.07	0.1	0.2	0.2	Ω
	Output Voltage Range	R_L = ∞	±3.8	±3.5	±3.3	±3.3	V
		R_L = 100Ω	±3.5	±3.2	±2.6	±1.3	V
	Input Voltage Range	Common Mode	±3.7	±3.5	±3.3	±3.3	V
	Output Current		±70	±50	±40	+35, −20	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: J-level: spec. is 100% tested at +25˚C, sample at 85˚C. L-level: spec. is 100% wafer probed at 25˚C.

Note 4: J-level: spec is sample tested at 25˚C

Note 5: Minimum table stable gain with out external compensation is +2 or −1V/V, the CLC426 unity-gain stable with external compensation.

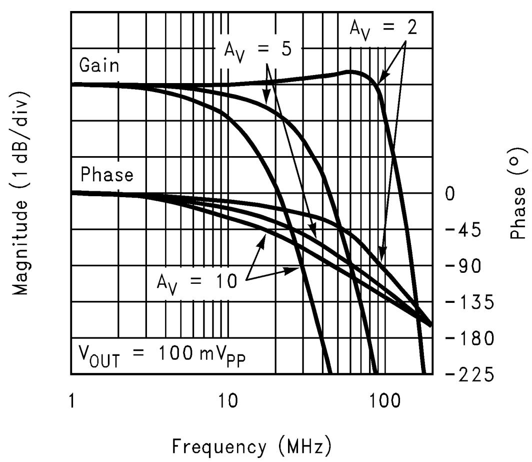
Note 6: Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 160mA

Note 7: See test for compensation techniques.

Note 8: Spec is guaranteed to $0.5V_{PP}$ but tested with $0.1V_{PP}$

Typical Performance Characteristics (T_A = 25˚C, ± V_{CC} = ±5V, A_V = +2, R_f = 100Ω, R_L = 100Ω, unless noted)

Non-Inverting Frequency Response



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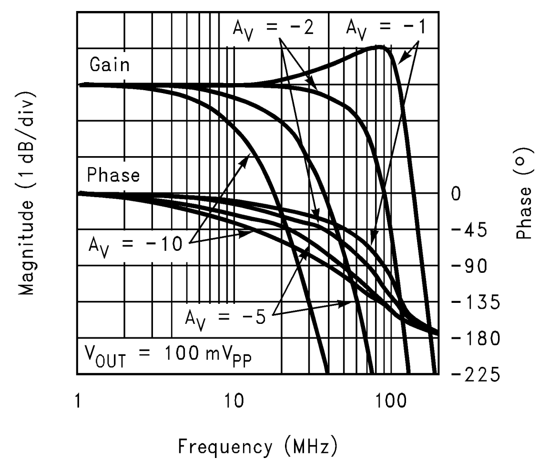
Inverting Frequency Response



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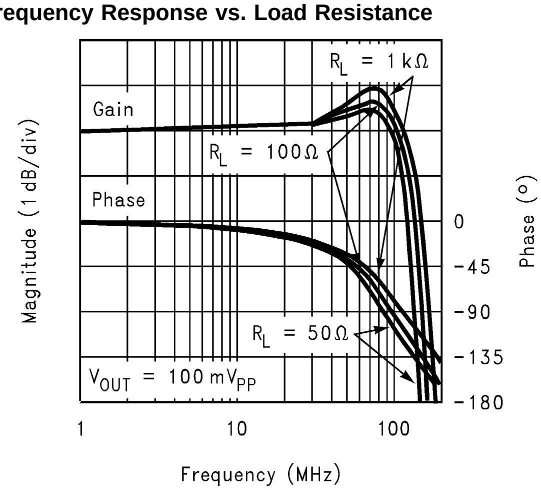
Frequency Response vs. Load Resistance



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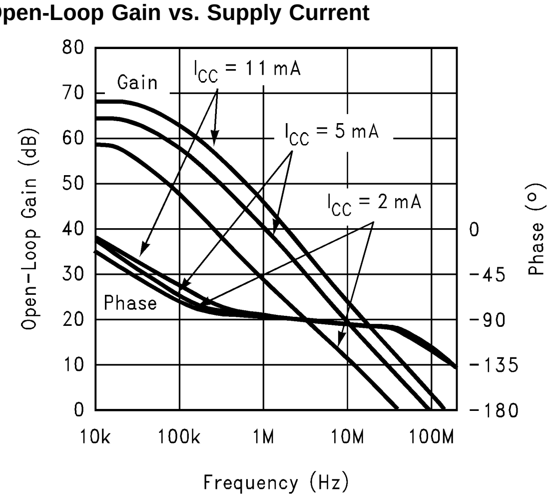
Open-Loop Gain vs. Supply Current



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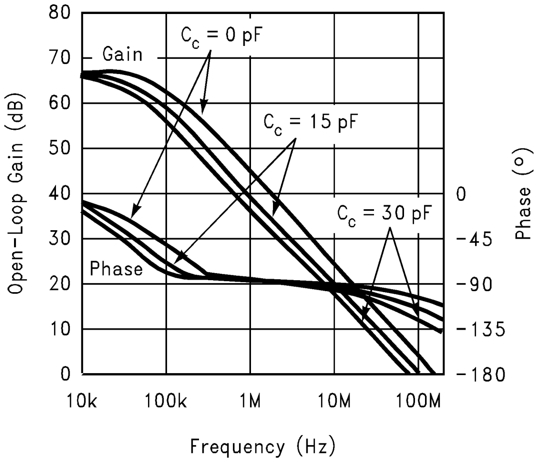
Typical Performance Characteristics (T_A = 25˚C, ± V_{CC} = ±5V, A_V = +2, R_f = 100Ω, R_L = 100Ω, unless noted) (Continued)

Open-Loop Gain vs. Compensation Cap.



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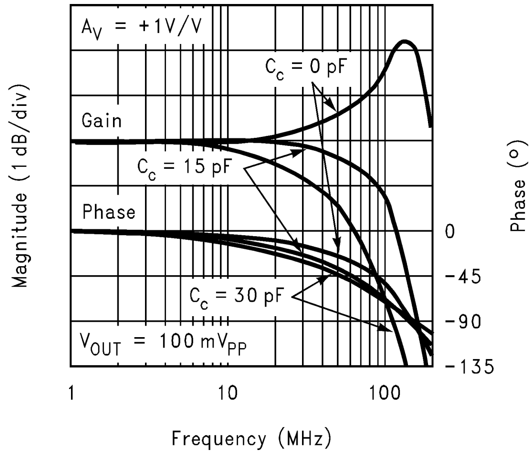
Frequency Response vs. Compensation Cap.



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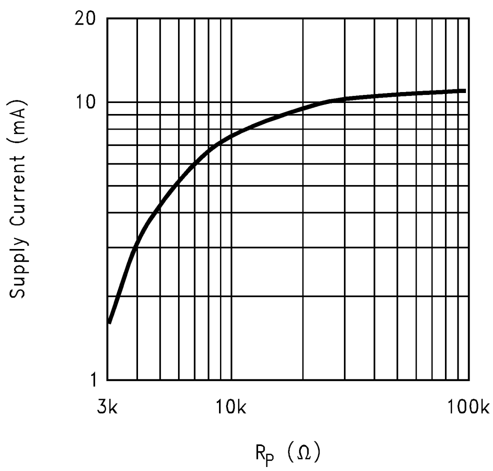
Supply Current vs. Rp



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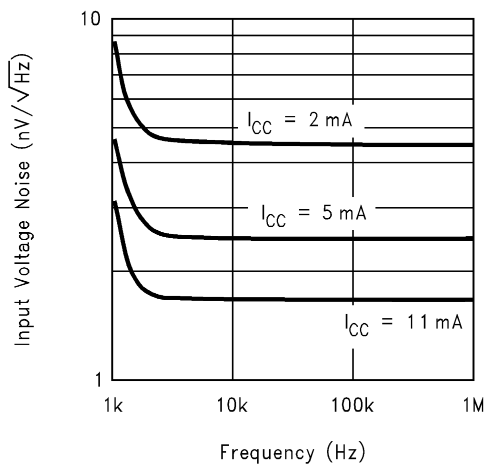
Voltage Noise vs. Supply Current



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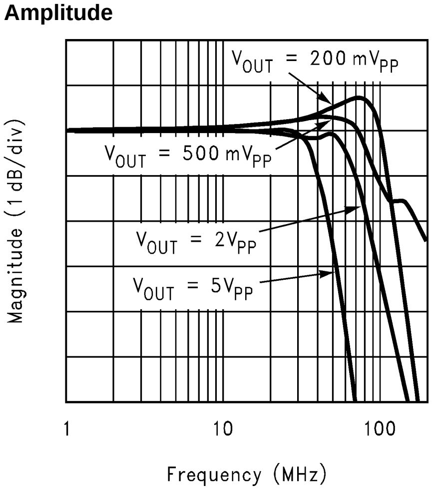
Frequency Response vs. Output Amplitude



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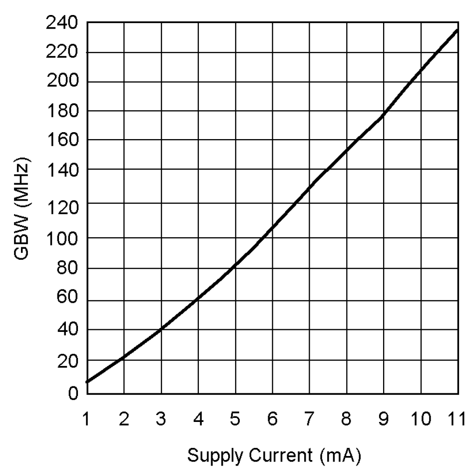
Gain-Bandwidth Product vs Supply Current



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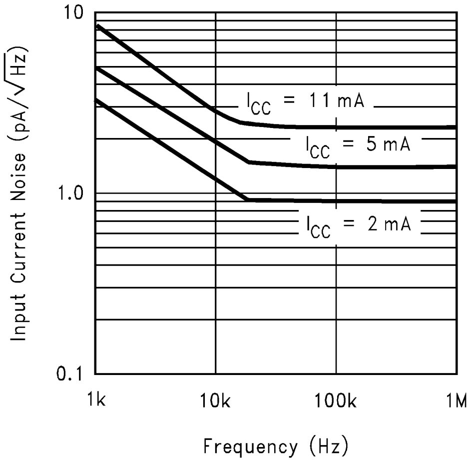
Typical Performance Characteristics (T_A = 25˚C, ± V_{CC} = ±5V, A_V = +2, R_f = 100Ω, R_L = 100Ω, unless noted) (Continued)

Current Noise vs. Supply Current



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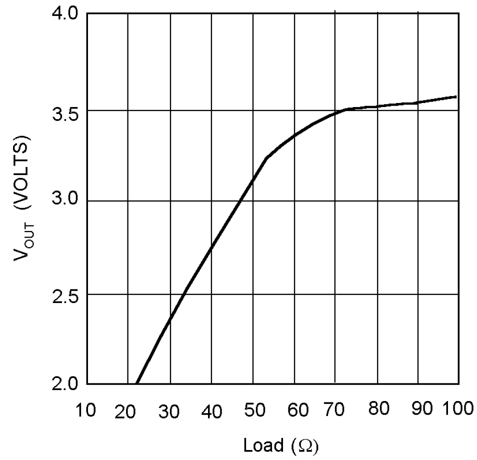
Maximum Output Voltage vs. Load



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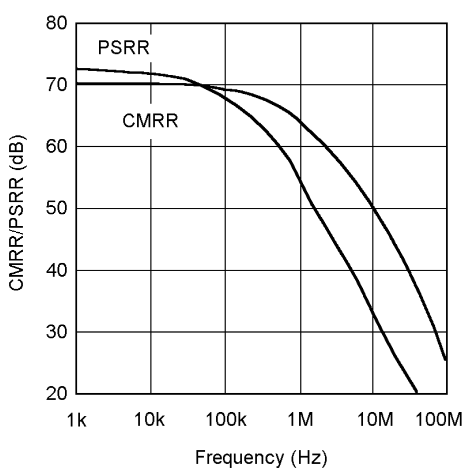
CMRR and PSRR



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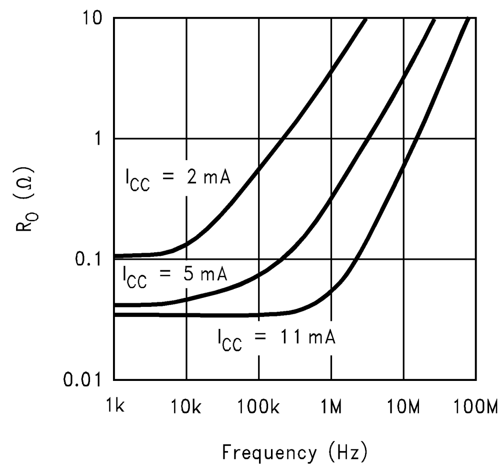
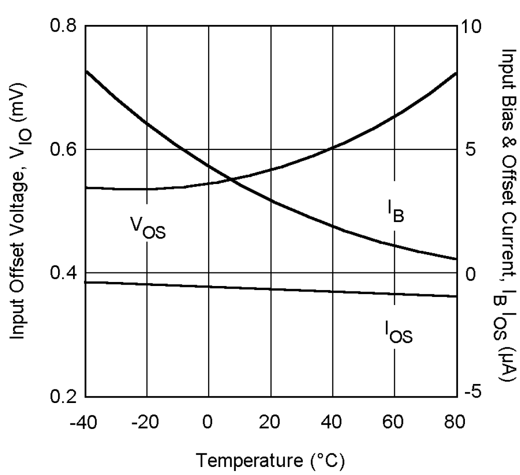
Closed-Loop Output Resistance



DS012709-18

Typical DC Errors vs. Temperature



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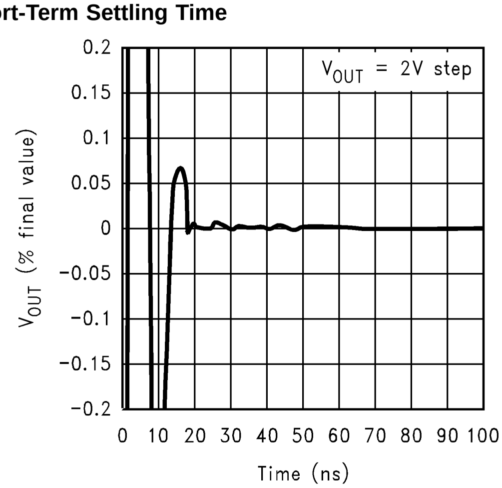
Short-Term Settling Time



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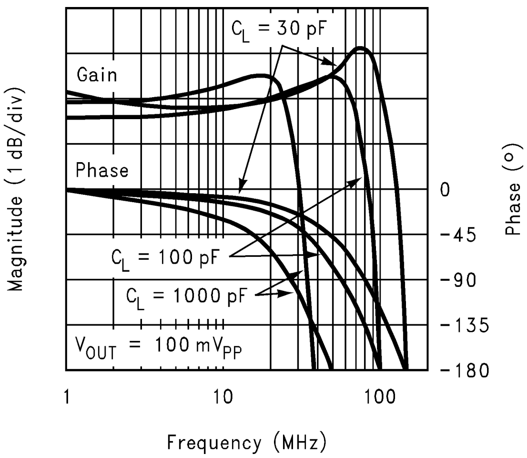
Typical Performance Characteristics (T_A = 25˚C, ± V_{CC} = ±5V, A_V = +2, R_f = 100Ω, R_L = 100Ω, unless noted) (Continued)

Frequency Response vs. Capacitive Load



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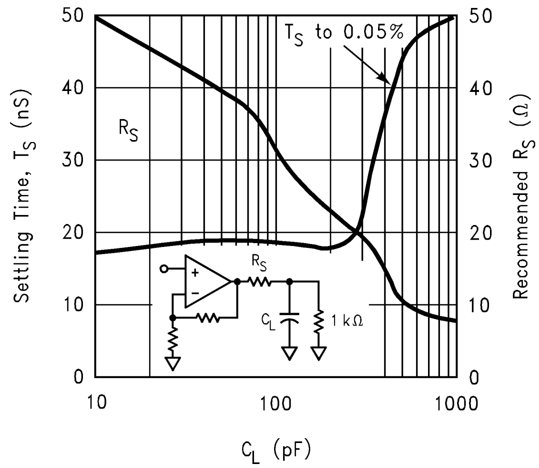
Settling Time vs. Capacitive Load



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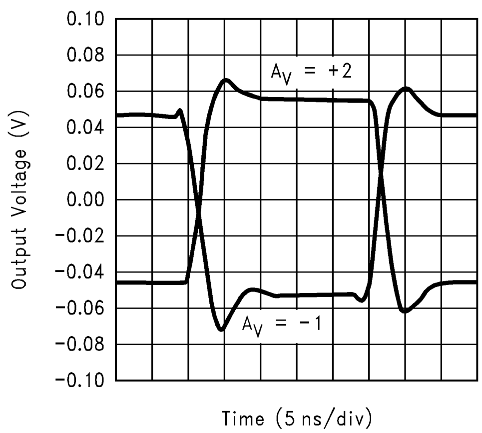
Pulse Response (V_{OUT} = 100mV$_{PP}$)



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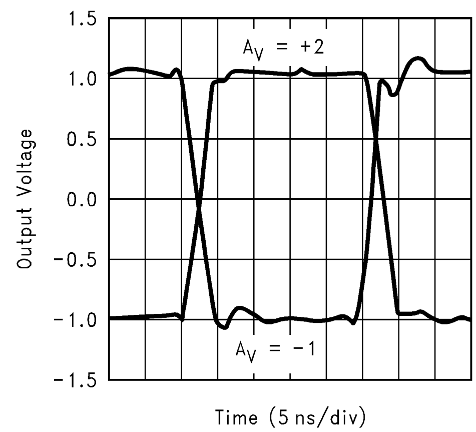
Pulse Response (V_{OUT} = 2V$_{PP}$)



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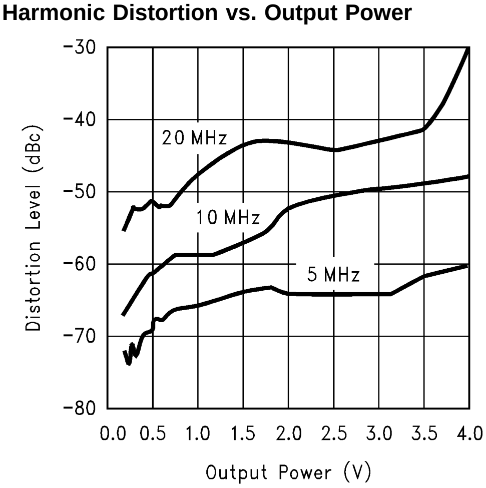
2nd Harmonic Distortion vs. Output Power



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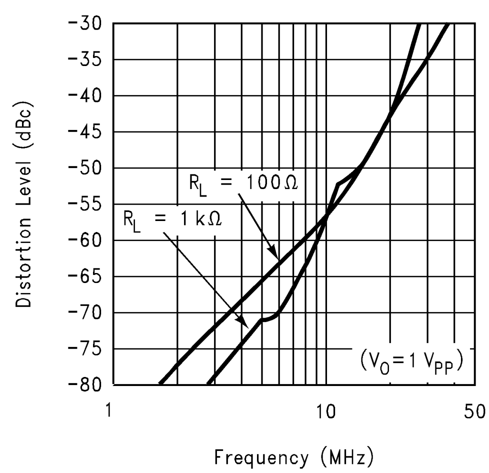
2nd Harmonic Distortion



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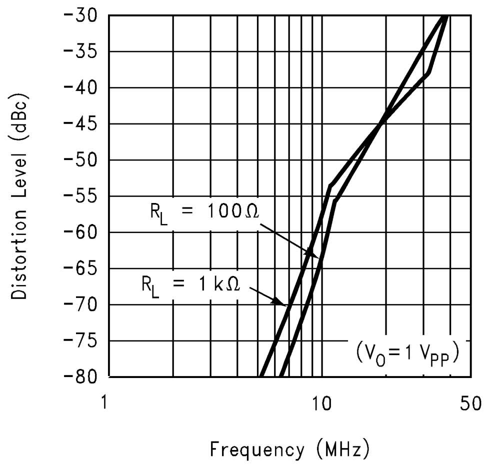
Typical Performance Characteristics (T_A = 25˚C, ± V_{CC} = ±5V, A_V = +2, R_f = 100Ω, R_L = 100Ω, unless noted) (Continued)

3rd Harmonic Distortion



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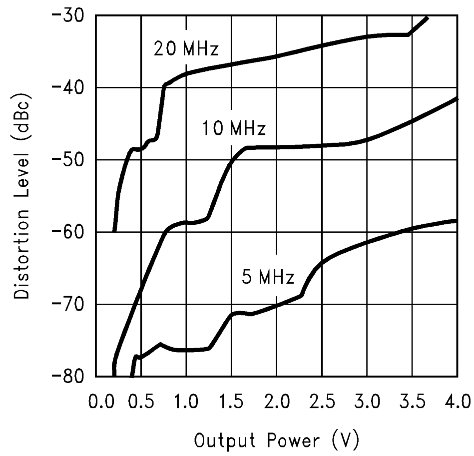
3rd Harmonic Distortion vs. Output Power



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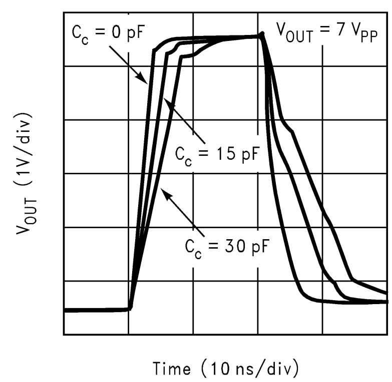
Application Discussion

Introduction

The CLC426 is a wide bandwidth voltage-feedback operational amplifier that is optimized for applications requiring wide dynamic range. The CLC426 features adjustable supply current and external compensation for the added flexibility of tuning its performance for demanding applications. The Typical Performance section illustrates many of the performance trade-offs. Although designed to operate from ±5Volt power supplies, the CLC426 is equally impressive operating from a single +5V supply. The following discussion will enable the proper selection of external components for optimum device performance in a variety of applications.

External Compensation

The CLC426 is stable for noise gains ≥2V/V. For unity-gain operation, the CLC426 requires an external compensation capacitor (from pin 5 to ground). The plot located in the Typical Performance section labeled “Frequency Response vs. Compensation Cap.” illustrates the CLC426’s typical AC response for different values of compensation capacitor. From the plot it is seen that a value of 15pF produces the optimal response of the CLC426 at unity gain. The plot labeled “Open-Loop Gain vs. Compensation Cap.” illustrates the CLC426’s open-loop behavior for various values of compensation capacitor. This plot also illustrates one technique of bandlimiting the device by reducing the open-loop gain resulting in lower closed-loop bandwidth. *Figure 1* shows the effect of external compensation on the CLC426’s pulse response.



DS012709-29

FIGURE 1.

Supply Current Adjustment

The CLC426’s supply current can be externally adjusted downward from its nominal value to less than 2mA by adding an optional resistor (R_p) between pin 8 and the negative supply as shown in *Figure 2*. The plot labeled “Open-Loop Gain vs. Supply Current” illustrates the influence that supply current has over the CLC426’s open-loop response. From the plot it is seen that the CLC426 can be compensated for unity-gain stability by simply lowering its supply current. Therefore lowering the CLC426’s supply current effectively reduces its open-loop gain to the point that there is adequate phase margin at unity gain crossover. The plot labeled “Supply Current vs. R_p” provides the means for selecting the value of R_p that produces the desired supply current. The curve in the plot represents nominal processing but a ±12% deviation over process can be expected. The two plots labeled “Voltage Noise vs. Supply Current” and “ Current Noise vs. Supply Current” illustrate the CLC426 supply current’s effect over its input-referred noise characteristics.

Application Discussion (Continued)

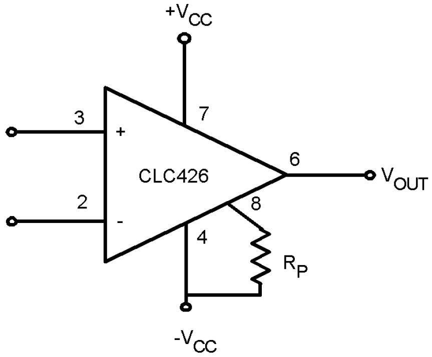


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FIGURE 2.

Driving Capacitive Loads

The CLC426 is designed to drive capacitive loads with the addition of a small series resistor placed between the output and the load as seen in *Figure 3*. Two plots located in the Typical Performance section illustrate this technique for both frequency domain and time domain applications. The plot labeled "Frequency Response vs. Capacitive Load" shows the CLC426's resulting AC response to various capacitive loads. The values of R_s in this plot were chosen to maximize the CLC426's AC response (limited to ≤1dB peaking).

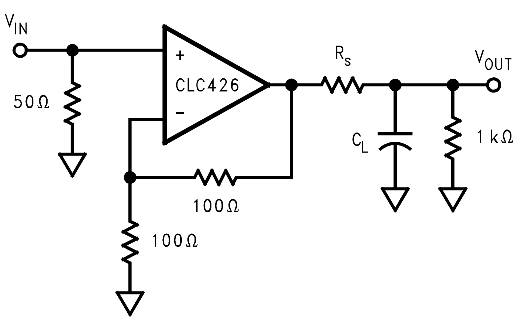

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FIGURE 3.

The second plot labeled "Settling Time vs. Capacitive Load" provides the means for the selection of the value of R_s which minimizes the CLC426's settling time. As seen from the plot, for a given capacitive load R_s is chosen from the curve labeled "R_s". The resulting settling time to 0.05% can then be estimated from the curve labeled "T_s to 0.05%". The plot of *Figure 4* shows the CLC426's pulse response for various capacitive loads where R_s has been chosen from the plot labeled "Settling Time vs. Capacitive Load".

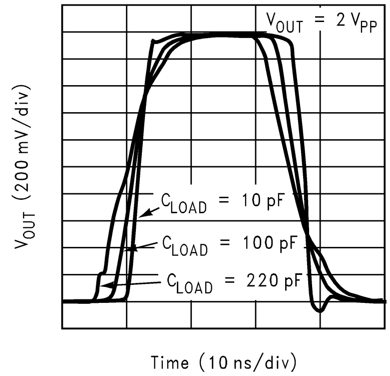

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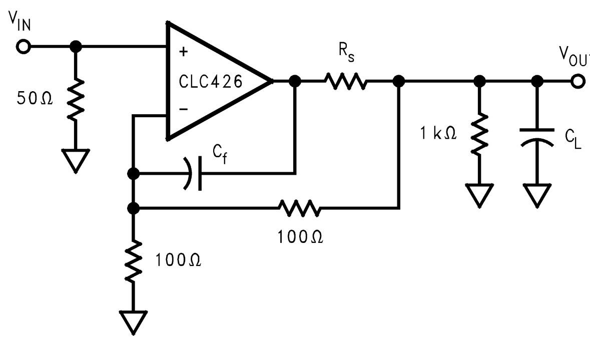
FIGURE 4.

Faster Settling

The circuit of *Figure 5* shows an alternative method for driving capacitive loads that results in quicker settling times. The small series resistor, R_s, is used to decouple the CLC426's open-loop output resistance, R_{out}, from the load capacitance. The small feedback capacitance, C_f, is used to provide a high frequency bypass between the output and inverting input. The phase lead introduced by C_f compensates for the phase lag due to C_L and therefore restores stability. The following equations provide values of R_s and C_f for a given load capacitance and closed-loop amplifier gain.



DS012709-33

FIGURE 5.

$$R_s = R_{OUT}\left(\frac{R_f}{R_g}\right); \text{ where } R_{OUT} \approx 6\,\Omega \qquad (1)$$

$$C_1 = \left[1 + \left[\frac{R_f}{R_g}\right]\right]^2 C_L \left[\frac{R_{OUT}}{R_g}\right] \qquad (2)$$

The plot in *Figure 6* shows the result of the two methods of capacitive load driving mentioned above while driving a 100 pF||1kΩ load.

Application Discussion (Continued)

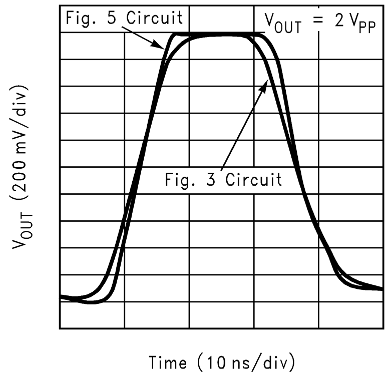


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FIGURE 6.

Single Supply Operation

The CLC426 can be operated with single power supply as shown in *Figure 7* . Both the input and output are capacitively coupled to set the dc operating point.

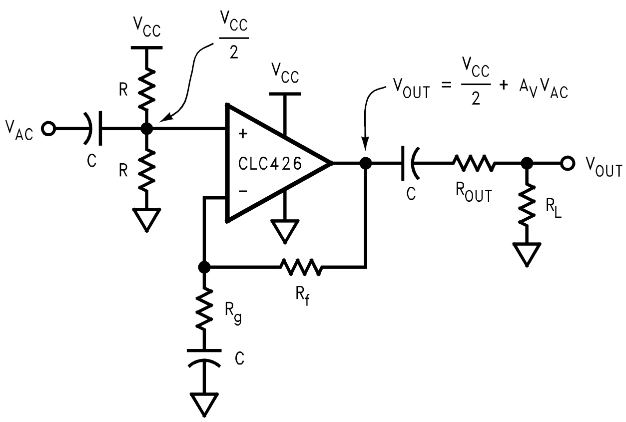

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FIGURE 7.

DAC Output Buffer

The CLC426's quick settling, wide bandwidth and low differential input capacitance combine to form an excellent I-to-V converter for current output DACs in such applications as reconstruction video. The circuit of *Figure 8* implements a low noise transimpedance amplifier commonly used to buffer high speed current output devices. The transimpedance gain is sent by R_f. A feedback capacitor, C_f, is needed in order to compensate for the inductive behavior of the closed-loop frequency response of this type of circuit.

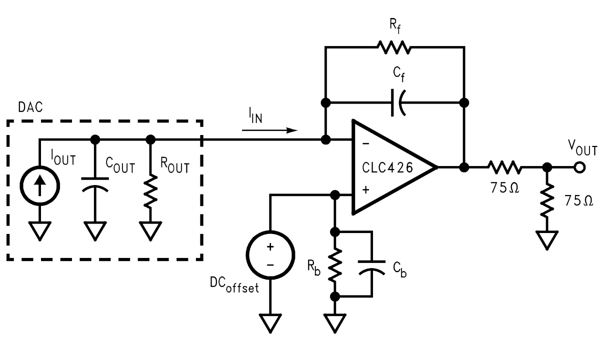

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FIGURE 8.

Equation 3 shows a means of calculating the value of C_f which will provide conditions for a maximally flat signal frequency response with approximately 65˚ phase margin and 5% step response overshoot. Notice that C_t is the sum of the DAC output capacitance and the differential input capacitance of the CLC426 which is located in its Electrical Characteristics Table. Notice also that CLC426's gain bandwidth product (GBW) is also located in the same table. Equation 5 provides the resulting signal bandwidth.

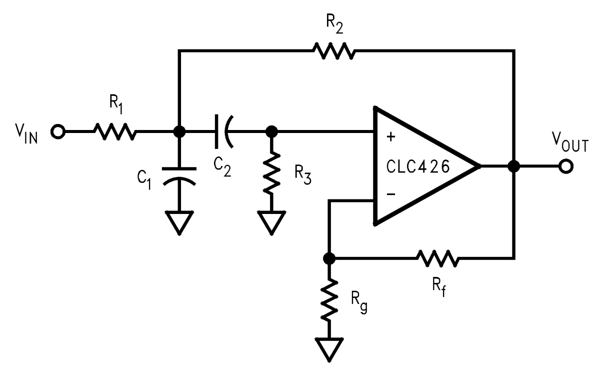
$$C_f = 2\sqrt{\frac{C_t}{2\pi R_f GBW}} \tag{3}$$

$$C_T = C_{OUT} + C_{IN\ DIF}$$

$$\text{signal bandwidth} = \frac{1}{2}\sqrt{\frac{GBW}{2\pi R_f C_t}} \tag{4}$$

Sallen-Key Active Filters

The CLC426 is well suited for Sallen-Key type of active filters. shows the 2nd order Sallen-Key band-pass filter topology and design equations.



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$$C_2 = \frac{1}{5} C_1$$

$$G = 1 + \frac{R_f}{R_g}\text{, desired mid-band gain}$$

$$R_1 = 2\frac{Q}{GC_1(2\pi f)}\text{, where f = desired center frequency}$$

$$R_2 = \frac{GR_1\left(\sqrt{1 + 4.8Q^2 - 2G + G^2} + 1\right)}{4.8Q^2 - 2G + G^2}$$

$$R_3 = \frac{5GR_1\left(\sqrt{1 + 4.8Q^2 - 2G + G^2} + G - 1\right)}{4Q^2}$$

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FIGURE 9.

To design the band-pass, begin by choosing values for R_f and R_g, for example $R_f = R_g = 200\Omega$. Then chosen reasonable values for $C_1$and C_2 (where $C_1 = 5C_2$) and then computer R_1. R_2 and R_3 can then be computed. For optimum high frequency performance it is recommended that the resistor values fall in the range of 10Ω to 1kΩ and the capacitors be kept above 10pF. The design can be further

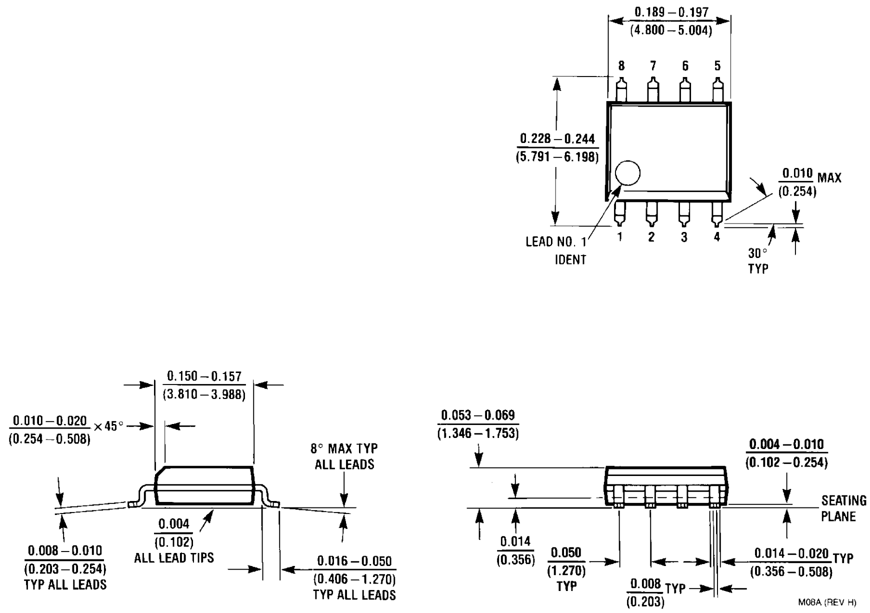
Application Discussion (Continued)

improved by compensating for the delay through the op amp. For further details on this technique, please request Application Note OA−21 from National Semiconductor Corporation.

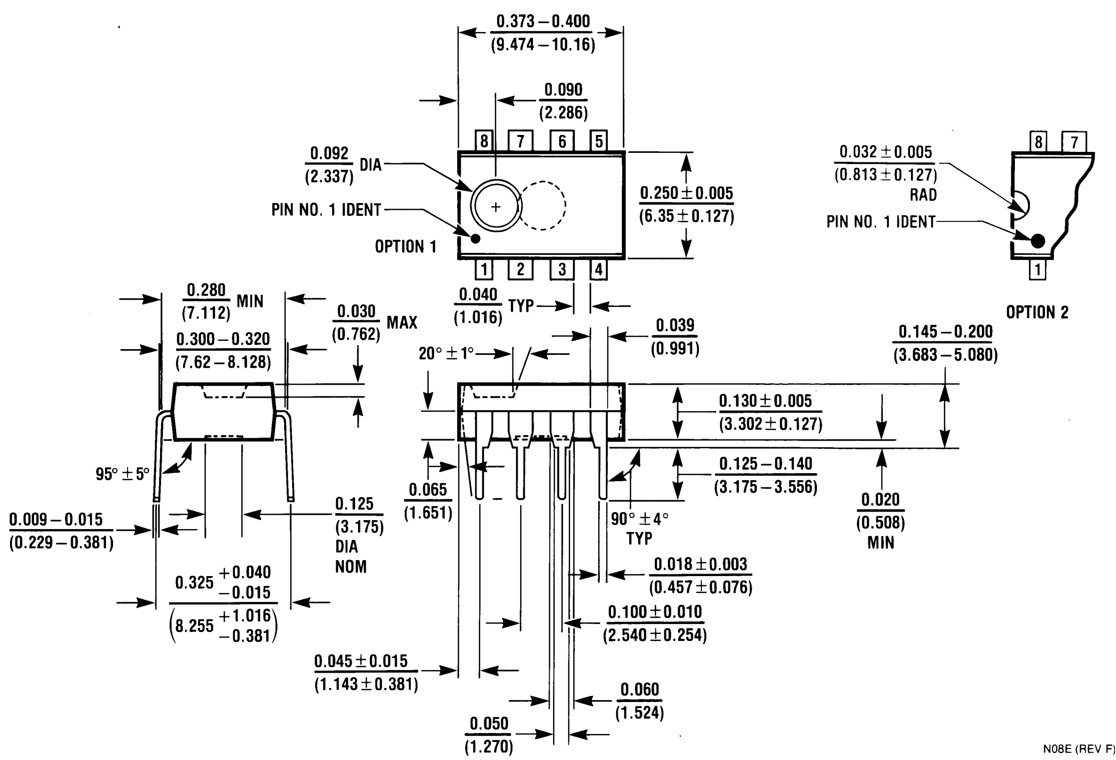
Printed Circuit Layout

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillation, see OA-15 for more information. National suggests the 730013 (through-hole) or the 730027 (SOIC) evaluation board as a guide for high frequency layout and as an aid in device testing and characterization.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



8-Pin MDIP
NS Package Number N08E

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