Embedded DRAM

Functional Summary

- Two configurations: x 256 or x 292
- 1 Mb to 16 Mb in 1 Mb increments
  - Multiple macros per chip for greater capacity or functional flexibility
  - Additional width for parity
- Data I/O organization:

x 256 configuration	- 256-bit data in with 256-bit write mask - 256-bit data out
x 292 configuration	- 292-bit data in with 292-bit write mask - 292-bit data out

- Broadside addressing for macro single bank operation
  - 16-bit address
    - Three bit (eight transfer) low-order page addressing
  - Random access and page access modes
- Multi 1 Mb bank interleaving for additional functional flexibility
  - Row/column addressing for multi bank operation
  - Bank-to-bank interleave operation: 4.0 ns, 250 MHz clock rate
- Performance at worst case process and voltage[1]
  - Random access mode: 11 ns access, 60 MHz clock cycle
  - Page access mode: 5.25 ns access, 182 MHz clock cycle
  - Bank-to-bank interleave operation: 5.25 ns, 182 MHz clock rate
  - 2 pF data out drive
- 3.2 ms refresh period (T_{ref}) at T_j = 0°C to 105°C
  - Distributed refresh, burst refresh, or a combination of distributed and burst refresh are allowed, provided that all word addresses are refreshed within the specified refresh period
- Row and column redundancy
  - Eight data lines can be replaced in every 1 Mb block
  - Eight word lines can be replaced in every 1 Mb block
- 1.2 V $\pm$ 0.10 V operation or 1.5 V $\pm$ 0.10 V operation
- Full memory BIST
  - Single pass test on logic tester
  - In-macro redundancy calculation
  - *In situ* memory burn-in capability

1. The embedded DRAM supports a junction temperature (T_j) range of 0°C to 105°C.

- Wiring
  - Blocked through M3
  - Signal connections at M1; power connections at M1–M3
  - Address, control, data pins located along one side and repeat on logic cell height pitch
  - Macro can be mirrored horizontally and/or vertically, but not rotated
- VHDL, Verilog, Synopsys, LEF, and VIM models provided

Related Documentation

For more information on using Cu-11 embedded DRAMs, refer to the following IBM application notes:

- *Embedded DRAMs in Cu-11*
- *Cu-11 Embedded DRAM General Usage Restrictions and Die-Sizing Guidelines*
- *Pin Sharing: How to Combine Test and System I/O Functions on a Single Pin*
- *ASIC I/O Test Considerations*

Macro Sizes

Table 1. Embedded DRAM Macro Sizes

Macro Capacity (megabits)	x 256 Configuration			x 292 Configuration		
	Macro X (μm)	Macro Y (μm)	Macro Area (mm^2)	Macro X (μm)	Macro Y (μm)	Macro Area (mm^2)
1	988.8	1900.8	1.88	988.8	2112.6	2.09
2	1291.2	1900.8	2.45	1291.2	2112.6	2.73
3	1622.4	1900.8	3.08	1622.4	2112.6	3.43
4	1924.8	1900.8	3.66	1924.8	2112.6	4.07
5	2256.0	1900.8	4.29	2256.0	2112.6	4.76
6	2558.4	1900.8	4.86	2558.4	2112.6	5.40
7	2889.6	1900.8	5.49	2889.6	2112.6	6.10
8	3192.0	1900.8	6.07	3192.0	2112.6	6.74
9	3523.2	1900.8	6.70	3523.2	2112.6	7.44
10	3825.6	1900.8	7.27	3825.6	2112.6	8.08
11	4156.8	1900.8	7.90	4156.8	2112.6	8.78
12	4502.4	1900.8	8.56	4502.4	2112.6	9.51
13	4833.6	1900.8	9.19	4833.6	2112.6	10.21
14	5136.0	1900.8	9.76	5136.0	2112.6	10.85
15	5467.2	1900.8	10.39	5467.2	2112.6	11.55
16	5769.6	1900.8	10.97	5769.6	2112.6	12.19

Naming Conventions

The naming strategy for the embedded DRAM macro is defined such that unique instance names can be created for each possible configuration. The first group of characters in the name defines the macro type. The fields that follow define the configuration options. Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

DRAMbbXwwwXcXdddVxxMz
where:

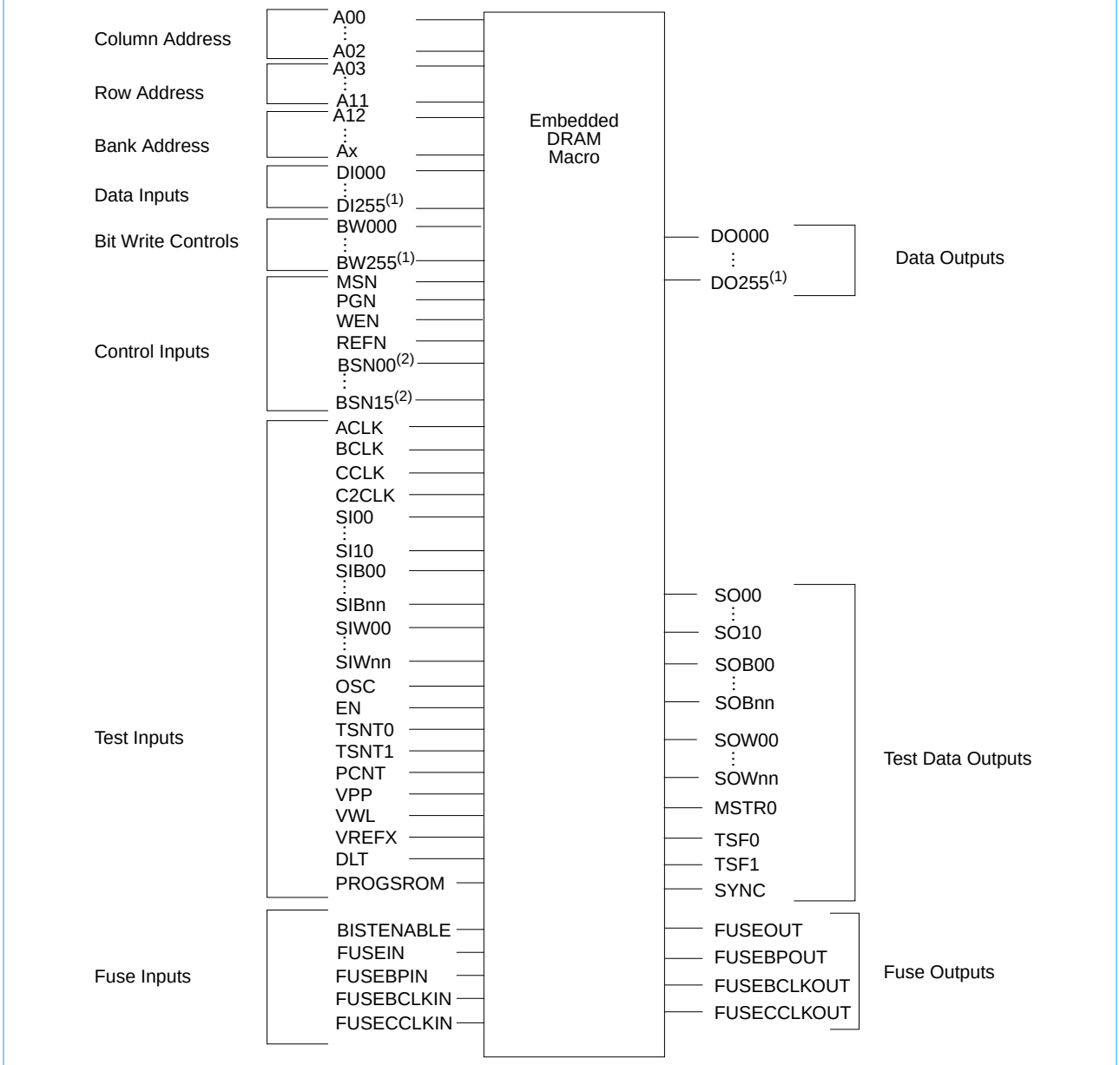
DRAM	=	DRAM macro
bb	=	total number of 1 Mb blocks: 2 digits
www	=	total number of word addresses: 3 digits (currently, only ‘512’ is available)
c	=	total number of column addresses: 1 digit (currently, only ‘8’ is available)
ddd	=	data width in bits: 3 digits
xx	=	operating voltage: 2 digits 12 = 1.2 V operation 15 = 1.5 V operation
z	=	functional mode: 1 digit 1 = single bank operation 2 = multi bank operation

A representative example is shown below:

DRAM01X512X8X256V15M1 A DRAM with 1 Mb density, 512 row addresses and 8 column addresses, 256 data bits wide, configured for 1.5 V operation, with a single bank interface.

Logical Description

Figure 1. x 256 or x 292 Configuration



Notes:

1. '291' for x 292 configuration.
2. BSN00–BSN15 only exist on multi-bank mode macros.

Pin Descriptions

Table 2. Embedded DRAM Pin Descriptions

Function	Signal	Count	Description	I/O
Control	MSN[1]	1	Macro select	I
	BSN0–BSN15[2]	1–16	Bank select	I
	PGN[1]	1	Page mode select	I
	WEN[1]	1	Write enable	I
	REFN[1]	1	Refresh enable	I
Address	A00–A02	3	Column address	I
	A03–A11	9	Row address	I
	A12–Ax[3]	0-4	Bank address/block address	I
Data (x 256 configuration)	DI000–DI255	256	Data inputs	I
	BW000–BW255[4]	256	Bit write inputs	I
	DO000–DO255	256	Data outputs	O
Data (x 292 configuration)	DI000–DI291	292	Data inputs	I
	BW000–BW291[4]	292	Bit write inputs	I
	DO000–DO291	292	Data outputs	O
Test	ACLK	1	LSSD A clock	I
	BCLK	1	LSSD B clock	I
	CCLK	1	LSSD C clock	I
	C2CLK	1	LSSD C clock	I
	SI00–SI10	11	Scan in	I
	SIB00–SIBnn[5]		Scan in	I
	SIW00–SIWnn[5]		Scan in	I
	SO00–SO10	11	Scan out	O
	S0B00–S0Bnn[5]		Scan out	O
	S0W00–S0Wnn[5]		Scan out	O
	OSC	1	Oscillator input	I
	EN	1	Oscillator enable	I
	TSTN0–TSTN1	2	Test mode enable	I

1. Input signals are negative active.
2. BSN inputs (0–15) only exist on multi-bank mode macros. All BSN inputs are negative active.
3. x depends on macro size and varies from 12–15.
4. High level enables write; low level disables write.
5. nn depends on macro size and is equal to: bb (in macro name) - 1.
6. Analog power-supply tester inputs.
7. All fuse pins are associated with the fuse decompression macro. Refer to the *FUSEDECOMPRESSION—Fuse Decompression Macro* datasheet in the *Cu-11 Databook: Macros*, or contact an IBM representative.

Table 2. Embedded DRAM Pin Descriptions (Continued)

Function	Signal	Count	Description	I/O
Test	MSTR0	1	MBIST result (real time)	O
	PCNT	1	Pause counter test input	I
	TSF0–TSF1	2	Test data save flag	O
	DLT	1	I_{DDQ} test input	I
	VPP[6]	1	Word line high bias	I
	VWL[6]	1	Word line low bias	I
	VREFX[6]	1	Reference cell bias	I
	SYNC	1	Diagnostic trigger	O
	PROGSROM	1	Scan-in pin for SROMReload	I
	FUSEIN[7]	1	Fuse shift-in port	I
	FUSEOUT[7]	1	Fuse shift-out port	O
	FUSEBCLKIN[7]	1	Fuse B clock in	I
	FUSEBCLKOUT[7]	1	Fuse B clock out	O
	FUSECCLKIN[7]	1	Fuse C clock in	I
	FUSECCLKOUT[7]	1	Fuse C clock out	O
	FUSEBPIN[7]	1	Fuse bypass in	I
	FUSEBPOUT[7]	1	Fuse bypass out	O
	BISTENABLE[7]	1	BIST enable from fuse decompression	I

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Banking Interfaces

The following paragraphs describe Cu-11's embedded DRAM macro single bank and multi bank configurations. For the multi bank mode configuration ('M2' parts), each 1-Mb block of the macro acts as an independent bank that shares a common data bus with all other 1-Mb blocks within the macro. A 1-Mb block consist of 512 wordlines by 2048 bitlines (by 2336 bitlines for x 292 configurations). The number of banks within a macro is determined by the macro size. A bank select pin (BSN) is associated with each 1-Mb block, and is used in conjunction with other command input signals (MSN, PGN, address, WEN) to determine which bank(s) within the macro respond to input commands. See *Table 4* and *Table 5* on page 9.

For the single bank mode configuration ('M1' parts), the operating mode is nearly identical to IBM's SA-27E embedded DRAM macro operation, with the following exceptions:

1. All bank select inputs (which did not exist on the SA-27E embedded DRAM macro) must be tied dc high or low.

2. The PGN input must be low prior to MSN falling to initiate random read or write cycles.

   Note: This second condition is a functional change from single bank operation of the SA-27E embedded DRAM macro. The SA-27E macro specified PGN ‘high’ prior to MSN falling to initiate random access cycles.

Broadside addressing is supported for single bank mode configurations, where:

- A0–A2 decodes 1-of-8 page (or column) addresses
- A3–A11 decodes 1-of-512 row addresses within a 1-Mb block
- A12–A15 decodes which 1-Mb block is to be accessed

The number of high order addresses (A12–A15) is determined by the macro size. The diagram in *Figure 2* on page 13 shows an example timing for a macro in single bank mode operation. Note that for page read or write cycles, only column address bits (A0–A2) need to be supplied with each successive page cycle. The row and block addresses remain latched until MSN is returned high.

In multi bank configuration, the macro does not employ broadside addressing. Rather, the embedded DRAM macro operates similar to a synchronous DRAM (SDRAM) where addressing is performed in a RAS/CAS type manner and the macro select input (MSN) is treated like a master input clock, latching the state of all other input pins with each falling MSN edge. See *Figure 8* on page 19. The MSN input can be cycled at a maximum rate of 200 MHz (5 ns assuming a nominal 50/50 clock duty cycle). All bank select inputs (BSN) must be defined at every MSN falling edge to indicate whether each bank is to remain open or closed or whether a bank is to become active/open (from the precharge state) or become precharged/closed (from the active state).

Any combination of banks within a macro can be active simultaneously as long as each 1-Mb bank is opened in a sequential fashion. Multiple banks cannot be activated or precharged on a single MSN clock cycle.

To activate a bank, the corresponding bank select signal (BSN) must be low and the row address for that bank must be supplied on address pins A3–A11 when MSN is clocked low. The row address for each active bank remains latched until the bank is precharged. This frees the row address bus to allow other banks to be activated at a different row address on subsequent MSN clock cycles. A bank is precharged by placing a high level on the corresponding BSN input when the MSN is clocked low. No address information is required to precharge a bank.

Once a bank has been activated, a read or write operation can be performed to that bank by bringing PGN low, selecting the state of the WEN pin (read = high, write = low), specifying the column address on A0–A2, and specifying the bank address on A12–A15 as MSN is clocked low. *Note that PGN must be low when MSN is clocked low to initiate a read or write operation, in contrast with the SA-27E embedded DRAM functional operation.*

Multiple operations to three banks can occur on each MSN cycle. For example, a first bank can be activated, a second bank can be accessed for a read or write operation, and a third bank can be precharged. Combinations of commands cannot occur on the same bank on any single clock cycle (for example, bank activate, read, write or precharge).

A multi bank timing example is shown in *Figure 8* on page 19. Note that the assumed macro size in this example is 4 Mb, and consequently, only four bank select inputs (BSN[0:3]) and two bank addresses (A12–A13) are required to address this macro.

A refresh operation is executed differently in single bank configuration versus multi bank configuration, but the minimum refresh cycle time is the same for both configurations. In either configuration, all banks must be closed and fully precharged prior to a refresh command.

In the single bank configuration, a refresh cycle is initiated by holding REFN low and WEN high when MSN is strobed low (PGN= don't care). MSN must remain low for the minimum bank activation time (T_{act}) and must return high and remain high for the minimum restore time (T_{res}) before a subsequent refresh cycle (or any new command) can be issued to the macro. Because the refresh addresses are determined by counter circuitry internal to the macro, the external address inputs to the macro are treated as "don't care" inputs. Back-to-back refresh cycles can be issued to the macro at a 66 MHz rate (15 ns). See *Figure 7* on page 18.

In the multi bank configuration, the refresh operation is handled differently because the macro is clocked in a synchronous manner by the MSN input. Here, a refresh cycle is a combination of three MSN clock cycles. A refresh cycle is initiated on the first MSN falling edge by holding REFN low, all BSN pins high, WEN high, and PGN high when MSN is clocked low at the start of the first cycle. To continue the refresh operation, REFN must be held low on the second (next) MSN falling edge with no other input changing state. Finally the refresh operation is completed by holding REFN high during the third (next) falling edge with no other input allowed to change state. Essentially, a refresh operation can be issued to the macro every fourth clock cycle. However, once a refresh operation is initiated, no other operation is permitted on the next two falling edges of MSN. For 1.5 V operation, the maximum MSN clock rate is 250 MHz (4 ns), which corresponds to a maximum refresh rate of 83 MHz (3 clocks x 4 ns). For 1.2 V operation, the maximum MSN clock rate is 200 MHz (5 ns), which which corresponds to a maximum refresh rate of 66 MHz (3 clocks x 5 ns). See *Figure 10* on page 21.

Truth Tables

Table 3. Bank Decode

Bank	BSN	A15	A14	A13	A12
Bank 0	BSN0	0	0	0	0
Bank 1	BSN1	0	0	0	1
Bank 2	BSN2	0	0	1	0
Bank 3	BSN3	0	0	1	1
Bank 4	BSN4	0	1	0	0
Bank 5	BSN5	0	1	0	1
Bank 6	BSN6	0	1	1	0
Bank 7	BSN7	0	1	1	1
Bank 8	BSN8	1	0	0	0
Bank 9	BSN9	1	0	0	1
Bank 10	BSN10	1	0	1	0
Bank 11	BSN11	1	0	1	1
Bank 12	BSN12	1	1	0	0
Bank13	BSN13	1	1	0	1
Bank 14	BSN14	1	1	1	0
Bank 15	BSN15	1	1	1	1

1. Address inputs A12-A15 and the number of bank select inputs (BSN[0:15]) are a function of macro density.

Table 4. Single-Bank Interface Embedded DRAM Truth Table

Operation	MSN	BSNx	PGN	WEN	REFN	Ax	DI	DO	BW
Random read	0	L/H	0	1	1	Row Column Bank	-	DOUT	-
Random write	0	L/H	0	0	1	Row Column Bank	L/H	L-R	L/H
Page read	0	L/H	0	1	1	Column	-	DOUT	-
Page write	0	L/H	0	0	1	Column	L/H	L-R	L/H
Refresh	0	L/H	L/H	1	0	-	-	L-R	-

1. “-” = Valid binary state; don't care if L or H
2. L/H = L or H depending on cycle
3. L-R = Last read data

Table 5. Multi-Bank Interface Embedded DRAM Truth Table

Operation	MSN	BSNx	PGN	WEN	REFN	Ax	DI	DO	BW
Bank activate	H -> L[1]	0	1[2]	L/H	1	Row	-	L-R	-
Bank precharge	H -> L[1]	1	1[2]	L/H	1	-	-	L-R	-
Bank read	H -> L[1]	0	0	1	1	Bank Column	-	DOUT	-
Bank write	H -> L[1]	0	0	0	1	Bank Column	L/H	L-R	L/H
Refresh	H -> L[1]	1	1	1	0	-	-	L-R	-
NOP	H -> L[1]	Previous State	1	L/H	1	-	-	L-R	-

1. H -> L = commands are initiated on the falling edge of the MSN clock input.
2. PGN can be low during bank activate or bank precharge cycles, depending on what command is used to other open banks when a bank activate or bank precharge operation command is used.
3. “-” = Valid binary state; don't care if L or H.
4. L/H = L or H depending on cycle.
5. L-R = Last read data.

Electrical Characteristics

Table 6. Power Supply Currents (1.5 V operation, 12.0 ns T_{cyc}, 4.0 ns T_{pcyc}, 4.0 ns T_{bcyc})

Condition		x 256 Configuration		x 292 Configuration	
		Active Current[1]	Standby Current[2]	Active Current[1]	Standby Current[2]
Single-Bank Random Cycle	No data changing	56.9 mA	Contact an IBM ASIC representative for standby current estimates	64.4 mA	Contact an IBM ASIC representative for standby current estimates
	All data changing continuous write	56.9 mA + 3.94 mA per Mb		64.4 mA + 4.50 mA per Mb	
	All data changing continuous read	56.9 mA + 2.63 mA per Mb		64.4 mA + 3.0 mA per Mb	
Single-Bank Page Cycle	No data changing	1.88 mA		2.13 mA	
	All data changing continuous write	1.88 mA + 11.25 mA per Mb		2.13 mA + 12.80 mA per Mb	
	All data changing continuous read	1.88 mA +7.40 mA per Mb		2.13 mA + 8.40 mA per Mb	
Multi-Bank Cycle	No data changing	170.6 mA		193.10 mA	
	All data changing continuous write	170.6 mA +11.80 mA per Mb		193.10 mA + 13.50 mA per Mb	
	All data changing continuous read	170.6 mA +7.90 mA per Mb		193.10 mA + 9.0 mA per Mb	

1. For multi-bank cycles, three operations per cycle are assumed.
2. For multi-bank operating mode, the standby current increases 0.500 mA for each address input that is switched, and 0.025 mA for each data input or bit-write input that is switched. These current adders are specified at the maximum MSN clock frequency and should be de-rated as the clock frequency decreases. IBM recommends holding these macro inputs at a dc stable level (high or low) in standby mode.

The data shown in *Table 6* can be modified for voltages other than 1.5 V, single-bank cycles other than 12 ns, page cycles other than 4.0 ns, multi-bank cycles other than 4.0 ns, and less than three operations per cycle in multi-bank mode by applying the factors shown in *Table 7*.

Table 7. Adjustment Factors

Multiplication Factor	Description
I (V/1.5 V) * I	For voltages other than 1.5 V
I (12.0 ns/T_{cyc}) * I	For single bank MSN cycles other than 12.0 ns
I (4.0 ns/T_{pcyc}) * I	For PGN page cycles other than 4.0 ns
I (4.0 ns/T_{bcyc}) * I	For BSN multi-bank cycles other than 4.0 ns
I (AOPC/3) * I	For less than three average operations per cycle (AOPC) in multi-banking mode

Table 8. 1.2 V ac Parameters[1, 2]

Symbol	Parameter	x 256 Configuration		x 292 Configuration		Units
		Min	Max	Min	Max	
T_{set}	Input setup to MSN/PGN[3]	1	—	1	—	ns
T_{hld}	Input hold to MSN/PGN[3]	2	—	2	—	ns
T_{acc}	Random access time	4.0	11.0	4.0	11.0	ns
T_{act}	MSN active time	11.0	100k	11.0	100k	ns
T_{res}	MSN restore time	5.5	—	5.5	—	ns
T_{cyc}	Random R/W cycle time	16.5	—	16.5	—	ns
T_{rfc}	Refresh cycle time	16.5	—	16.5	—	ns
T_{accp}	Page mode access time	1.2	5.25	1.2	5.25	ns
T_{pa}	PGN active time	2.2	—	2.2	—	ns
T_{pr}	PGN restore time	2.2	—	2.2	—	ns
T_{pcyc}	PGN cycle time[4]	5.5	—	5.5	—	ns
T_{setp}	PGN to MSN setup[5]	0		0		ns
T_{mprd}	MSN to PGN restore delay[4]	8.25	—	8.25	—	ns
T_{actp}	MSN active for page mode[6]	16.5	—	16.5	—	ns
T_{ref}	Refresh period[7]	—	3.2	—	3.2	ms
T_{pamr}	Page active to MSN restore	5.5	—	5.5	—	ns
T_{bcyc}	Bank mode MSN cycle time	5.5	—	5.5	—	ns
T_{bacc}	Bank mode MSN access time	1.2	5.25	1.2	5.25	ns
T_{ma}	Bank mode MSN low time	2.2	—	2.2	—	ns
T_{mr}	Bank mode MSN high time	2.2	—	2.2	—	ns
T_{rrd}	Bank mode MSN activate to activate delay	T_{bcyc}	—	T_{bcyc}	—	ns
T_{rcd}	Bank mode MSN activate to read/write delay	T_{bcyc}	—	T_{bcyc}	—	ns
T_{crp}	Bank mode MSN read/write to precharge delay	T_{bcyc}	—	T_{bcyc}	—	ns

1. Propagation delay and setup/hold timing calculations throughout this databook are representative numbers at beginning-of-life. Refer to *End-of-Life Considerations* in the *Cu-11 Databook: Macros*, or contact an IBM representative for more information. Data shown is for reference only: refer to the timing models (NDRs) for application-specific supported timings.
2. 1.2 V ac parameters are applicable for T_j ranging from 0°C to 105°C.
3. All input set up and hold times are specified with respect to either MSN (random cycle) or PGN (page cycle).
4. The PGN cycle time and MSN and PGN delay must be chosen to allow a sufficient data output window.
5. For single-bank M1 operation only.
6. The T_{actp} parameter depends on the number of page cycles (T_{pcyc}) performed during MSN active time.
7. *W* refresh cycles must be issued within 3.2 ms, where *W* is the total number of word addresses in the macro. Distributed refresh, burst refresh, or a combination of distributed and burst refresh are allowed, provided that all word addresses are refreshed within the specified refresh period.
8. Signal rise and fall times to the macro are assumed to be ≤ 0.2 ns.

Table 9. 1.5 V ac Parameters[1, 2]

Symbol	Parameter	x 256 Configuration		x 292 Configuration		Units
		Min	Max	Min	Max	
T_{set}	Input setup to MSN/PGN[3]	1	—	1	—	ns
T_{hld}	Input hold to MSN/PGN[3]	2	—	2	—	ns
T_{acc}	Random access time	3.0	8.0	3.0	8.0	ns
T_{act}	MSN active time	8.0	100k	8.0	100k	ns
T_{res}	MSN restore time	4.0	—	4.0	—	ns
T_{cyc}	Random R/W cycle time	12	—	12	—	ns
T_{rfc}	Refresh cycle time	12	—	12	—	ns
T_{accp}	Page mode access time	1.0	3.9	1.0	3.9	ns
T_{pa}	PGN active time	1.6	—	1.6	—	ns
T_{pr}	PGN restore time	1.6	—	1.6	—	ns
T_{pcyc}	PGN cycle time[4]	—	—	—	—	—
T_{setp}	PGN to MSN setup[5]	0		0		ns
T_{mprd}	MSN to PGN restore delay[4]	6	—	6	—	ns
T_{actp}	MSN active for page mode[6]	12	—	12	—	ns
T_{ref}	Refresh period[7]	—	3.2	—	3.2	ms
T_{pamr}	Page active to MSN restore	4	—	4	—	ns
T_{bcyc}	Bank mode MSN cycle time	4	—	4	—	ns
T_{bacc}	Bank mode MSN access time	1.0	3.9	1.0	3.9	ns
T_{ma}	Bank mode MSN low time	1.6	—	1.6	—	ns
T_{mr}	Bank mode MSN high time	1.6	—	1.6	—	ns
T_{rrd}	Bank mode MSN activate to activate delay	T_{bcyc}	—	T_{bcyc}	—	ns
T_{rcd}	Bank mode MSN activate to read/write delay	T_{bcyc}	—	T_{bcyc}	—	ns
T_{crp}	Bank mode MSN read/write to precharge delay	T_{bcyc}	—	T_{bcyc}	—	ns

1. Propagation delay and setup/hold timing calculations throughout this databook are representative numbers at beginning-of-life. Refer to *End-of-Life Considerations* in the *Cu-11 Macros* databook or contact an IBM representative for more information. Data shown is for reference only: refer to the timing models (NDRs) for application-specific supported timings.
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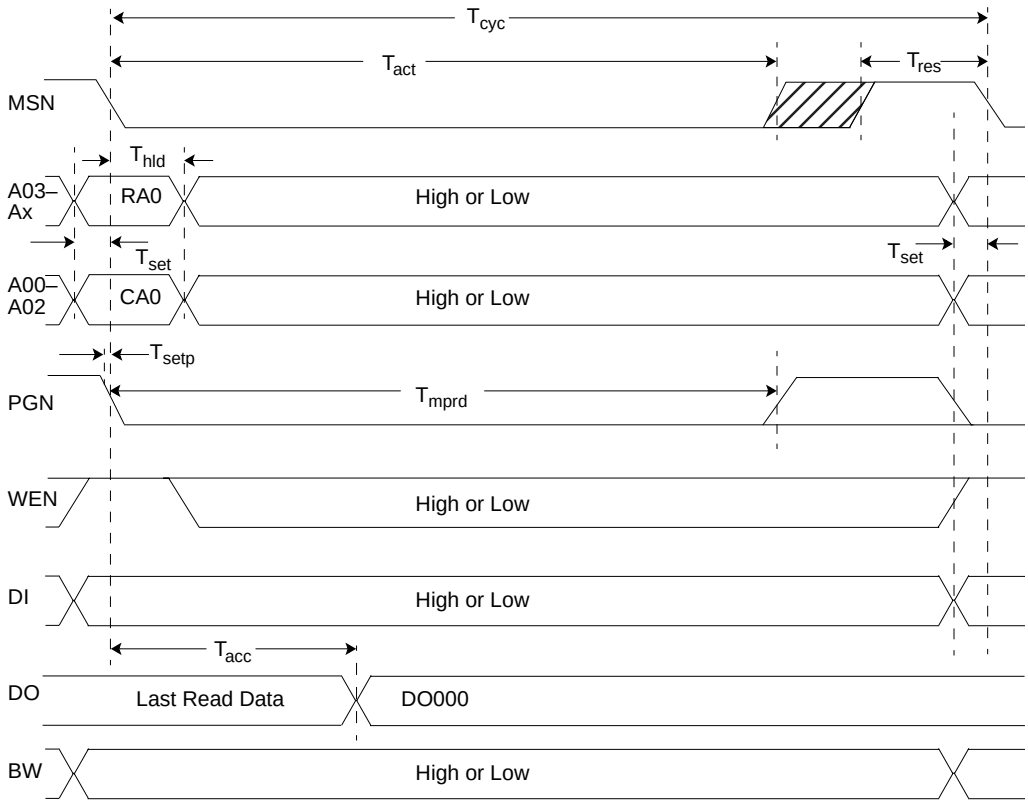
3. All input set up and hold times are specified with respect to either MSN (random cycle) or PGN (page cycle).
4. The PGN cycle time and MSN and PGN delay must be chosen to allow a sufficient data output window.
5. For single-bank M1 operation only.
6. The T_{actp} parameter depends on the number of page cycles (T_{pcyc}) performed during MSN active time.
7. *W* refresh cycles must be issued within 3.2 ms, where *W* is the total number of word addresses in the macro. Distributed refresh, burst refresh, or a combination of distributed and burst refresh are allowed, provided that all word addresses are refreshed within the specified refresh period.
8. Signal rise and fall times to the macro are assumed to be ≤ 0.2 ns.

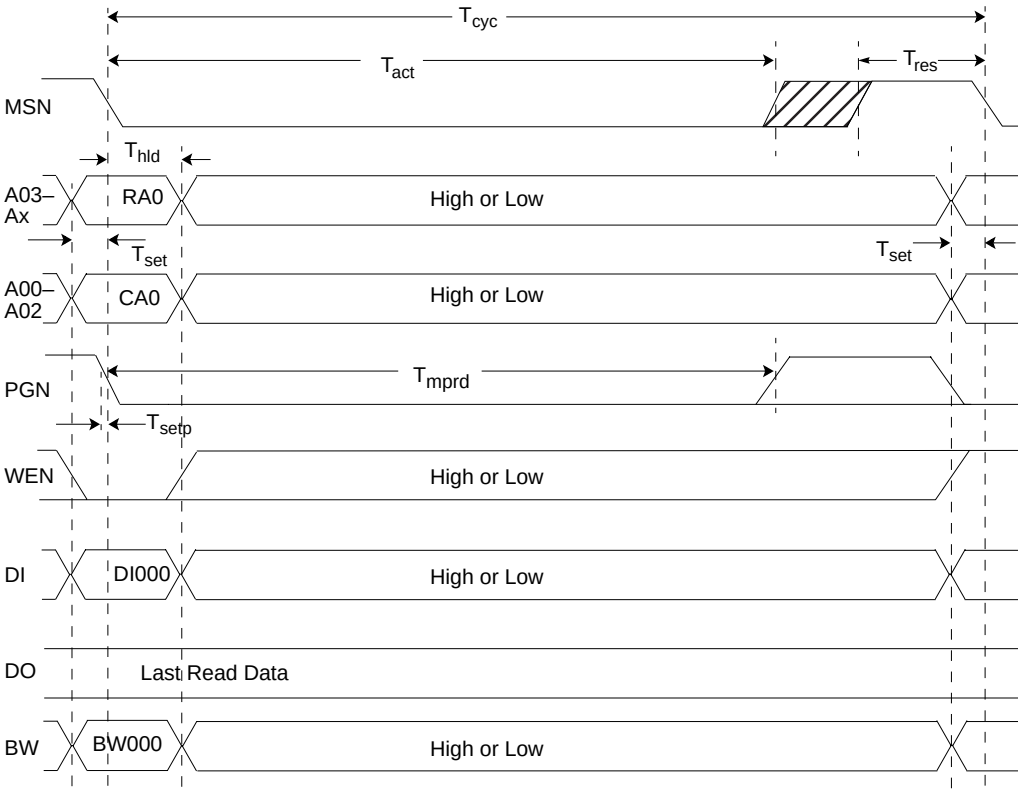
Timing Diagrams

Figure 2. Random Read Cycle (Single-Bank Configuration)



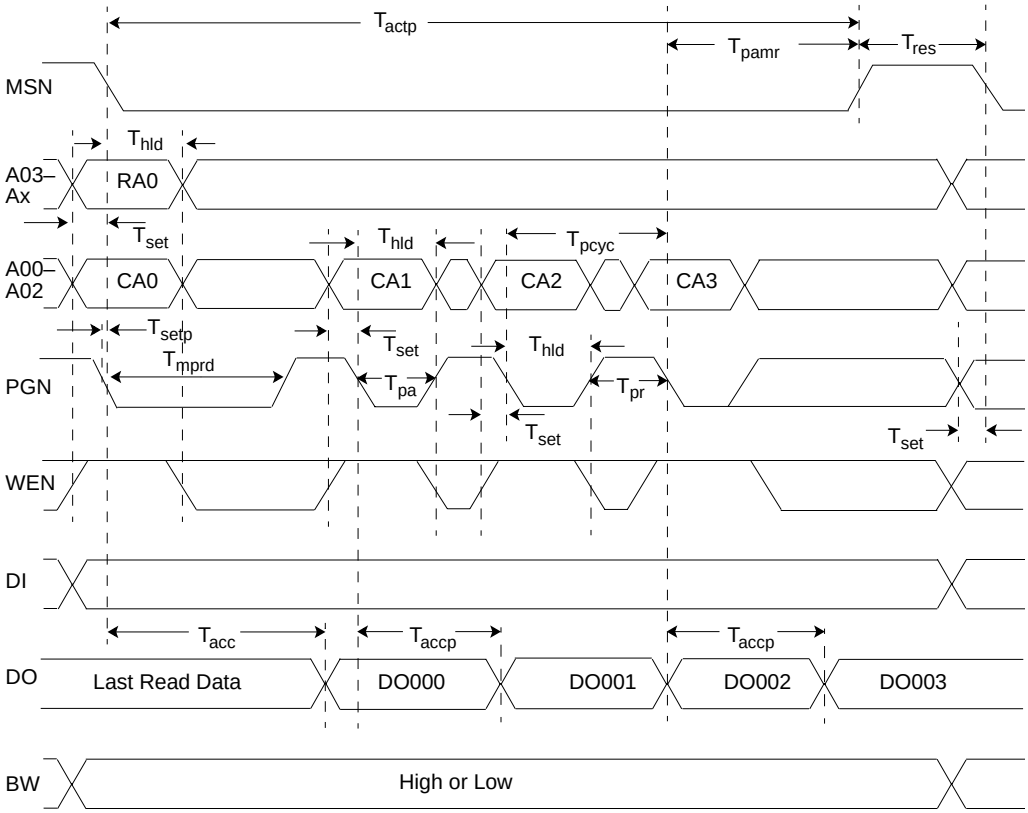
1. All inputs should stay at valid signal levels and not switch unnecessarily.
2. REFN high during all cycles except refresh.

Figure 3. Random Write Cycle (Single-Bank Configuration)



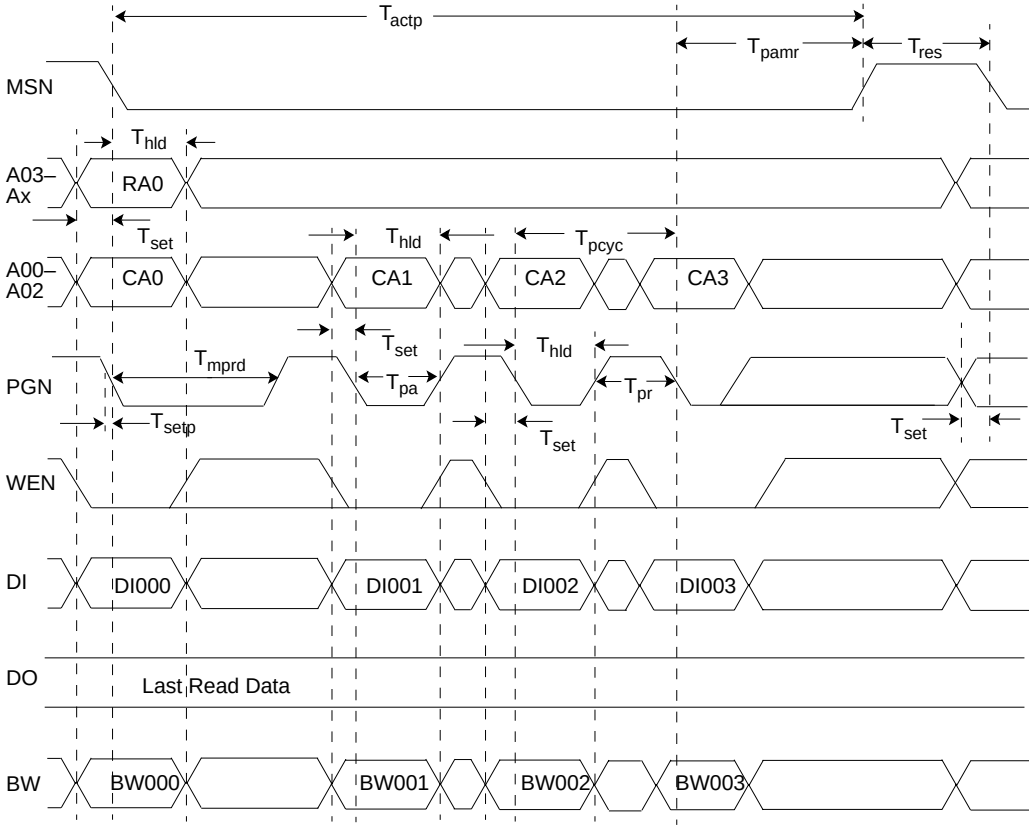
1. All inputs should stay at valid signal levels and not switch unnecessarily.
2. REFN high during all cycles except refresh.

Figure 4. Page-Mode Read Cycle (Single-Bank Configuration)



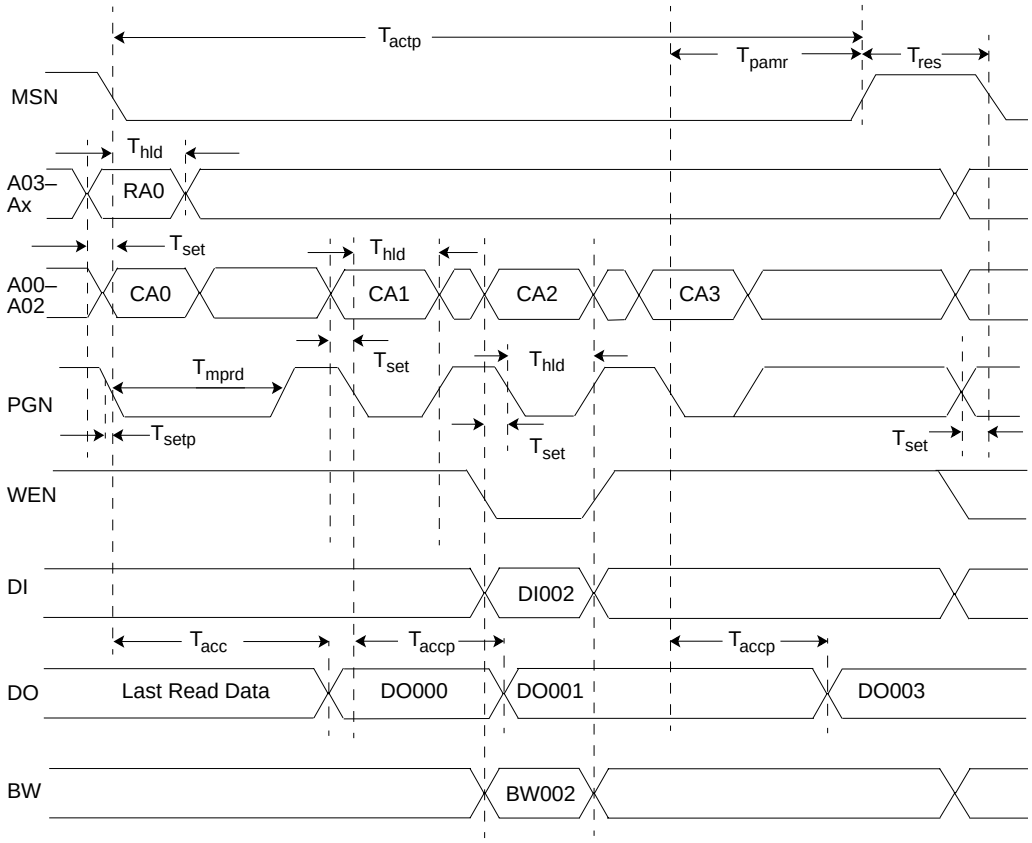
1. All inputs should stay at valid signal levels and not switch unnecessarily.
2. REFN high during all cycles except refresh.

Figure 5. Page-Mode Write Cycle (Single-Bank Configuration)



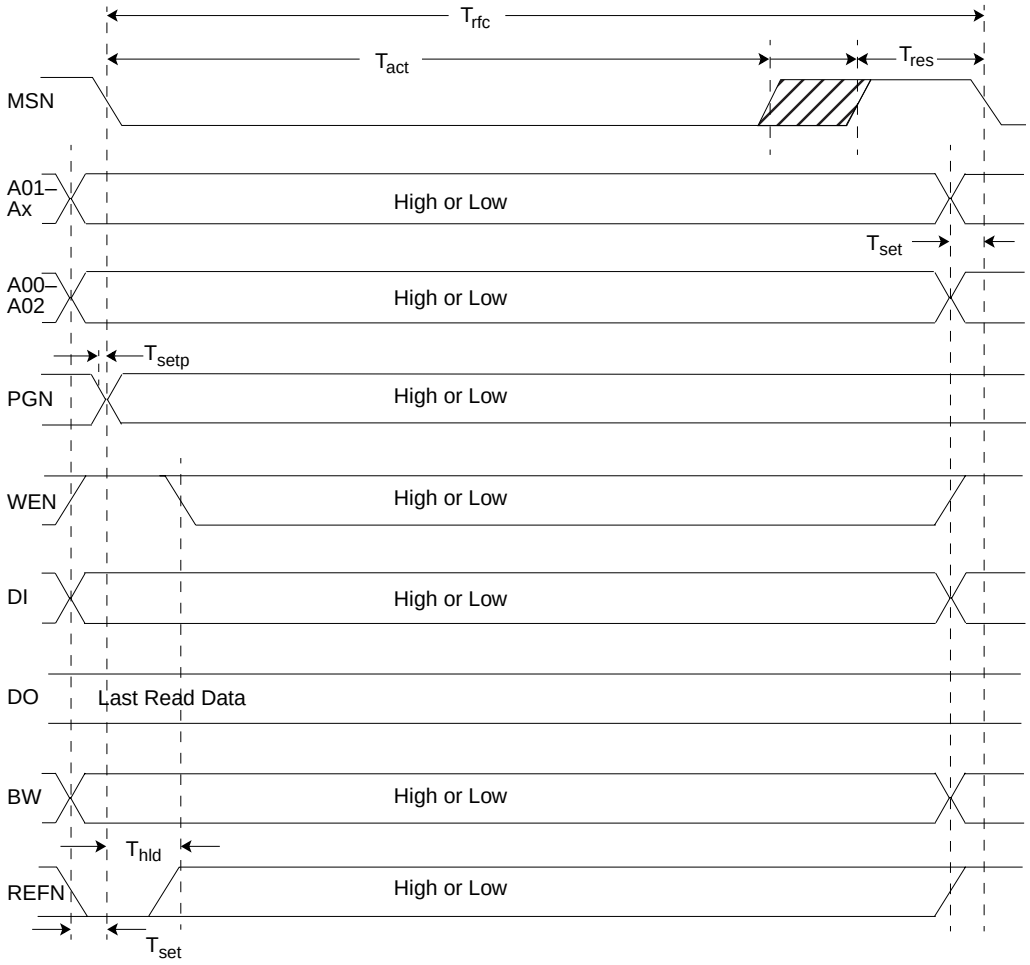
1. All inputs should stay at valid signal levels and not switch unnecessarily.
2. REFN high during all cycles except refresh.

Figure 6. Page-Mode Read-Write-Read Cycle (Single-Bank Configuration)



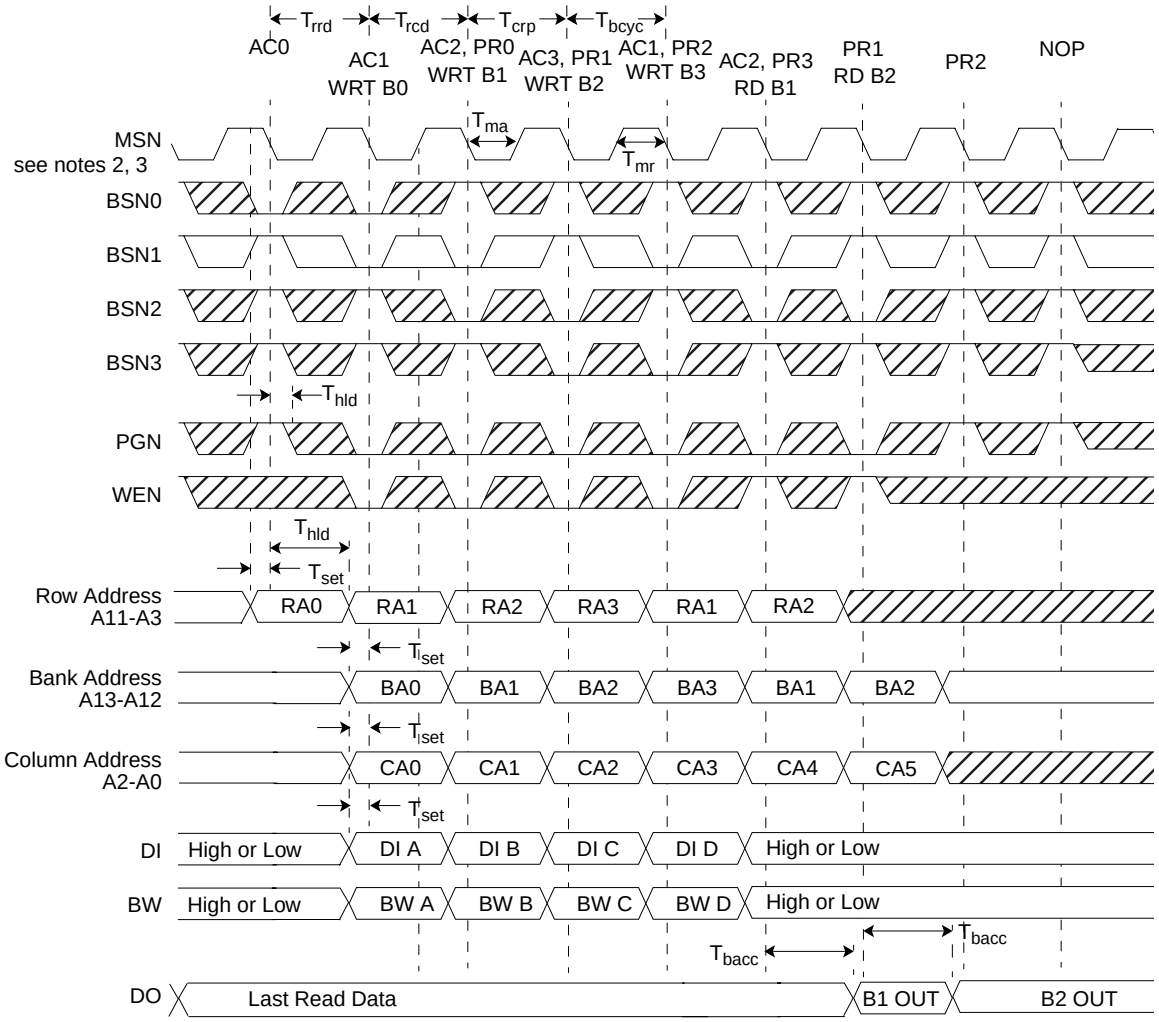
1. All inputs should stay at valid signal levels and not switch unnecessarily.
2. REFN high during all cycles except refresh.

Figure 7. Refresh Cycle (Single-Bank Configuration)



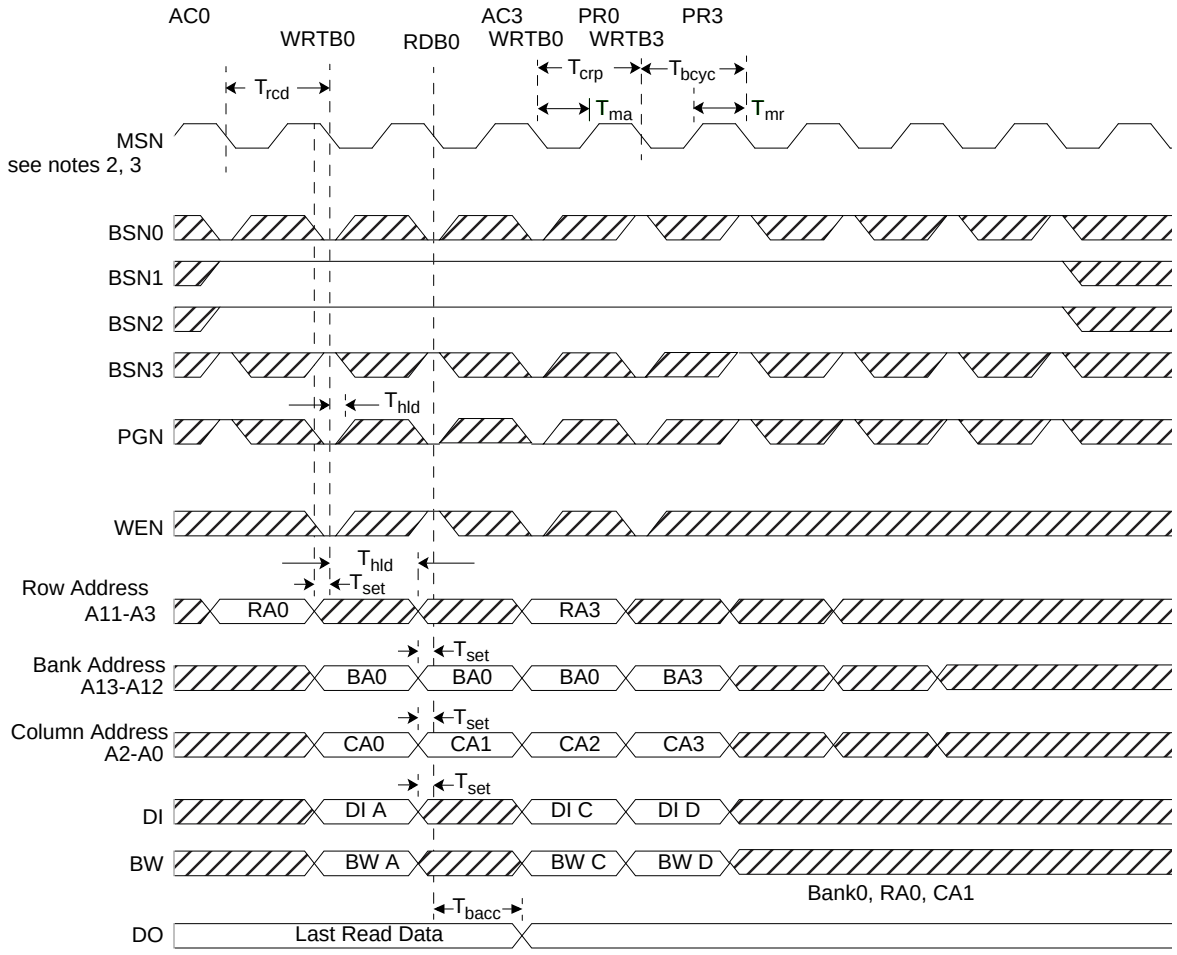
1. All inputs should stay at valid signal levels and not switch unnecessarily.

Figure 8. Multi-Bank Configuration



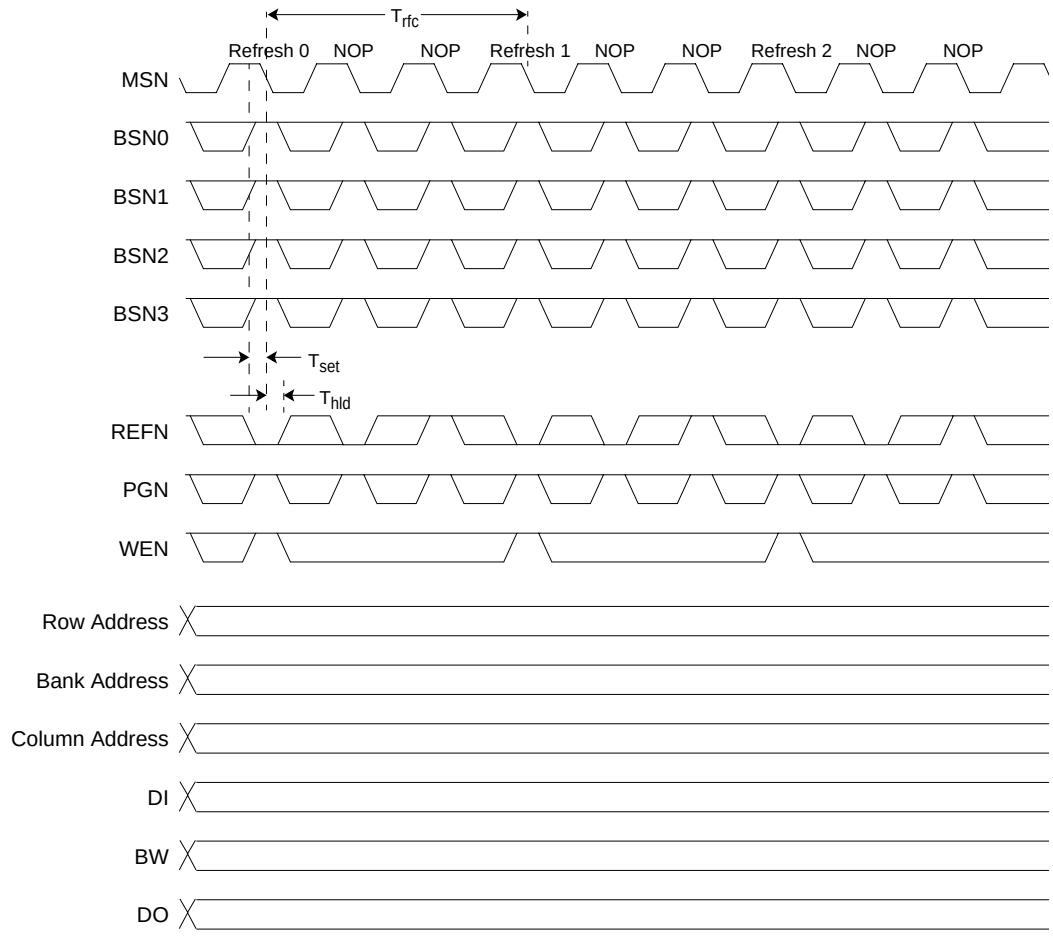
1. Synchronous multi bank timing for a 4 Mb macro.
2. ACx = activate bank x; PRx = precharge bank x.
3. WRT Bx = write bank x; RD Bx = read bank x.
4. BSN[0:3] only, A13-A12 only.
5. Does not support broadside addressing.
6. NOP = no activates, precharges, writes, reads, or refreshes on that cycle.

Figure 9. Multi-Bank Configuration with Page-Mode Access



1. Synchronous multi bank timing for a 4 Mb macro.
2. ACx = activate bank x; PRx = precharge bank x.
3. WRT Bx = write bank x; RD Bx = read bank x.
4. BSN[0:3] only, A13-A12 only.
5. Does not support broadside addressing.
6. NOP = no activates, precharges, writes, reads, or refreshes on that cycle.

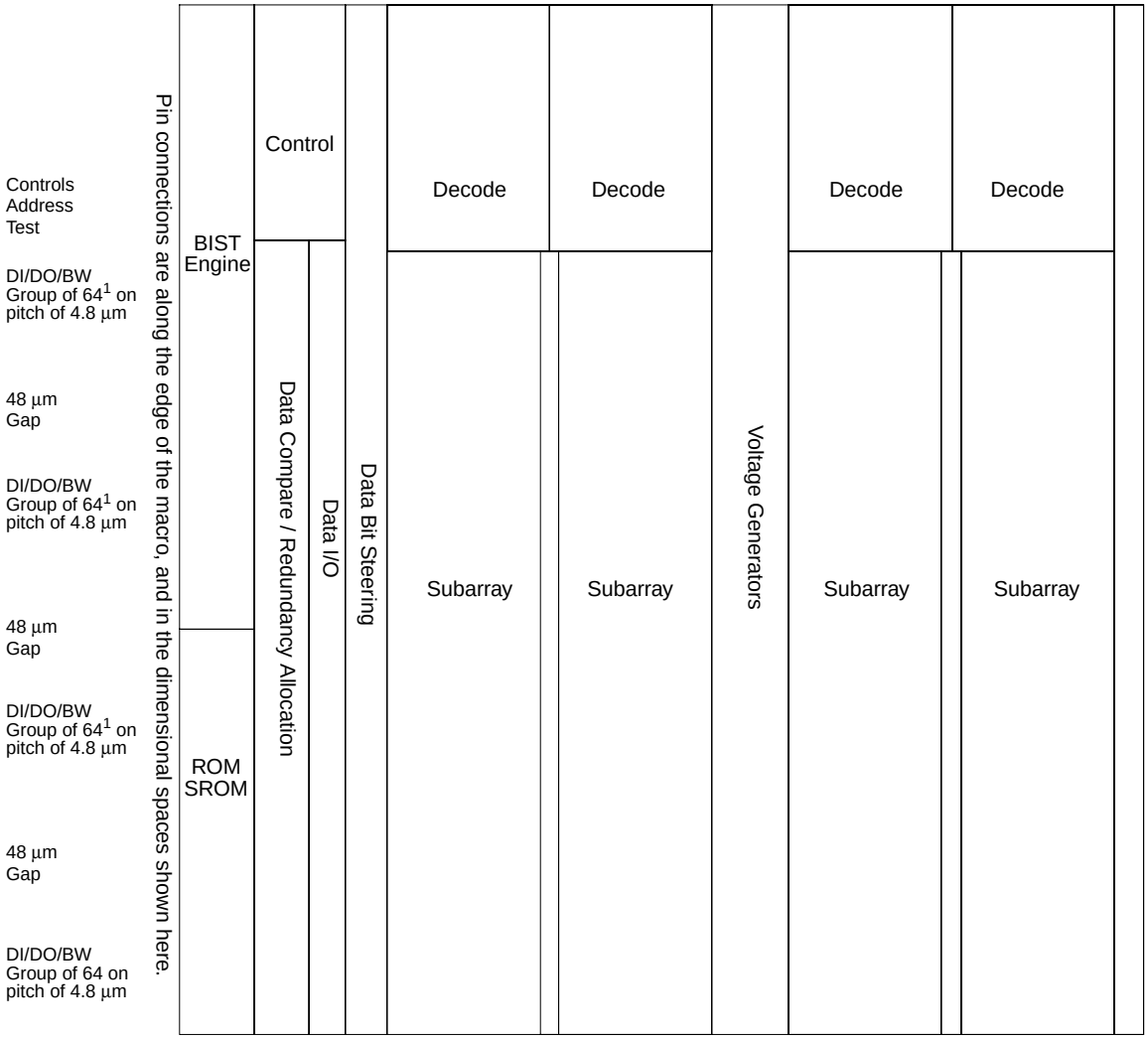
Figure 10. Multi-Bank Configuration Refresh Cycle (Three Back-to-Back Refresh Operations)



1. Synchronous multi bank timing for a 4 Mb macro.
2. BSN[0:3] only.
3. NOP = no activates, precharges, writes, reads, or refreshes on that cycle.

Macro Orientation

Figure 11. x 256 DRAM Macro Orientation



1. The x 292 configuration is in groups of 73 on a pitch of 4.8 µm.

Revision Log

Date	Page	Description
March 25, 2003	10	Corrected embedded DRAM x292 standby currents.
February 13, 2003	2, 11–12, 15–18, 19	Added *Related Documentation* and T_{setp} timing. Updated *Multi-Bank Configuration* figure.
December 12, 2002	1, 10–12	Miscellaneous updates.
August 30, 2002	1	Updated embedded DRAM interleave operation timing.
June 25, 2002	1, 10–12, 20	Added additional references to junction temperature and *Multi-Bank Configuration with Page-Mode Access* timing diagram.
March 21, 2002	—	Updated to reflect Cu-11 design kit v9.0 and FSG manufacturing process performance data, and other miscellaneous updates.
January 18, 2002	10	Updated electrical characteristics

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