BURR - BROWN®

DAC7634

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16-Bit, Quad Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 10mW
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10μs to 0.003%
- 15-BIT LINEARITY AND MONOTONICITY: –40°C to +85°C
- PROGRAMMABLE RESET TO MID-SCALE OR ZERO-SCALE
- DOUBLE-BUFFERED DATA INPUTS

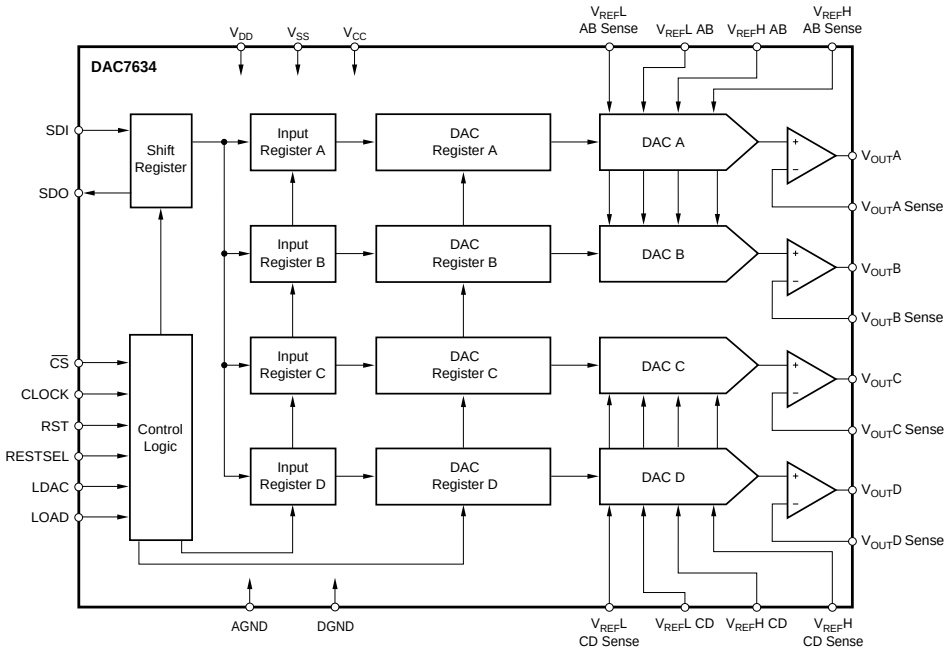
APPLICATIONS

- PROCESS CONTROL
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS
- DAC-PER-PIN PROGRAMMERS

DESCRIPTION

The DAC7634 is a 16-bit, quad voltage output, digital-to-analog converter with guaranteed 15-bit monotonic performance over the specified temperature range. It accepts 24-bit serial input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a serial data output for daisy chaining multiple DACs. Programmable asynchronous reset clears all registers to a mid-scale code of 8000_H or to a zero-scale of 0000_H. The DAC7634 can operate from a single +5V supply or from +5V and –5V supplies.

Low power and small size per DAC make the DAC7634 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7634 is available in a 48-lead SSOP package and offers guaranteed specifications over the –40°C to +85°C temperature range.



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SPECIFICATIONS

At $T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $V_{REF}H = +2.5V$, and $V_{REF}L = -2.5V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7634E			DAC7634EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error			±3	±4		±2	±3	LSB
Linearity Match			±4			±2		LSB
Differential Linearity Error			±2	±3		±1	±2	LSB
Montonicity, T_{MIN} to T_{MIN}		14			15			Bits
Bipolar Zero Error			±1	±2		*	*	mV
Bipolar Zero Error Drift			5	10		*	*	ppm/°C
Full-Scale Error			±1	±2		*	*	mV
Full-Scale Error Drift			5	10		*	*	ppm/°C
Bipolar Zero Matching	Channel-to-Channel Matching		±1	±2		±1	±2	mV
Full Scale Matching	Channel-to-Channel Matching		±1	±2		±1	±2	mV
Power Supply Rejection Ratio (PSRR)	At Full Scale		10	100		*	*	ppm/V
ANALOG OUTPUT								
Voltage Output	$V_{REF} = -2.5V$, $R_L = 10k\Omega$, $V_{SS} = -5V$	$V_{REF}L$		$V_{REF}H$	*		*	V
Output Current		–1.25		+1.25	*		*	mA
Maximum Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			–10, +30			*		mA
Short-Circuit Duration	GND or V_{CC} or V_{SS}		Indefinite			*		
REFERENCE INPUT								
Ref High Input Voltage Range		$V_{REF}L + 1.25$		+2.5	*		*	V
Ref Low Input Voltage Range		–2.5		$V_{REF}H - 1.25$	*		*	V
Ref High Input Current			500			*		µA
Ref Low Input Current			–500			*		µA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.003%, 5V Output Step		8	10		*	*	µs
Channel-to-Channel Crosstalk	See Figure 5.		0.5			*		LSB
Digital Feedthrough			2			*		nV-s
Output Noise Voltage	f = 10kHz		60			*		$nV/\sqrt{Hz}$
DAC Glitch	$7FFF_H$ to 8000_H or 8000_H to $7FFF_H$		40			*		nV-s
DIGITAL INPUT								
V_{IH}		$0.7 \cdot V_{DD}$			*			V
V_{IL}				$0.3 \cdot V_{DD}$			*	V
I_{IH}				±10			*	µA
I_{IL}				±10			*	µA
DIGITAL OUTPUT								
V_{OH}	$I_{OH} = -0.8mA$	3.6	4.5		*	*		V
V_{OL}	$I_{OL} = 1.6mA$		0.3	0.4		*	*	V
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	*	*	*	V
V_{CC}		+4.75	+5.0	+5.25	*	*	*	V
V_{SS}		–5.25	–5.0	–4.75	*	*	*	V
I_{CC}			1.5	2		*	*	mA
I_{DD}			50			*		µA
I_{SS}		–2.3	–1.5		*	*		mA
Power			15	20		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Specifications same as DAC7634E.

SPECIFICATIONS

At $T_A = T_{MIN}$ to T_{MAX}, $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REF}H = +2.5V$, and $V_{REF}L = 0V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7634E			DAC7634EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error(1)			±3	±4		±2	±3	LSB
Linearity Match			±4			±2		LSB
Differential Linearity Error			±2	±3		±1	±2	LSB
Montonicity, T_{MIN} to T_{MAX}		14			15			Bits
Zero Scale Error			±1	±2		✻	✻	mV
Zero Scale Error Drift			5	10		✻	✻	ppm/°C
Full-Scale Error			±1	±2		✻	✻	mV
Full-Scale Error Drift			5	10		✻	✻	ppm/°C
Zero Scale Matching	Channel-to-Channel Matching		±1	±2		±1	±2	mV
Full-Scale Matching	Channel-to-Channel Matching		±1	±2		±1	±2	mV
Power Supply Rejection Ratio (PSRR)	At Full Scale		10	100		✻	✻	ppm/V
ANALOG OUTPUT								
Voltage Output	$V_{REF}L = 0V$, $V_{SS} = 0V$, $R_L = 10k\Omega$	0		$V_{REF}H$	✻		✻	V
Output Current		–1.25		+1.25	✻		✻	mA
Maximum Load Capacitance	No Oscillation		500			✻		pF
Short-Circuit Current			±30			✻		mA
Short-Circuit Duration	GND or V_{CC}		Indefinite			✻		
REFERENCE INPUT								
Ref High Input Voltage Range		$V_{REF}L + 1.25$		+2.5	✻		✻	V
Ref Low Input Voltage Range		0		$V_{REF}H - 1.25$	✻		✻	V
Ref High Input Current			250			✻		µA
Ref Low Input Current			–250			✻		µA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.003%, 2.5V Output Step		8	10		✻	✻	µs
Channel-to-Channel Crosstalk	See Figure 6.		0.5			✻		LSB
Digital Feedthrough			2			✻		nV-s
Output Noise Voltage, f = 10kHz			60			✻		nV/√Hz
DAC Glitch	$7FFF_H$ to 8000_H or 8000_H to $7FFF_H$		40			✻		nV-s
DIGITAL INPUT								
V_{IH}		0.7 • V_{DD}			✻			V
V_{IL}				0.3 • V_{DD}			✻	V
I_{IH}				±10			✻	µA
I_{IL}				±10			✻	µA
DIGITAL OUTPUT								
V_{OH}	$I_{OH} = –0.8mA$	3.6	4.5		✻	✻		V
V_{OL}	$I_{OL} = 1.6mA$		0.3	0.4		✻	✻	V
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	✻	✻	✻	V
V_{CC}		+4.75	+5.0	+5.25	✻	✻	✻	V
V_{SS}		0	0	0	✻	✻	✻	V
I_{CC}			1.5	2		✻	✻	mA
I_{DD}			50			✻		µA
Power			7.5	10		✻	✻	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	✻		✻	°C

NOTE: (1) If $V_{SS} = 0V$ specification applies at Code 0040_H and above due to possible negative zero-scale error.

✻ Specifications same as DAC7634E.

ABSOLUTE MAXIMUM RATINGS[1]

V_{CC} and V_{DD} to V_{SS}	–0.3V to 11V
V_{CC} and V_{DD} to GND	–0.3V to 5.5V
$V_{REF}L$ to V_{SS}	–0.3V to (V_{CC} – V_{SS})
V_{CC} to $V_{REF}H$	–0.3V to (V_{CC} – V_{SS})
$V_{REF}H$ to $V_{REF}L$	–0.3V to (V_{CC} – V_{SS})
Digital Input Voltage to GND	–0.3V to V_{DD} + 0.3V
Digital Output Voltage to GND	–0.3V to V_{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	LINEARITY ERROR (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER[1]	TRANSPORT MEDIA
DAC7634E	±4	±3	48-Lead SSOP	333	–40°C to +85°C	DAC7634E	Rails
"	"	"	"	"	"	DAC7634E/1K	Tape and Reel
DAC7634EB	±3	±2	48-Lead SSOP	333	–40°C to +85°C	DAC7634EB	Rails
"	"	"	"	"	"	DAC7634EB/1K	Tape and Reel

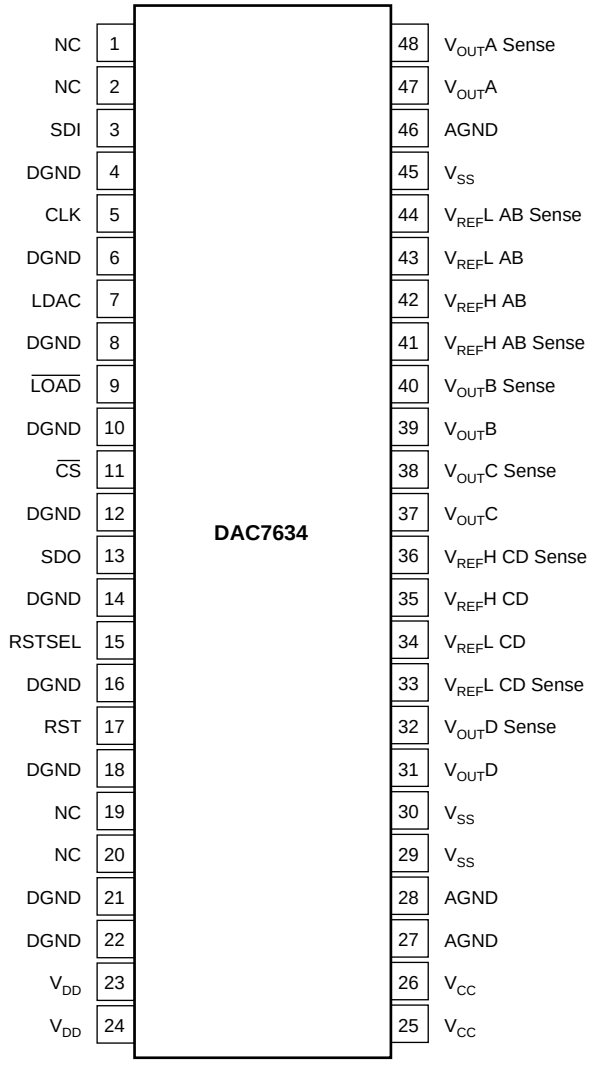
NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC7634E/1K" will get a single 1000-piece Tape and Reel.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	NC	No Connection	24	V_{DD}	Digital +5V Power Supply
2	NC	No Connection	25	V_{CC}	Analog +5V Power Supply
3	SDI	Serial Data Input	26	V_{CC}	Analog +5V Power Supply
4	DGND	Digital Ground	27	AGND	Analog Ground
5	CLK	Data Clock Input	28	AGND	Analog Ground
6	DGND	Digital Ground	29	V_{SS}	Analog –5V Power Supply or 0V Single Supply
7	LDAC	DAC Register Load Control, Rising Edge Triggered	30	V_{SS}	Analog –5V Power Supply or 0V Single Supply
			31	$V_{OUT}D$	DAC D Output Voltage
8	DGND	Digital Ground	32	$V_{OUT}D$ Sense	DAC D's Output Amplifier Inverting Input. Used to close feedback loop at load.
9	$\overline{LOAD}$	DAC Input Register Load Control, Active Low			
10	DGND	Digital Ground	33	$V_{REF}L$ CD Sense	DAC C and D Reference Low Sense Input
11	$\overline{CS}$	Chip Select, Active Low	34	$V_{REF}L$ CD	DAC C and D Reference Low Input
12	DGND	Digital Ground	35	$V_{REF}H$ CD	DAC C and D Reference High Input
13	SDO	Serial Data Output	36	$V_{REF}H$ CD Sense	DAC C and D Reference High Sense Input
14	DGND	Digital Ground	37	$V_{OUT}C$	DAC C Output Voltage
15	RSTSEL	Reset Select. Determines the action of RST. If HIGH, a RST common will set the DAC registers to mid-scale (8000H). If LOW, a RST command will set the DAC registers to zero (0000H).	38	$V_{OUT}C$ Sense	DAC C's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
			39	$V_{OUT}B$	DAC B Output Voltage
16	DGND	Digital Ground	40	$V_{OUT}B$ Sense	DAC B's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
17	RST	Reset, Rising Edge Triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale or zero.	41	$V_{REF}H$ AB Sense	DAC A and B Reference High Sense Input
			42	$V_{REF}H$ AB	DAC A and B Reference High Input
18	DGND	Digital Ground	43	$V_{OUT}L$ AB	DAC A and B Reference Low Input
19	NC	No Connection	44	$V_{REF}L$ AB Sense	DAC A and B Reference Low Sense Input
20	NC	No Connection	45	V_{SS}	Analog –5V Power Supply or 0V Single Supply
21	DGND	Digital Ground	46	AGND	Analog Ground
22	DGND	Digital Ground	47	$V_{OUT}A$	DAC A Output Voltage
23	V_{DD}	Digital +5V Power Supply	48	$V_{OUT}A$ Sense	DAC A's Output Amplifier Inverting Input. Used to close the feedback loop at the load.

PIN CONFIGURATION

Top View **SSOP**

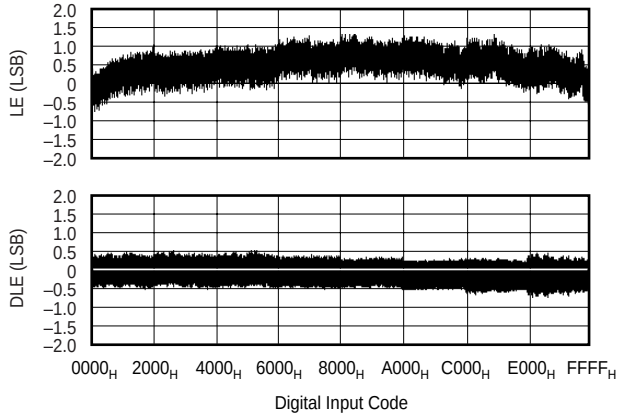


TYPICAL PERFORMANCE CURVES: V_{SS} = 0V

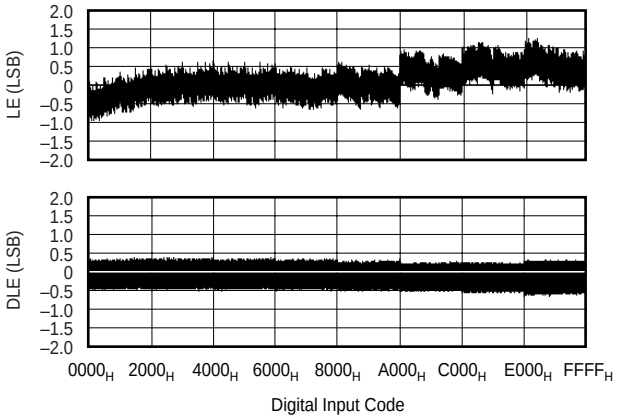
At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

+25°C

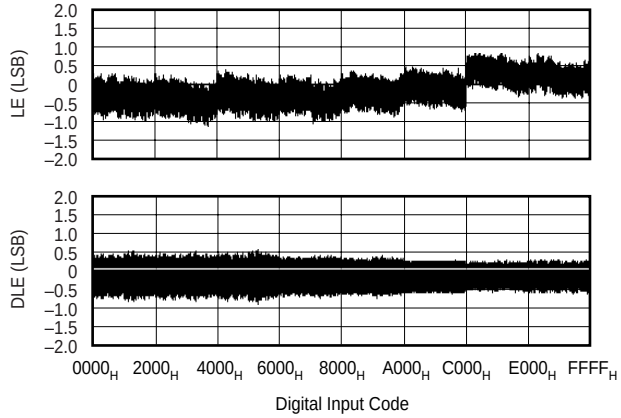
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +25°C)



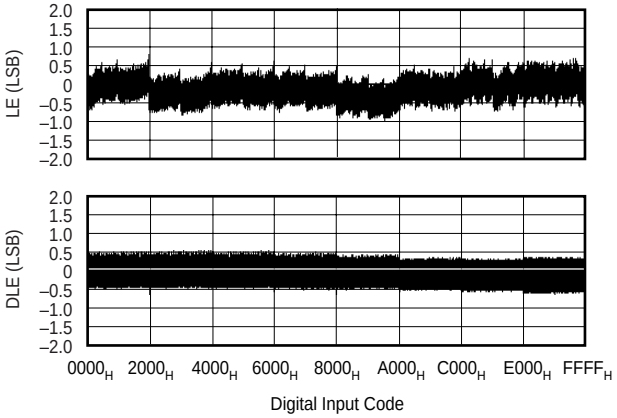
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +25°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +25°C)

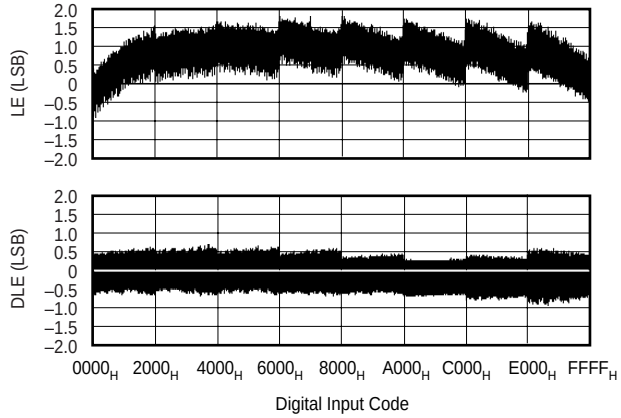


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +25°C)

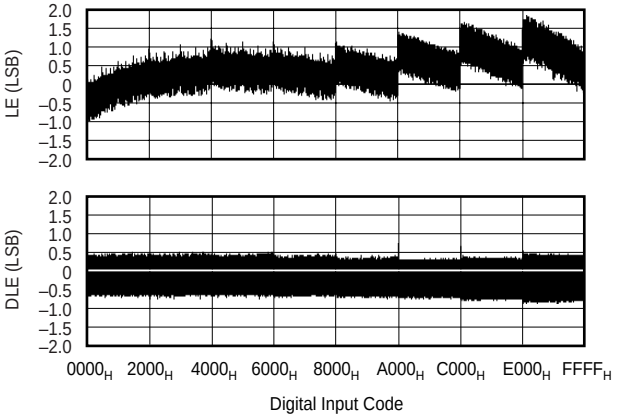


+85°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +85°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85°C)

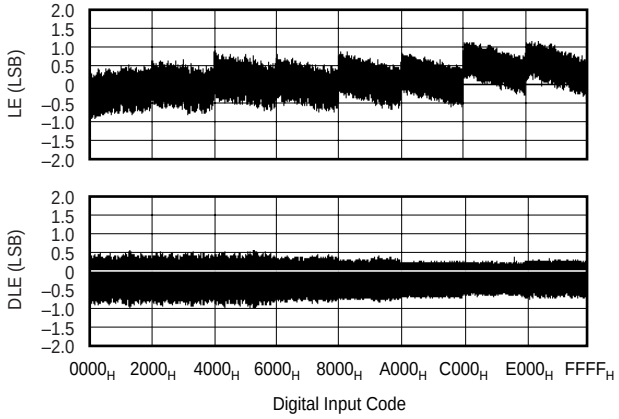


TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

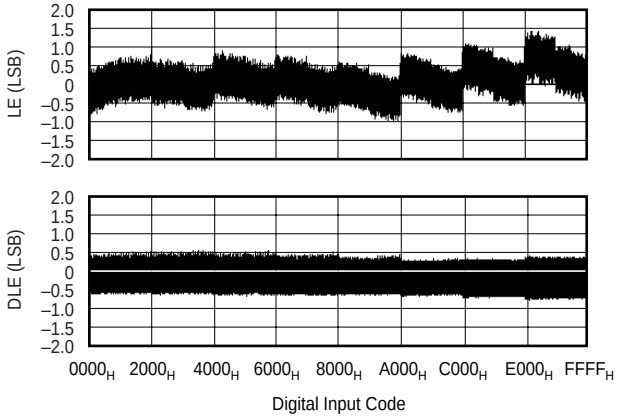
At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

+85°C (cont.)

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +85°C)

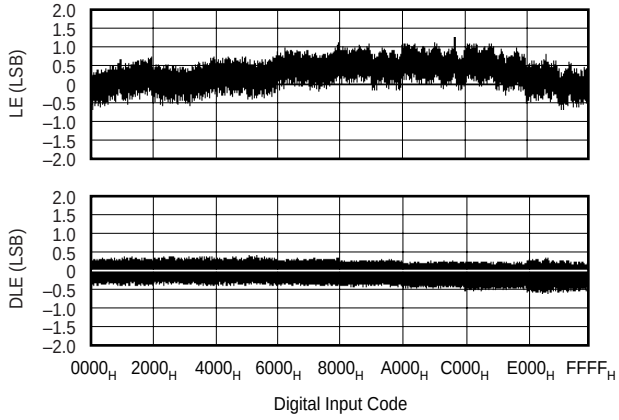


LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +85°C)

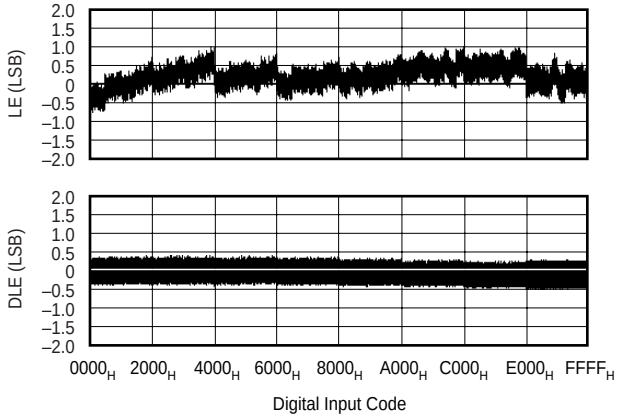


–40°C

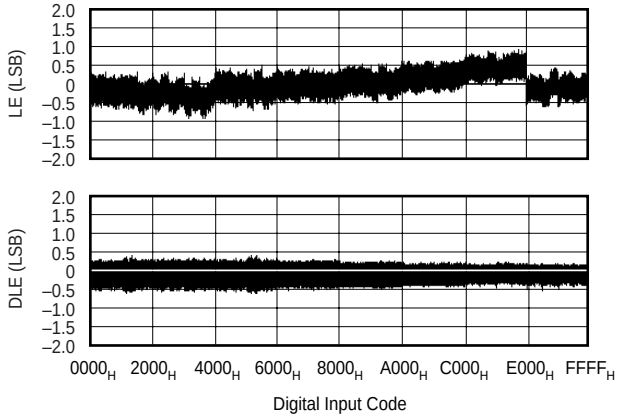
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, –40°C)



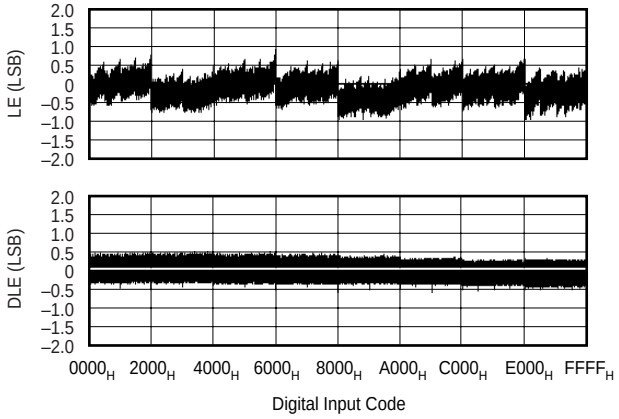
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, –40°C)



LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, –40°C)



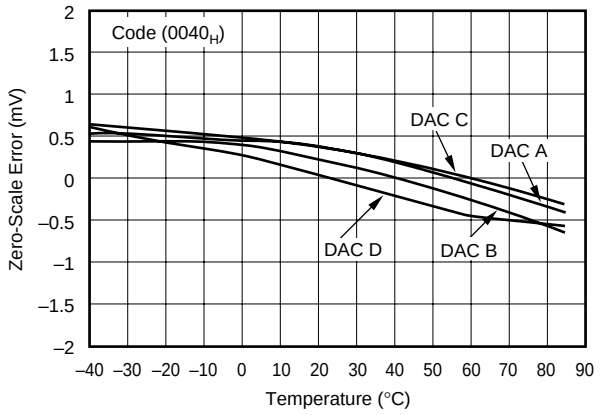
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, –40°C)



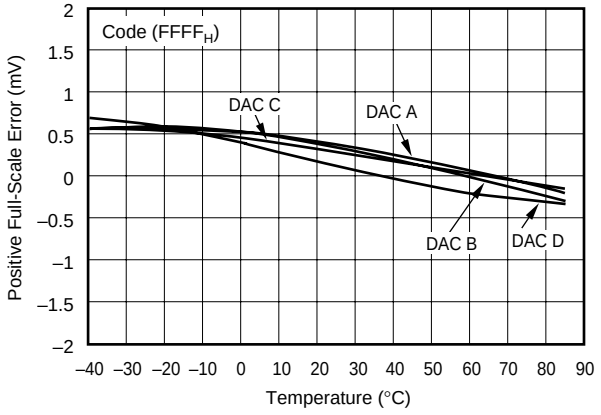
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

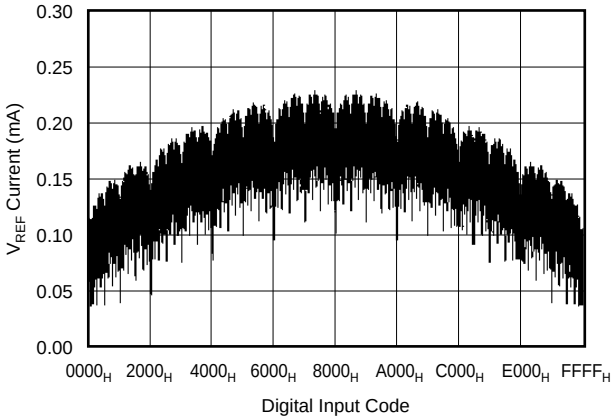
ZERO-SCALE ERROR vs TEMPERATURE



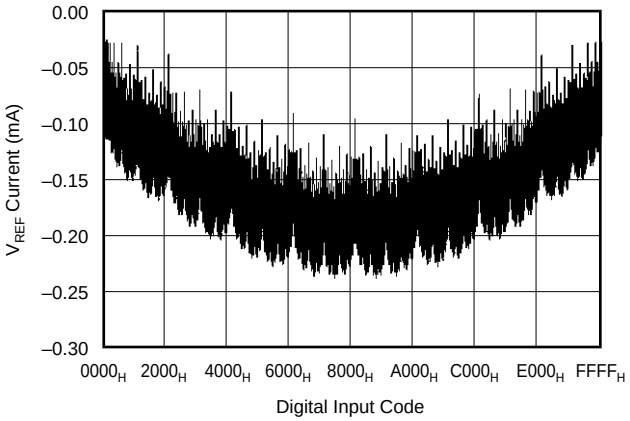
FULL-SCALE ERROR vs TEMPERATURE



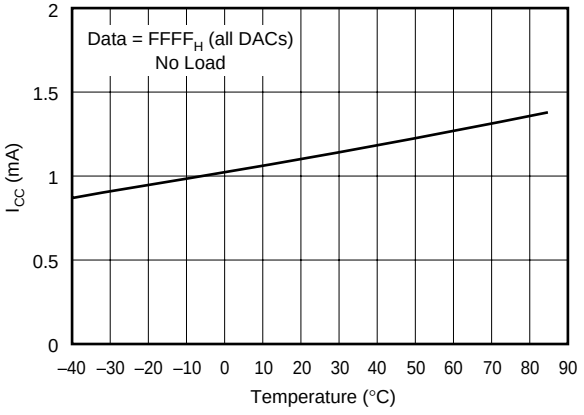
V_{REFH} CURRENT vs CODE
(all DACs sent to indicated code)



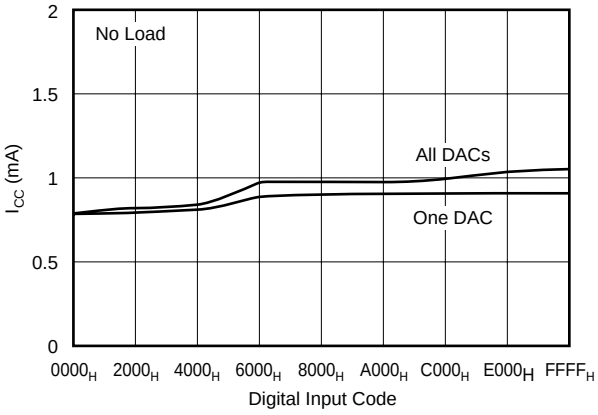
V_{REFL} CURRENT vs CODE
(all DACs sent to indicated code)



POWER SUPPLY CURRENT vs TEMPERATURE



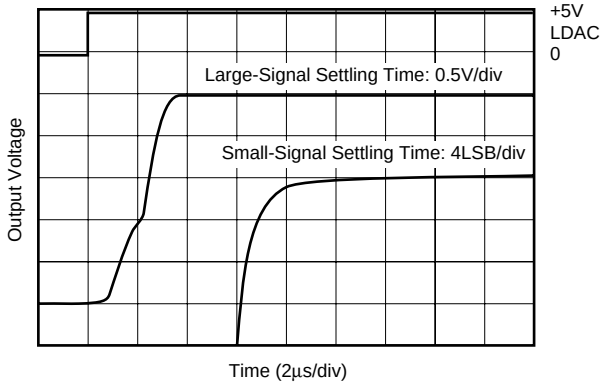
POSITIVE SUPPLY CURRENT
vs DIGITAL INPUT CODE



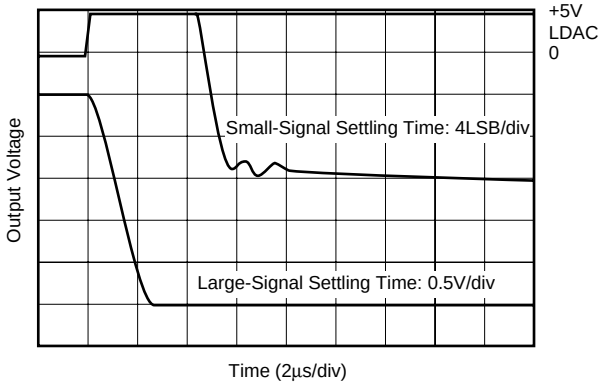
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

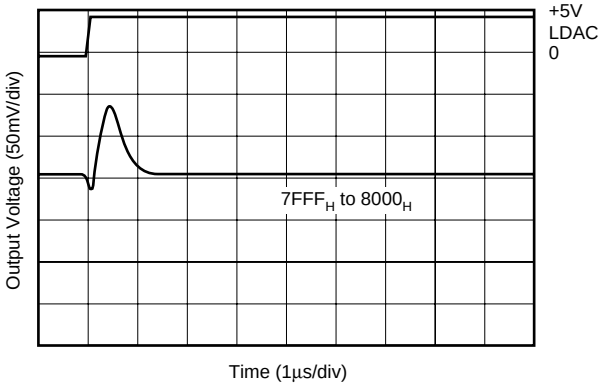
OUTPUT VOLTAGE vs SETTLING TIME
(0V to +2.5V)



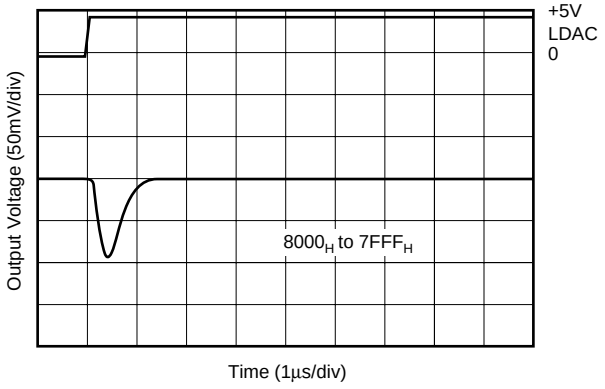
OUTPUT VOLTAGE vs SETTLING TIME
(+2.5V to 2mV)



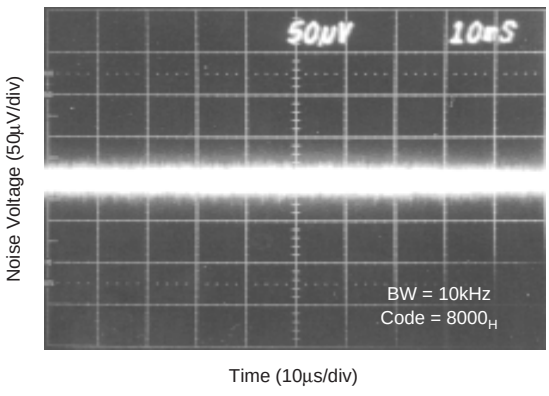
OUTPUT VOLTAGE
vs MIDSCALE GLITCH PERFORMANCE



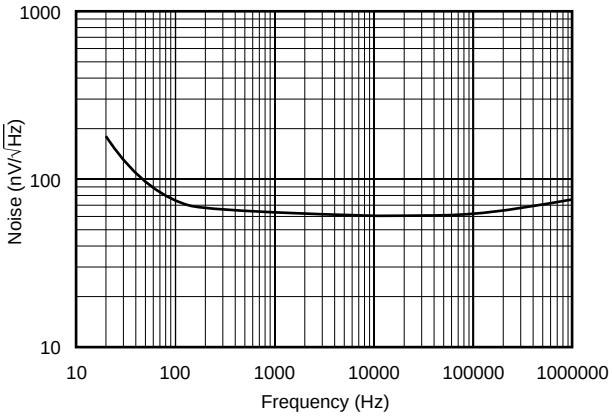
OUTPUT VOLTAGE
vs MIDSCALE GLITCH PERFORMANCE



BROADBAND NOISE

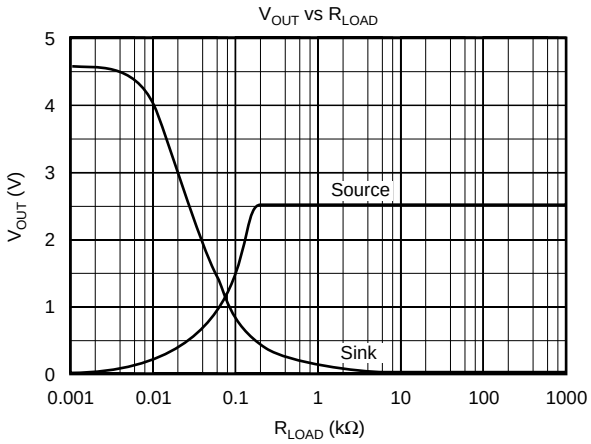


OUTPUT NOISE VOLTAGE vs FREQUENCY



TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = 0V, V_{REFH} = +2.5V, V_{REFL} = 0V, representative unit, unless otherwise specified.

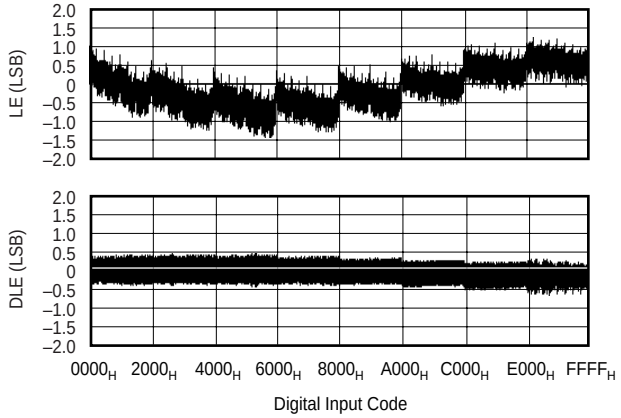


TYPICAL PERFORMANCE CURVES: V_{SS} = –5V

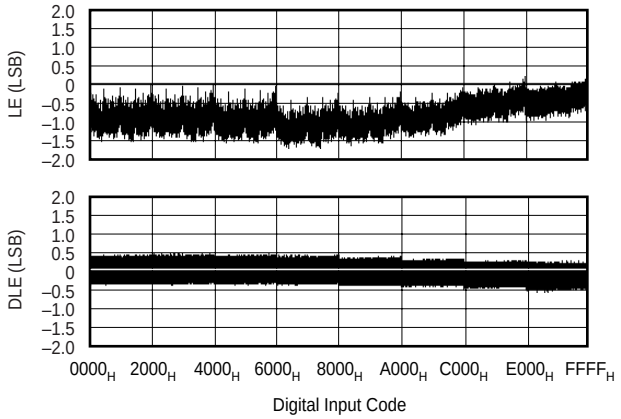
At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.

+25°C

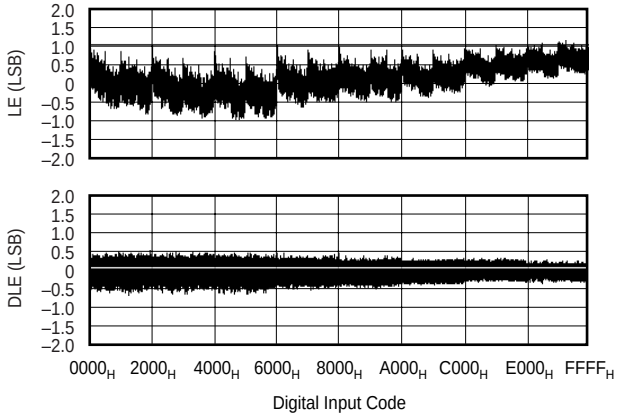
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +25°C)



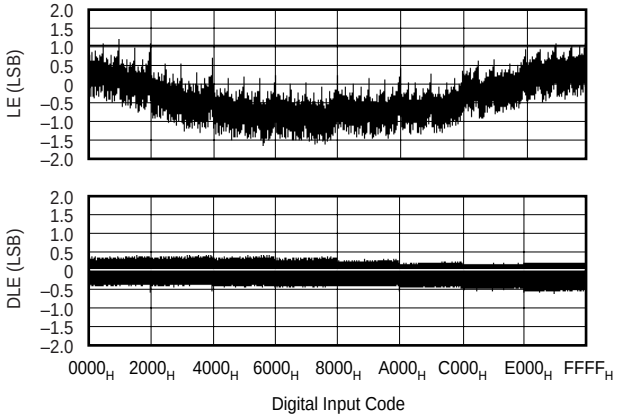
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +25°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +25°C)

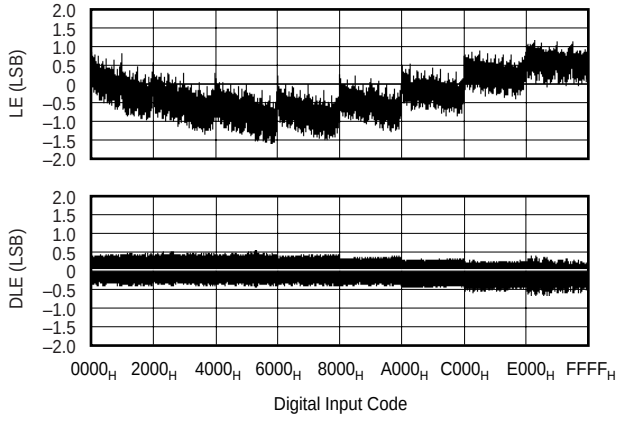


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +25°C)

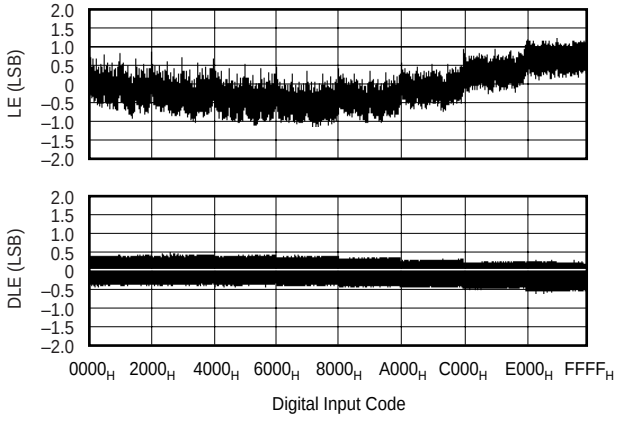


+85°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +85°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85°C)

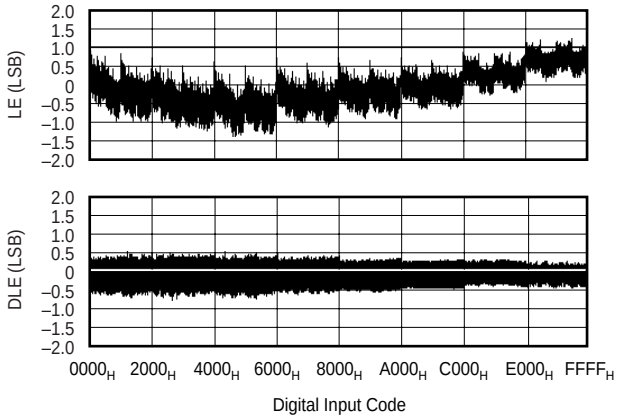


TYPICAL PERFORMANCE CURVES: V_{SS} = –5V (Cont.)

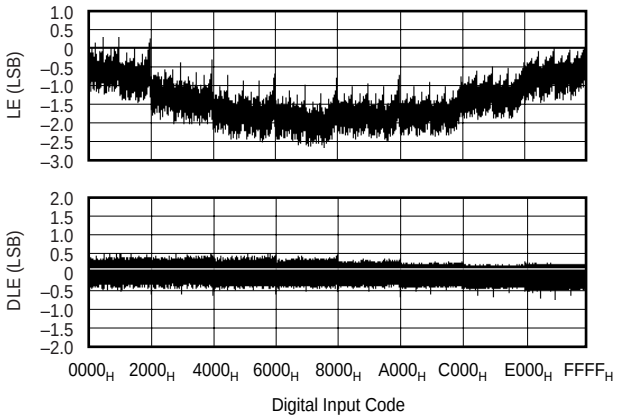
At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.

+85°C (cont.)

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +85°C)

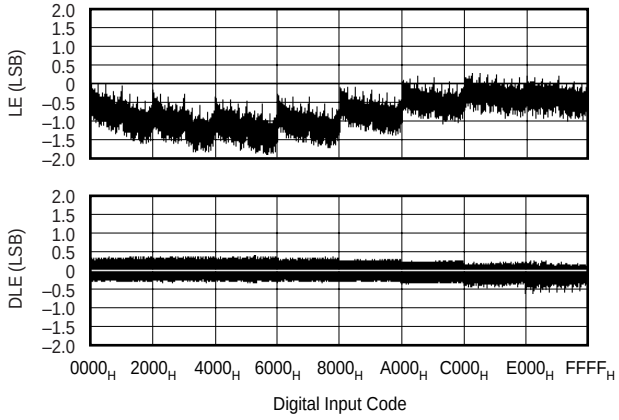


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +85°C)

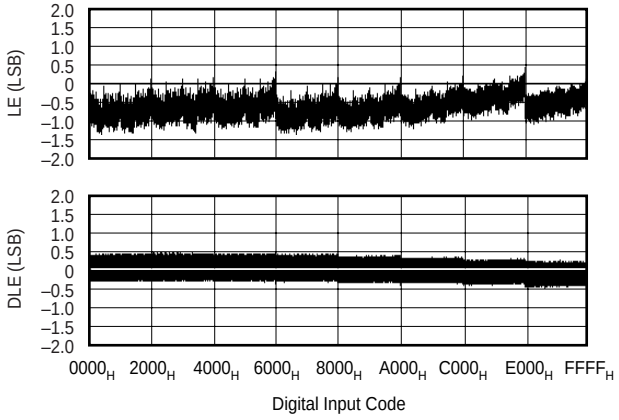


–40°C

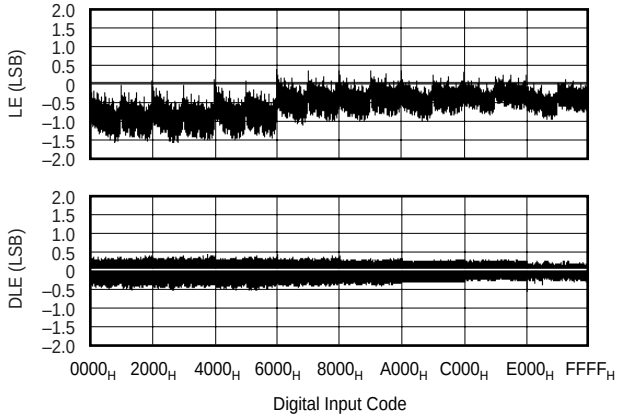
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, –40°C)



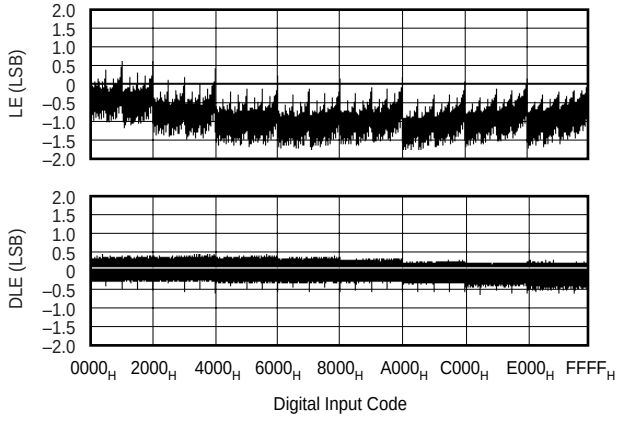
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, –40°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, –40°C)



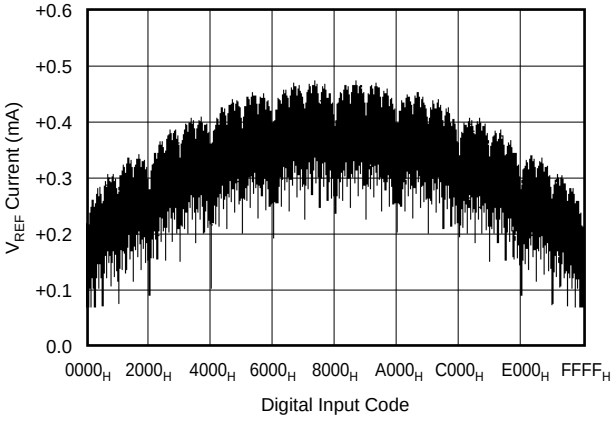
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, –40°C)



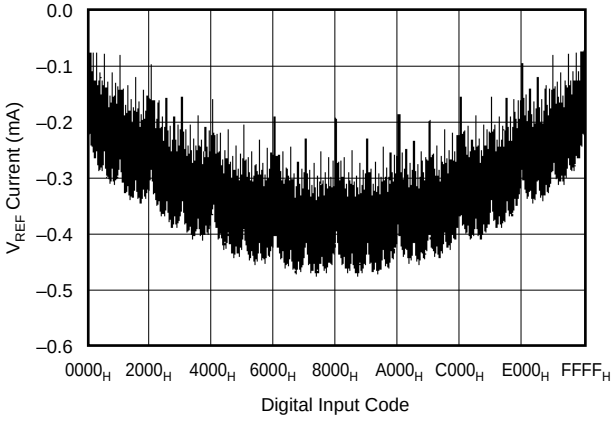
TYPICAL PERFORMANCE CURVES: V_{SS} = –5V (Cont.)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.

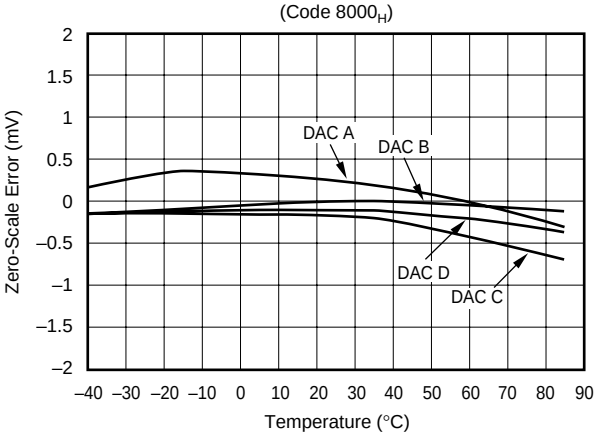
V_{REFH} CURRENT vs CODE
(all DACs sent to indicated code)



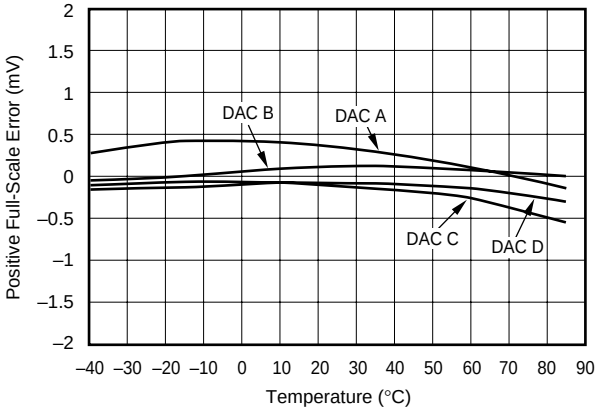
V_{REFL} CURRENT vs CODE
(all DACs sent to indicated code)



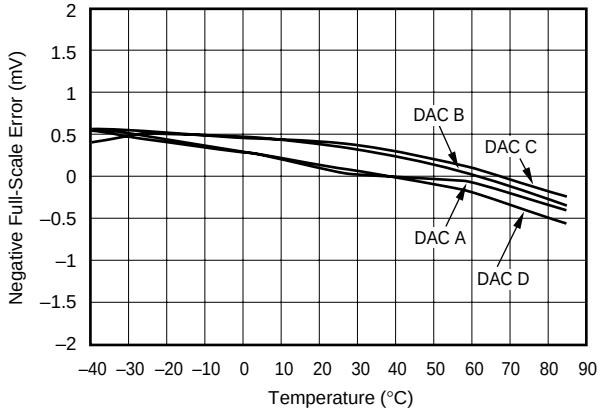
ZERO-SCALE ERROR vs TEMPERATURE
(Code 8000_H)



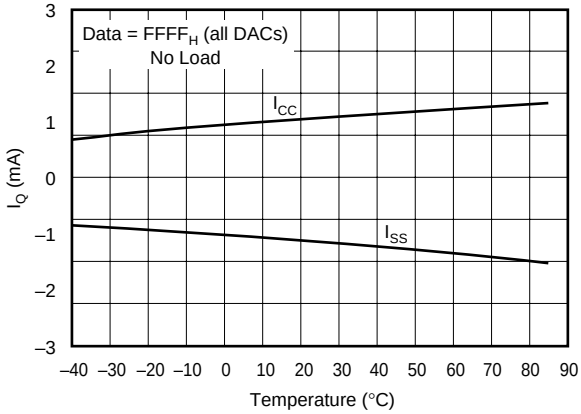
POSITIVE FULL-SCALE ERROR vs TEMPERATURE
(Code $FFFF_H$)



NEGATIVE FULL-SCALE ERROR vs TEMPERATURE
(Code 0000_H)



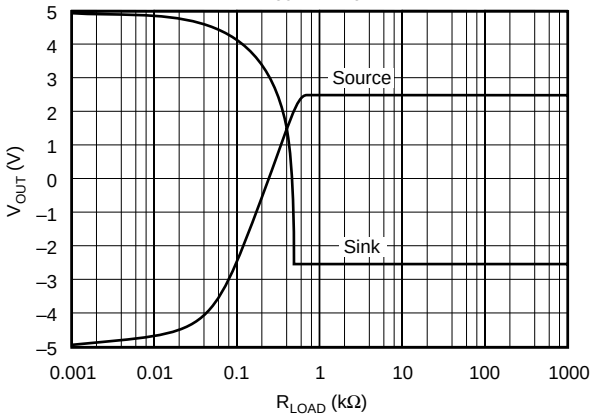
POWER SUPPLY CURRENT vs TEMPERATURE



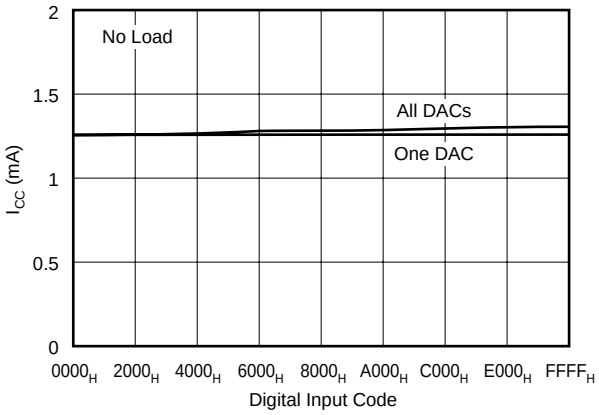
TYPICAL PERFORMANCE CURVES: V_{SS} = –5V (Cont.)

At T_A = +25°C, V_{DD} = V_{CC} = +5V, V_{SS} = –5V, V_{REFH} = +2.5V, V_{REFL} = –2.5V, representative unit, unless otherwise specified.

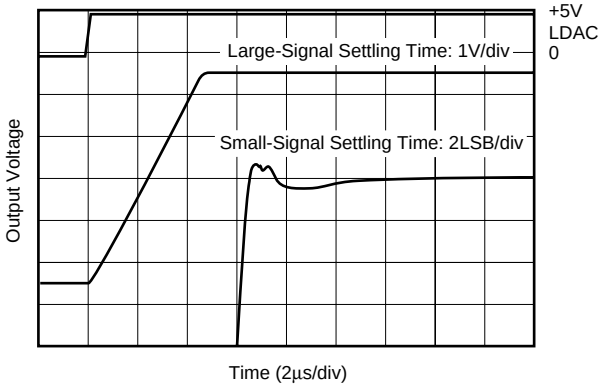
V_{OUT} vs R_{LOAD}



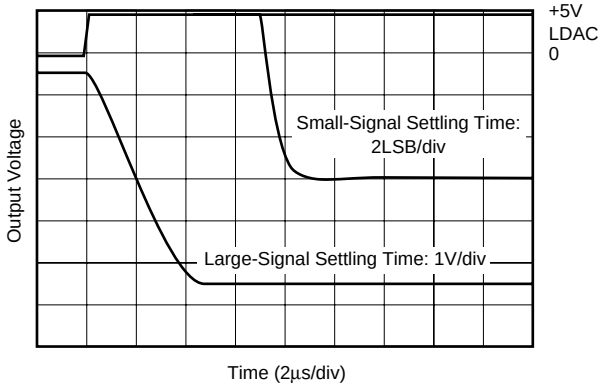
POSITIVE SUPPLY CURRENT vs DIGITAL INPUT CODE



OUTPUT VOLTAGE vs SETTLING TIME (–2.5V to +2.5V)



OUTPUT VOLTAGE vs SETTLING TIME (+2.5V to –2.5V)



THEORY OF OPERATION

The DAC7634 is a quad voltage output, 16-bit Digital-to-Analog Converter (DAC). The architecture is an R-2R ladder configuration with the three MSB's segmented, followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network, segmented MSBs, and output op amp, as shown in Figure 1. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the external voltage references ($V_{REF}L$ and $V_{REF}H$, respectively).

The digital input is a 24-bit serial word that contains the 16-bit DAC code (LSB first), five unused bits, a quick load bit, and a 2-bit address code for selecting one of the four DACs. The converters can be powered from either a single +5V supply or a dual ±5V supply. The device offers a reset function which immediately sets all DAC output voltages and DAC registers to mid-scale code 8000_H or to zero-scale, code 0000_H. See Figures 2 and 3 for the basic operation of the DAC7634.

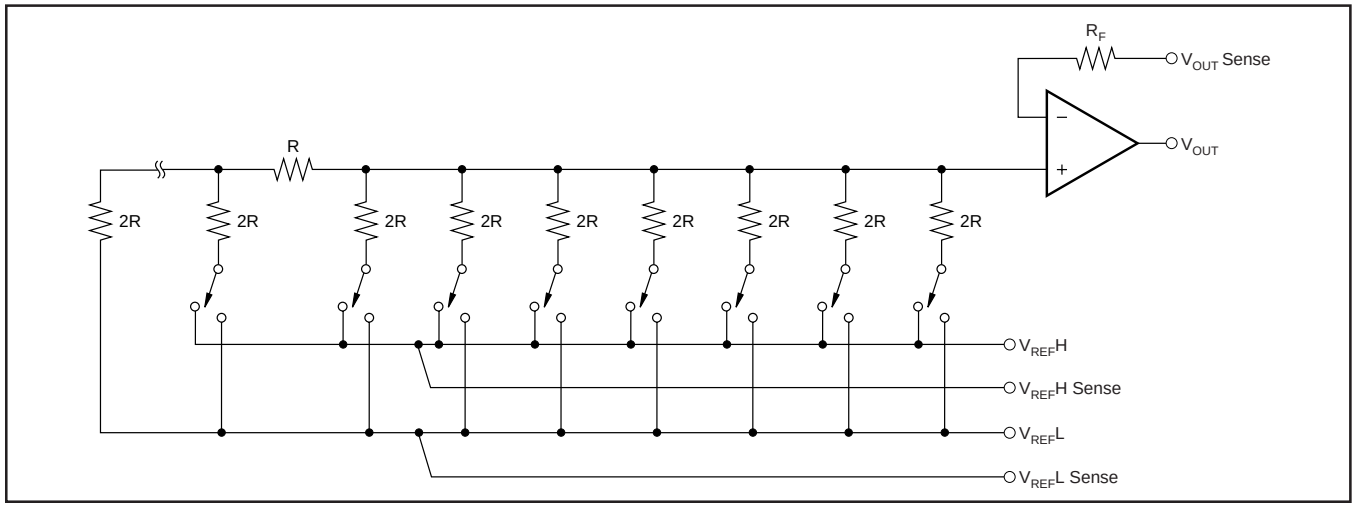


FIGURE 1. DAC7634 Architecture.

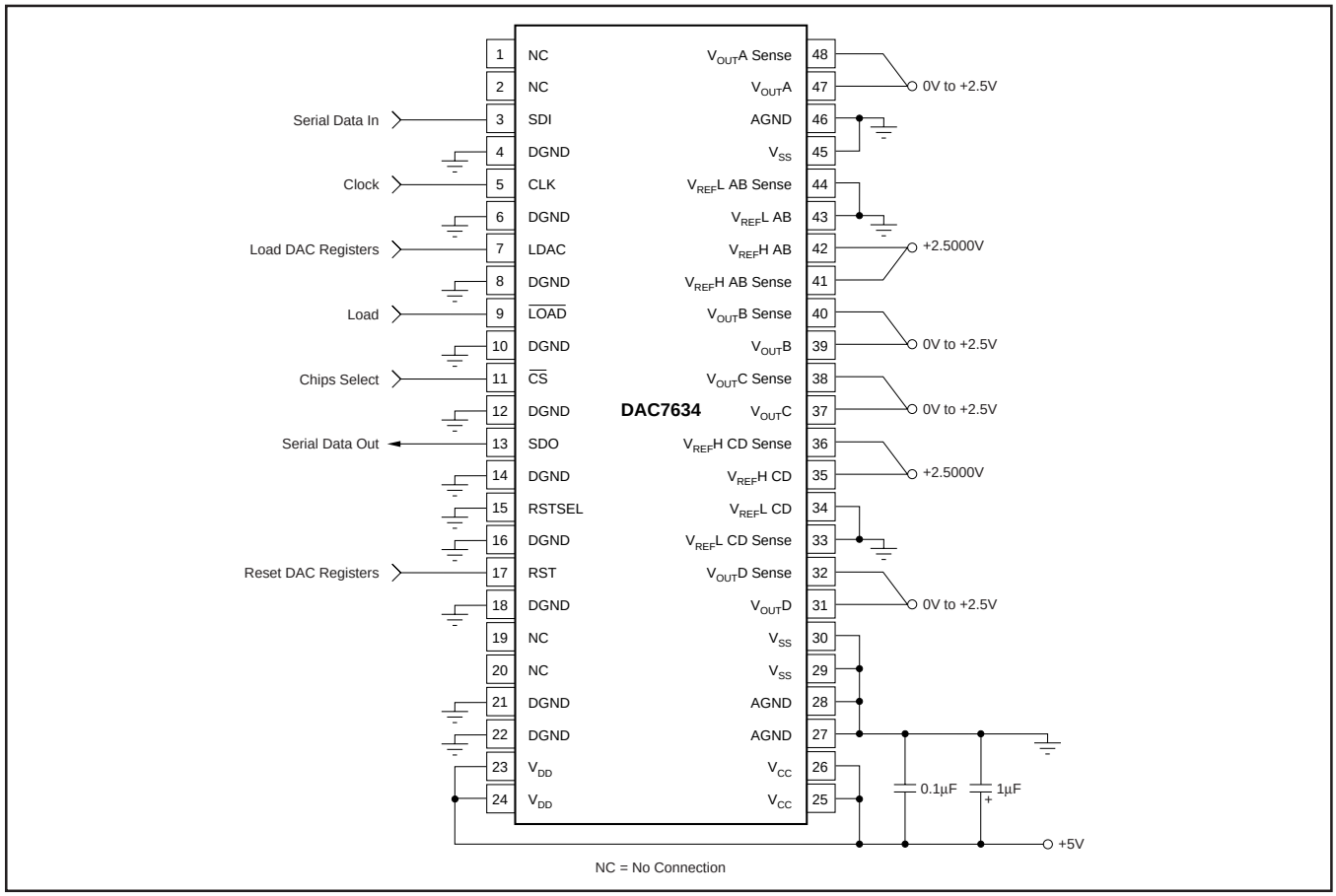


FIGURE 2. Basic Single-Supply Operation of the DAC7634.

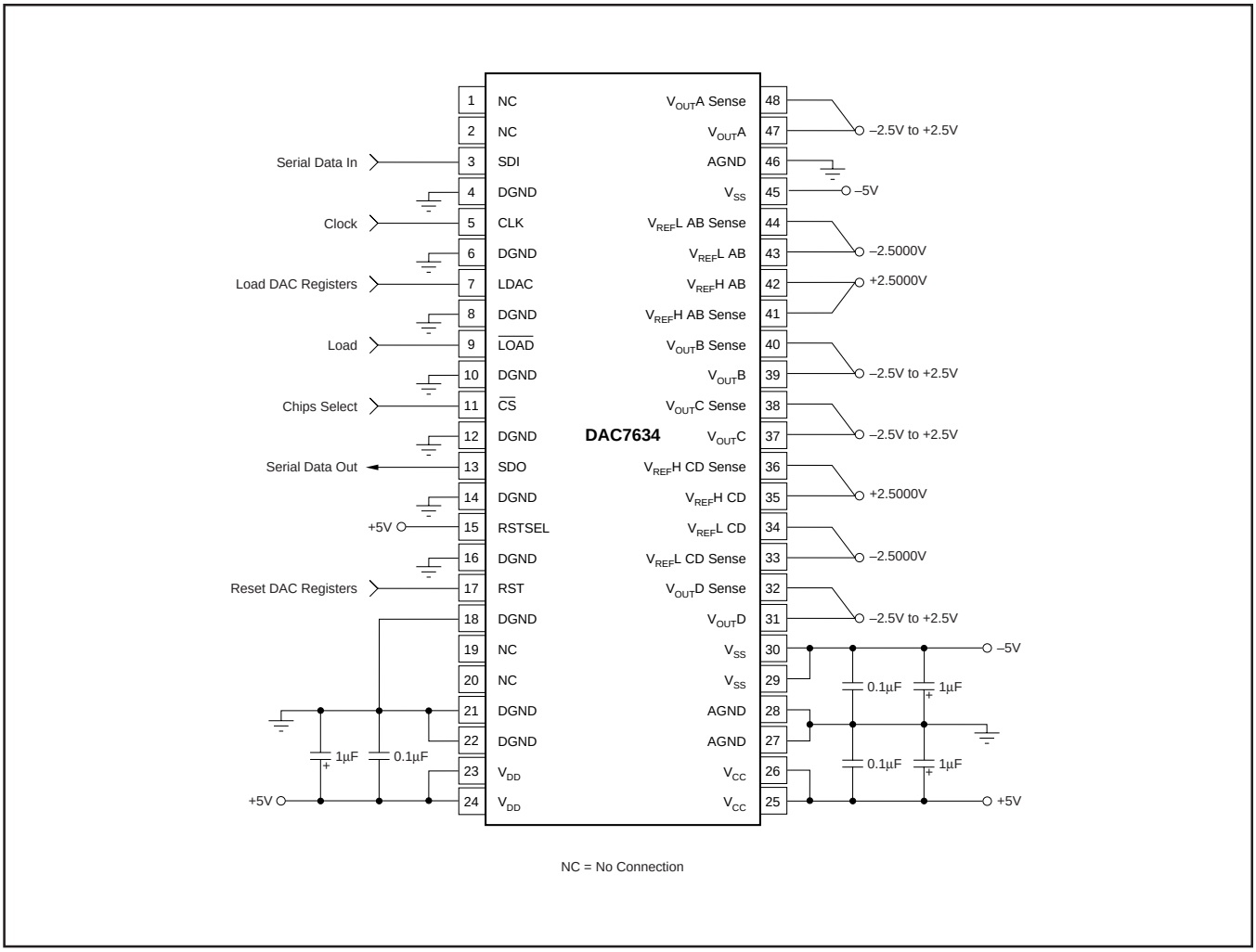


FIGURE 3. Basic Dual-Supply Operation of the DAC7634.

ANALOG OUTPUTS

When V_{SS} = –5V (dual supply operation), the output amplifier can swing to within 2.25V of the supply rails, guaranteed over the –40°C to +85°C temperature range. When V_{SS} = 0V (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when V_{SS} = 0V. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000_H, 0001_H, 0002_H, etc.) if the output amplifier has a negative offset. At the negative limit of –2mV, the first specified output starts at code 0040_H.

Due to the high accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 2.5V full-scale range has a 1LSB value of 38µV. With a load current of 1mA, series wiring and connector resistance of only 40mΩ (R_{W2}) will cause a voltage drop of 40µV, as shown in Figure 4. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 1mA load, a 10 milli-inch wide printed circuit conductor 600 milli-inches long will result in a voltage drop of 30µV.

The DAC7634 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 4), thus ensuring an accurate output voltage.

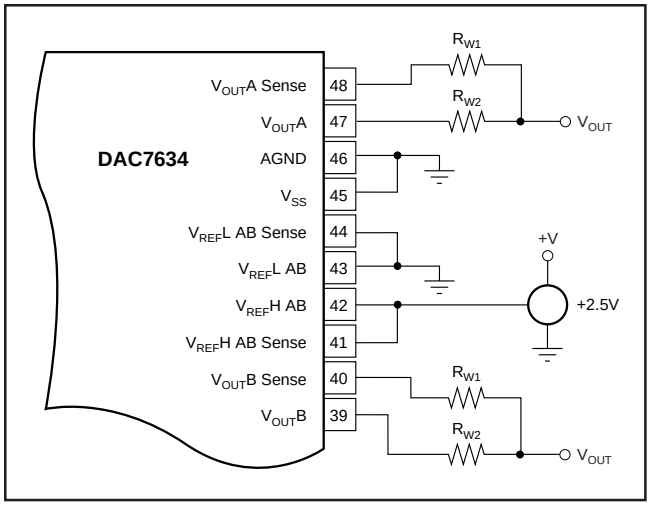


FIGURE 4. Analog Output Closed-Loop Configuration (1/2 DAC7634). R_W represents wiring resistances.

REFERENCE INPUTS

The reference inputs, $V_{REF}L$ and $V_{REF}H$, can be any voltage between V_{SS} + 2.5V and V_{CC} – 2.5V, provided that $V_{REF}H$ is at least 1.25V greater than $V_{REF}L$. The minimum output of each DAC is equal to $V_{REF}L$ plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to $V_{REF}H$ plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of –4.75V to –5.25V. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the $V_{REF}H$ input and out of $V_{REF}L$ depends on the DAC output voltages, and can vary from a few microamps to approximately 0.5mA. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC7634 features a reference drive and sense connection such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figures 5 through 13 show different reference configurations, and the effect on the linearity and differential linearity.

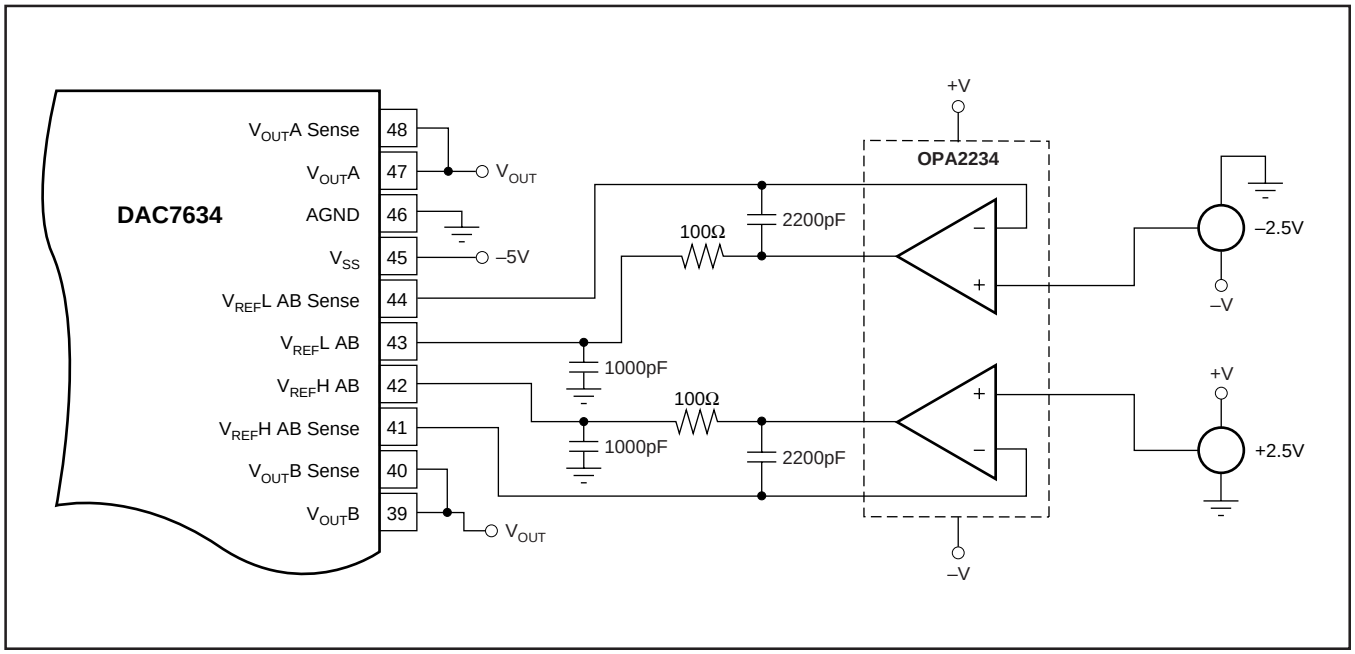
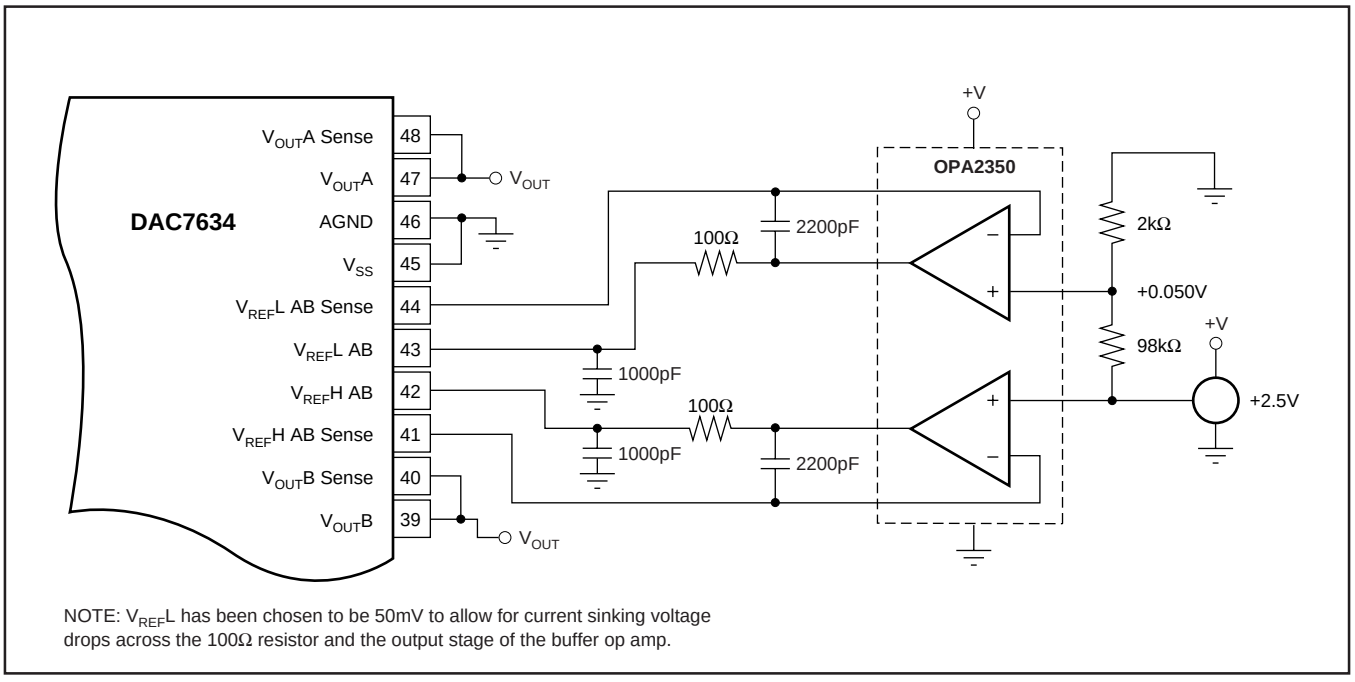


FIGURE 5. Dual Supply Configuration-Buffered References, used for Dual Supply Performance



NOTE: $V_{REF}L$ has been chosen to be 50mV to allow for current sinking voltage drops across the 100Ω resistor and the output stage of the buffer op amp.

FIGURE 6. Single-Supply Buffered Reference with a Reference Low of 50mV (1/2 DAC7634).

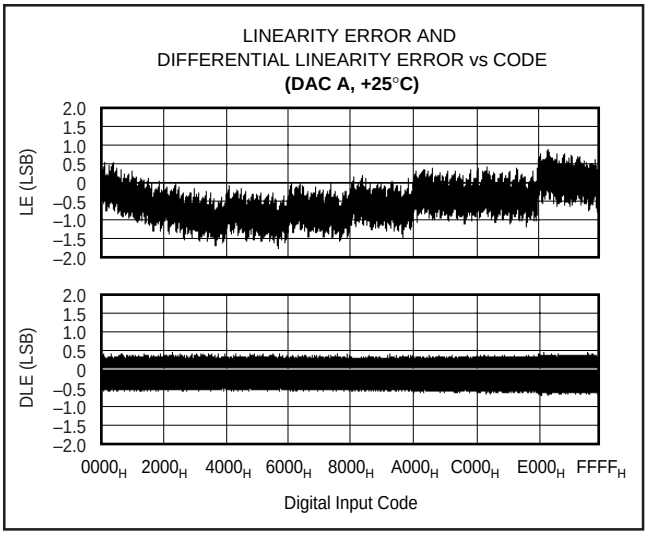


FIGURE 7. Integral Linearity and Differential Linearity Error Curves for Figure 6.

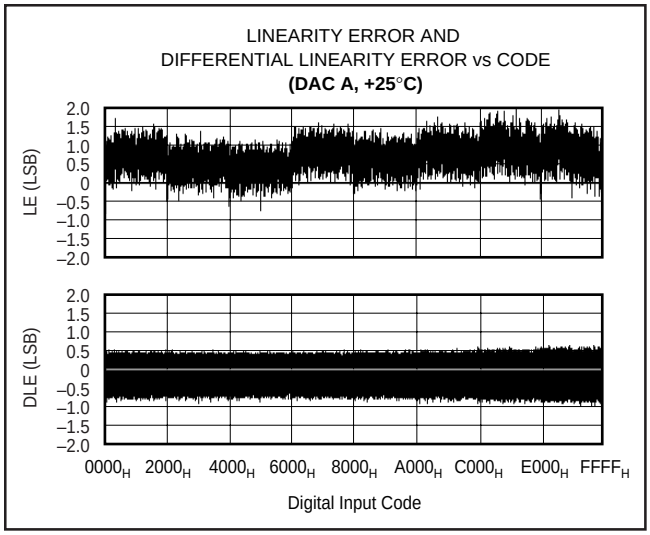


FIGURE 8. Integral Linearity and Differential Linearity Error Curves for Figure 9.

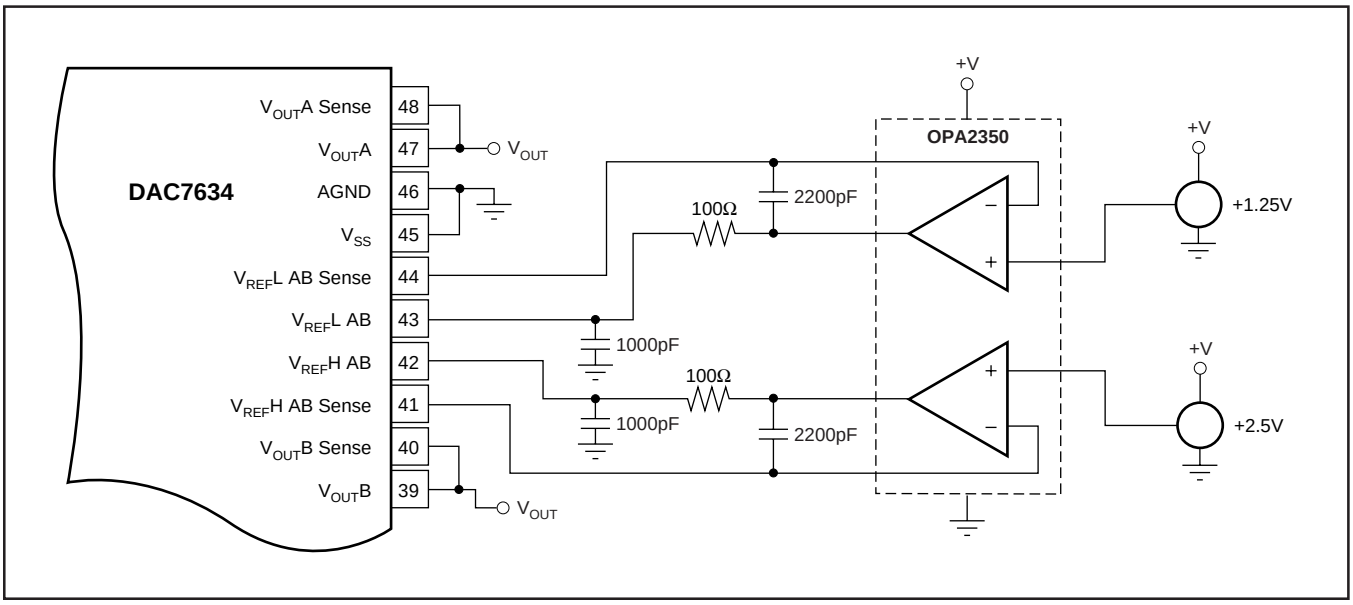


FIGURE 9. Single-Supply Buffered Reference with $V_{REF}L$ = +1.25V and $V_{REF}H$ = +2.5V (1/2 DAC7634).

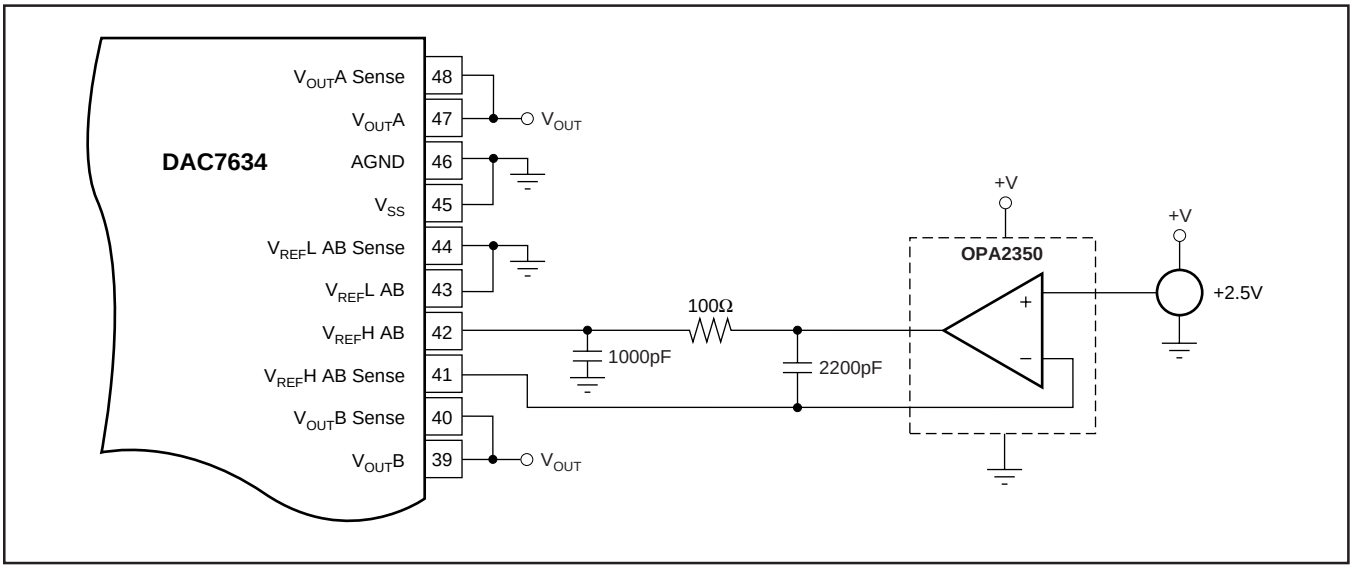


FIGURE 10. Single-Supply Buffered $V_{REF}H$ (1/2 DAC7634).

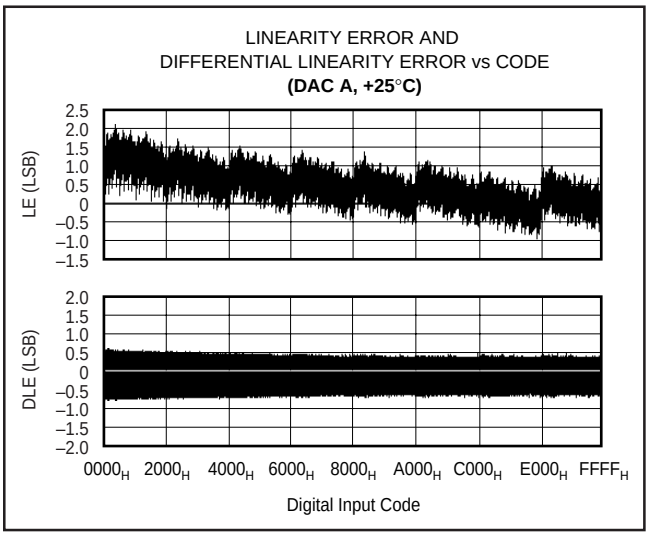


FIGURE 11. Linearity and Differential Linearity Error Curves for Figure 10.

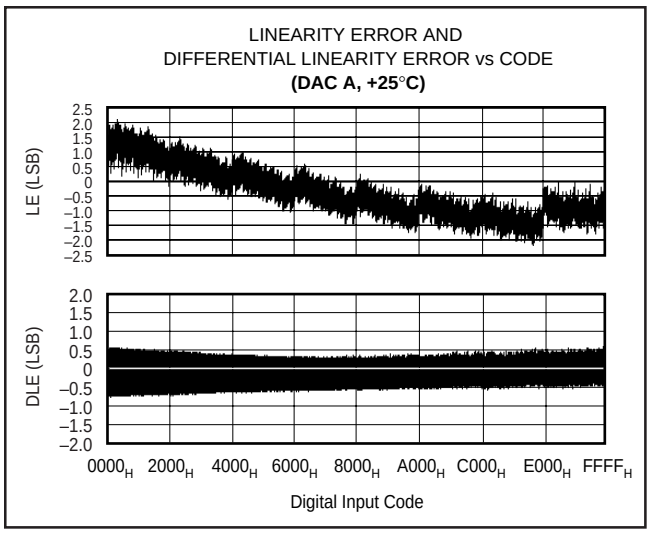


FIGURE 13. Linearity and Differential Linearity Error Curves for Figure 12.

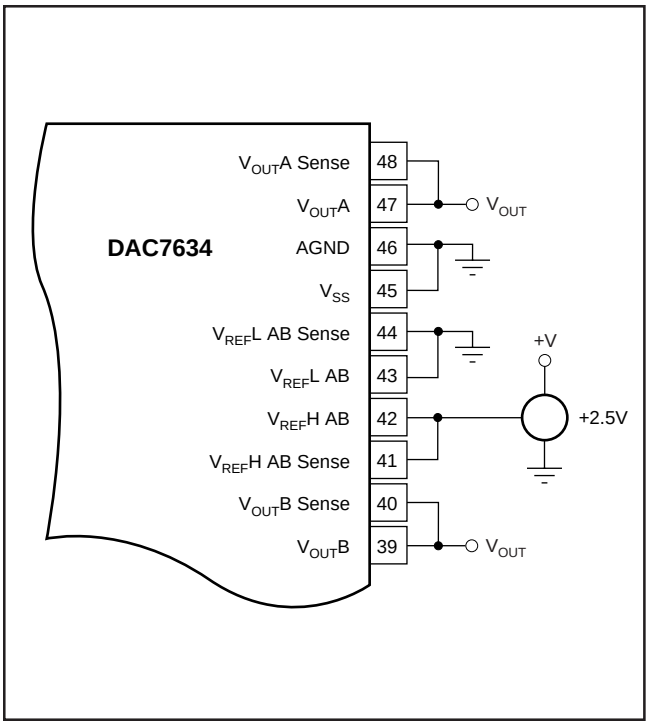


FIGURE 12. Low Cost Single-Supply Configuration.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7634. The interface consists of a Signal Data Clock (CLK) input, Serial Data (SDI), DAC Input Register Load Control Signal ($\overline{\text{LOAD}}$), and DAC Register Load Control Signal (LDAC). In addition, a Chip Select ($\overline{\text{CS}}$) input is available to enable serial communication when there are multiple serial devices. An asynchronous Reset (RST) input, by the rising edge, is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state, depending on the status of the reset select (RSTSEL) signal.

The DAC code, quick load control, and address are provided via a 24-bit serial interface (see Figure 15). The first sixteen bits (LSB first) are the DAC code followed by five unused bits. The twenty-second bit is a "Quick Load" bit such that if HIGH, the code in the shift register is loaded into ALL DAC's input register when $\overline{\text{Load}}$ signal goes LOW. If the "Quick Load" bit is LOW, the content of shift register is loaded only to the DAC input register that is addressed. The last two bits select the input register that will be updated when $\overline{\text{LOAD}}$ goes LOW.

SERIAL DATA INPUT

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A1	A0	QUICK LOAD	X	X	X	X	X	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

A1	A0	$\overline{\text{CS}}$	RST	RSTSEL	LDAC	$\overline{\text{LOAD}}$	INPUT REGISTER	DAC REGISTER	MODE	DAC
L	L	L	H	X	X	L	Write	Hold	Write Input	A
L	H	L	H	X	X	L	Write	Hold	Write Input	B
H	L	L	H	X	X	L	Write	Hold	Write Input	C
H	H	L	H	X	X	L	Write	Hold	Write Input	D
X	X	H	H	X	↑	H	Hold	Write	Update	All
X	X	H	H	X	H	H	Hold	Hold	Hold	All
X	X	X	↑	L	X	X	Reset to Zero	Reset to Zero	Reset to Zero	All
X	X	X	↑	H	X	X	Reset to Midscale	Reset to Midscale	Reset to Midscale	All

TABLE I. DAC7634 Logic Truth Table.

The internal DAC register is edge triggered and not level triggered. When the LDAC signal is transitioned from LOW to HIGH, the digital word currently in the DAC input register is latched. The first set of registers (the DAC input registers) are level triggered via the $\overline{LOAD}$ signal. This double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. When the new data has been entered into the device, all of the DAC outputs can be updated simultaneously by the rising edge of LDAC. Additionally, it allows the DAC input registers to be written to at any point, then the DAC output voltages can be synchronously changed via a trigger signal (LDAC).

Note that $\overline{CS}$ and CLK are combined with an OR gate, which controls the serial-to-parallel shift register. These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when $\overline{CS}$ rises at the end of a serial transfer. If CLK is LOW when $\overline{CS}$ rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong input register(s). If both $\overline{CS}$ and CLK are used, $\overline{CS}$ should rise only when CLK is HIGH. If not, then either CS or CLK can be used to operate the shift register. See Table II for more information.

SERIAL-DATA OUTPUT

$\overline{CS}$(1)	CLK(1)	$\overline{LOAD}$	RST	SERIAL SHIFT REGISTER
H(2)	X(3)	H	H	No Change
L(4)	L	H	H	No Change
L	↑(5)	H	H	Advanced One Bit
↑	L	H	H	Advanced One Bit
H(6)	X	L(7)	H	No Change
H(6)	X	H	↑(8)	No Change

NOTES: (1) $\overline{CS}$ and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a "false clock" from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while $\overline{LOAD}$ is LOW, the selected DAC register will change as the shift register bits "flow" through A1 and A0. This will corrupt the data in each DAC register that has been erroneously selected. (8) Rising edge of RST causes no change in the contents of the serial shift register.

TABLE II. Serial Shift Register Truth Table.

The Serial-Data Output (SDO) is the internal shift register's output. For DAC7634, the SDO is a driven output and does not require an external pull-up. Any number of DAC7634's can be daisy chained by connecting the SDO pin of one device to the SDI pin of the following device in the chain, as shown in Figure 14.

DIGITAL TIMING

Figure 15 and Table III provide detailed timing for the digital interface of the DAC7634.

DIGITAL INPUT CODING

The DAC7634 input data is in Straight Binary format. The output voltage is given by Equation 1.

where N is the digital input code. This equation does not

$$V_{OUT} = V_{REF}L + \frac{(V_{REF}H - V_{REF}L) \bullet N}{65,536} \qquad (1)$$

include the effects of offset (zero-scale) or gain (full-scale) errors.

DIGITALLY-PROGRAMMABLE CURRENT SOURCE

The DAC7634 offers a unique set of features that allows a wide range of flexibility in designing applications circuits such as programmable current sources. The DAC7634 offers both a differential reference input, as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows a transistor to be placed within the loop to implement a digitally-programmable, unidirectional current source. The availability of a differential reference allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left(\left(\frac{V_{REF}H - V_{REF}L}{R_{SENSE}}\right) \bullet \left(\frac{N}{65,536}\right)\right) + \left(V_{REF}L / R_{SENSE}\right) \qquad (2)$$

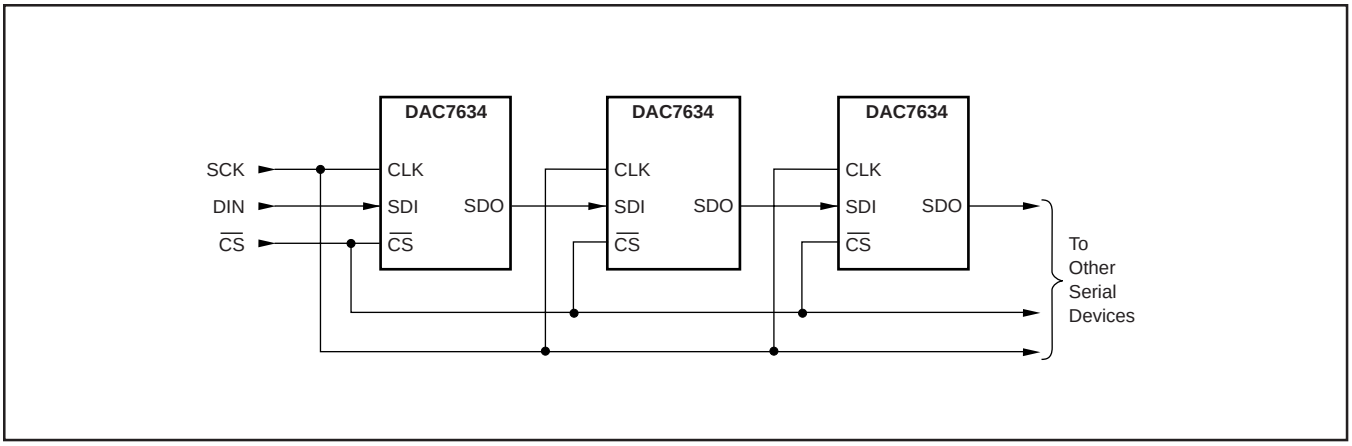


FIGURE 14. Daisy-Chaining DAC7634.

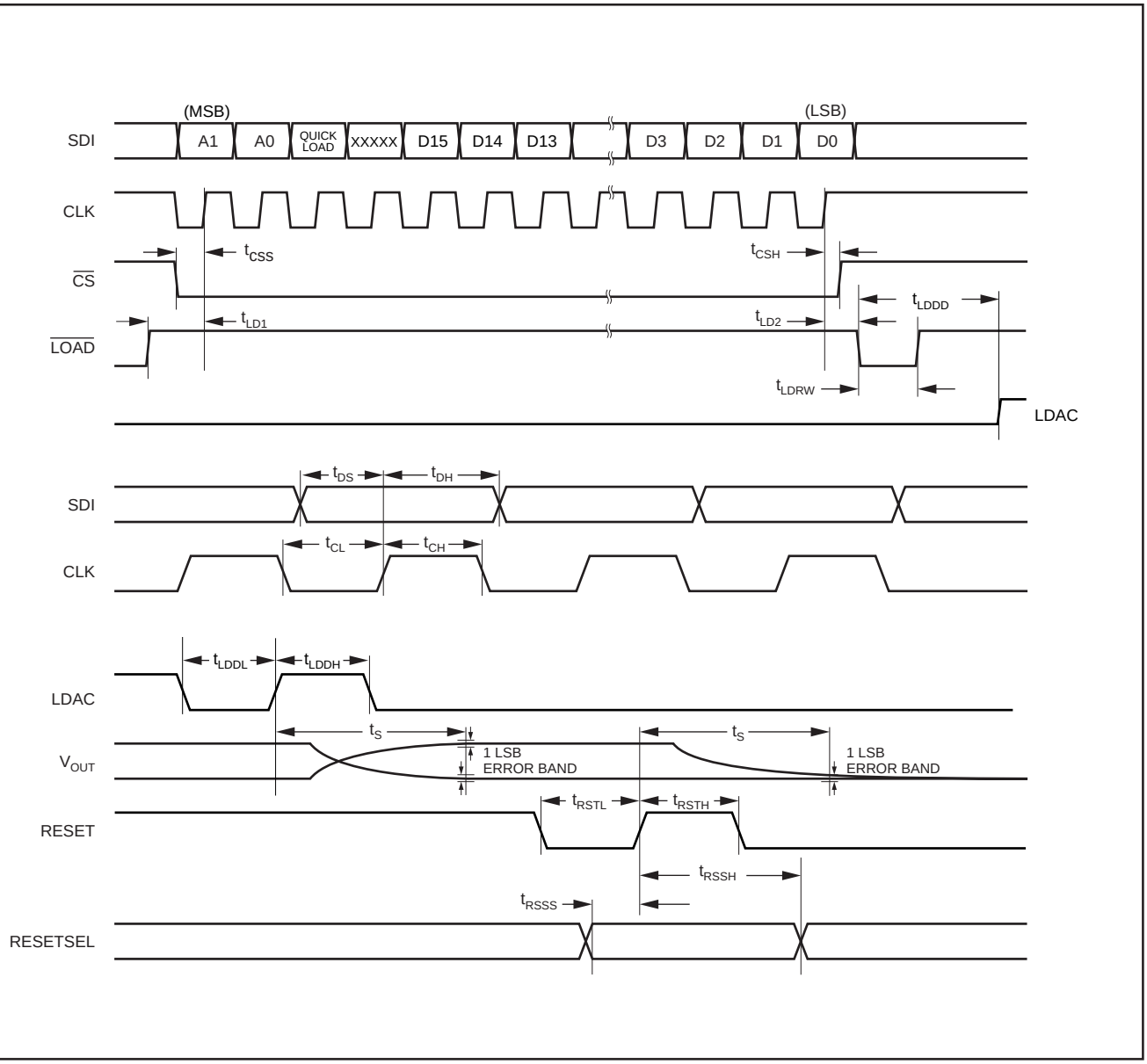


FIGURE 15. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	UNITS
t_{DS}	Data Valid to CLK Rising	10	ns
t_{DH}	Data Held Valid after CLK Rises	20	ns
t_{CH}	CLK HIGH	25	ns
t_{CL}	CLK LOW	25	ns
t_{CSS}	$\overline{CS}$ LOW to CLK Rising	15	ns
t_{CSH}	CLK HIGH to $\overline{CS}$ Rising	0	ns
t_{LD1}	$\overline{LOAD}$ HIGH to CLK Rising	10	ns
t_{LD2}	CLK Rising to $\overline{LOAD}$ LOW	30	ns
t_{LDRW}	$\overline{LOAD}$ LOW Time	30	ns
t_{LDDWL}	LDAC LOW Time	100	ns
t_{LDDH}	LDAC HIGH Time	150	ns
t_{RSSS}	RESETSEL Valid to RESET HIGH	0	ns
t_{RSSH}	RESET HIGH to RESETSEL Not Valid	100	ns
t_{RSTL}	RESET LOW Time	10	ns
t_{RSTH}	RESET HIGH Time	10	ns
t_S	Settling Time	10	µs

TABLE III. Timing Specifications (T_A = –40°C to +85°C).

Figure 16 shows a DAC7634 in a 4mA to 20mA current output configuration. The output current can be determined by Equation 3:

$$I_{OUT} = \left(\left(\frac{2.5V - 0.5V}{125\Omega}\right) \bullet \left(\frac{N}{65,536}\right)\right) + \left(\frac{0.5V}{125\Omega}\right) \quad (3)$$

At full-scale, the output current is 16mA, plus the 4mA, for the zero current. At zero scale the output current is the offset current of 4mA (0.5V/125Ω).

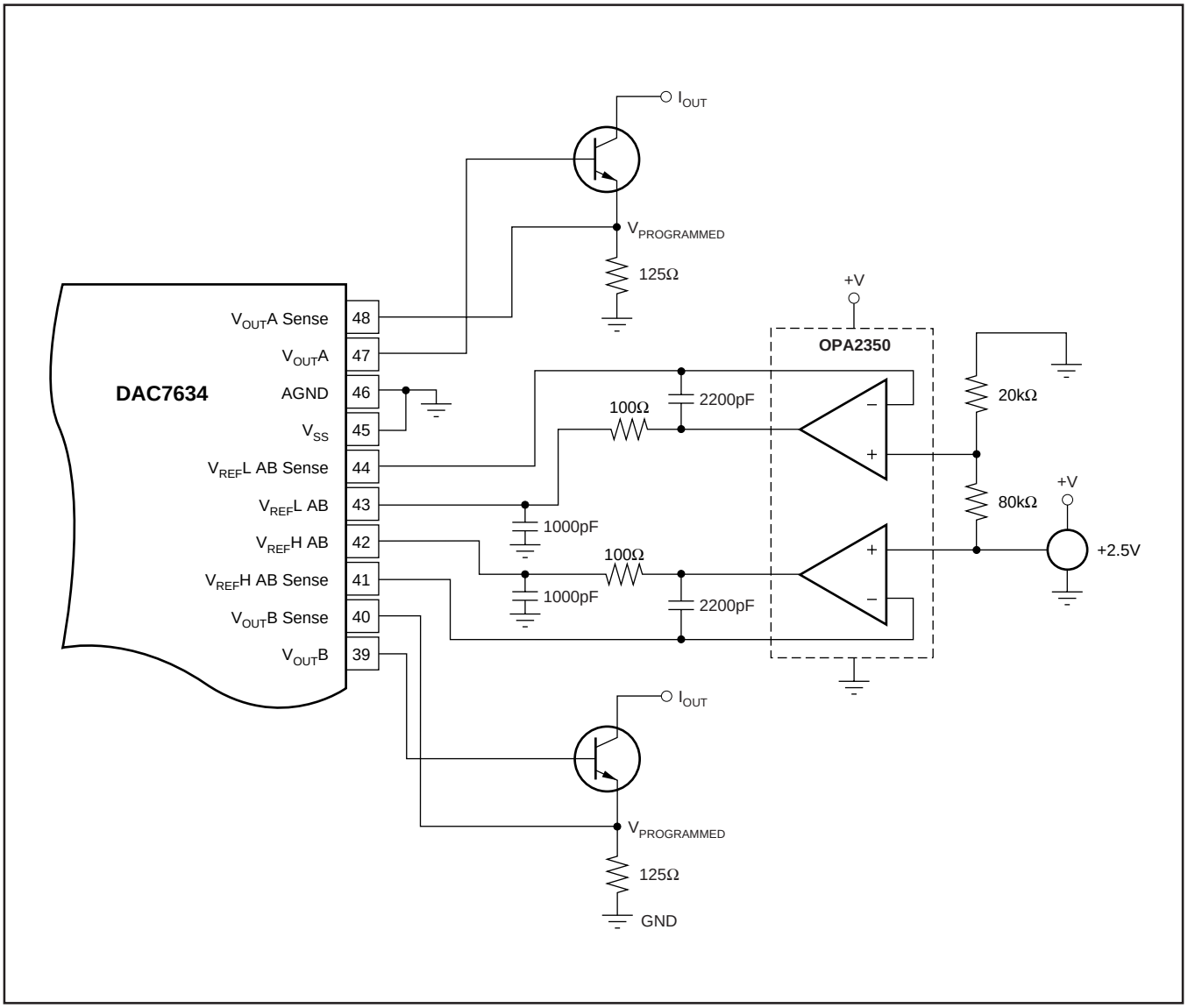


FIGURE 16. 4-to-20mA Digitally Controlled Current Source (1/2 DAC7634).