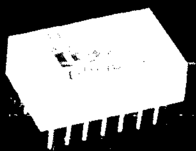
BURR-BROWN®



DIV100

ANALOG DIVIDER

FEATURES

- **HIGH ACCURACY: 0.25% Maximum Error, 40:1 Denominator Range**
- **TWO-QUADRANT OPERATION**
  Dedicated Log-Antilog Technique
- **EASY TO USE**
  Laser-trimmed to Specified Accuracy
  No External Resistors Needed
- **LOW COST**
- **DIP PACKAGE**

APPLICATIONS

- **DIVISION**
- **SQUARE ROOT**
- **RATIOMETRIC MEASUREMENT**
- **PERCENTAGE COMPUTATION**
- **TRANSDUCER AND BRIDGE LINEARIZATION**
- **AUTOMATIC LEVEL AND GAIN CONTROL**
- **VOLTAGE CONTROLLED AMPLIFIERS**
- **ANALOG SIMULATION**

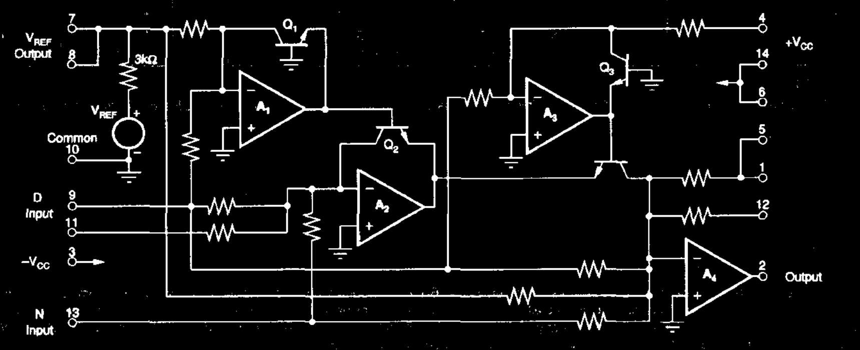
DESCRIPTION

The DIV100 is a precision two-quadrant analog divider offering superior performance over a wide range of denominator input. Its accuracy is nearly two orders of magnitude better than multipliers used for division. It consists of four operational amplifiers and logging transistors integrated into a single monolithic circuit and a laser-trimmed, thin-film resistor network. The electrical characteristics of these devices offer the user guaranteed accuracy without the need for external adjustment — the DIV100 is a complete, single package analog divider.

For those applications requiring higher accuracy than the DIV100 specifies, the capability for optional adjustment is provided. These adjustments allow the user to set scale factor, feedthrough, and output-referred offsets for the lowest total divider error.

The DIV100 also gives the user a precision, temperature-compensated reference voltage for external use.

Designers of industrial process control systems, analytical instruments, or biomedical instrumentation will find the DIV100 easy to use and also a low cost, but highly accurate solution to their analog divider applications.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{CC} = ±15VDC, unless otherwise specified.

PARAMETER	CONDITIONS	DIV100HP MIN	DIV100HP TYP	DIV100HP MAX	DIV100JP MIN	DIV100JP TYP	DIV100JP MAX	DIV100KP MIN	DIV100KP TYP	DIV100KP MAX	UNITS
TRANSFER FUNCTION						V_O = 10N/D					
ACCURACY	R_L ≥ 10kΩ										
Total Error											
Initial	0.25V ≤ D ≤ 10V, N ≤ |D|		0.7	±1.0		0.3	0.5		0.2	0.25	% FSO(1)
vs Temperature	1V ≤ D ≤ 10V, N ≤ |D|		0.02	0.05(2)		*	*		*	*	% FSO/°C
	0.25V ≤ D ≤ 1V, N ≤ |D|		0.06	0.2(2)		*	*		*	*	% FSO/°C
vs Supply	0.25V ≤ D ≤ 10V, N ≤ |D|		0.15			*			*		% FSO/%
Warm-up Time to Rated Performace			5			*			*		Minutes
AC PERFORMANCE	D = +10V										
Small-Signal Bandwidth	–3dB		350			*			*		kHz
0.5% Amplitude Error	Small-Signal		15			*			*		kHz
0.57° Vector Error	Small-Signal		1000			*			*		Hz
Full-Power Bandwidth	V_O = ±10V, I_O = ±5mA		30			*			*		kHz
Slew Rate	V_O = ±10V, I_O = ±5mA		2			*			*		V/µs
Settling Time	ε = 1%, ΔV_O = 20V		15			*			*		µs
Overload Recovery	50% Output Overload		4			*			*		µs
INPUT CHARACTERISTICS											
Input Voltage Range											
Numerator	N ≤ |D|	±10			*			*			V
Denominatior	D ≥ +250mV	±10			*			*			V
Input Resistance	Either Input		25			*			*		kΩ
OUTPUT CHARACTERISTICS											
Full-Scale Output		±10			*			*			V
Rated Output											
Voltage	I_O = ±5mA	±10			*			*			V
Current	V_O = ±10V	±5			*			*			mA
Current Limit											
Positive			15	20(2)		*			*		mA
Negative			19	23(2)		*			*		mA
OUTPUT NOISE VOLTAGE	N = 0V										
f_B = 10Hz to 10kHz											
D = +10V			370			*			*		µVrms
D = +250mV			1			*			*		mVrms
REFERENCE VOLTAGE CHARACTERISTICS, R_L ≥ 10MΩ											
Output Voltage											
Initial	At 25°C	6.5(2)	6.8	7.1(2)	*	*	*	*	*	*	V
vs Supply			±25			*			*		µV/V
Temperature Coefficient			±50			*			*		ppm/°C
Output Resistance			3			*			*		kΩ
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			*			*		VDC
Operating Range	Derated Performance	±12		±20	*		*	*		*	VDC
Quiescent Current											
Postive Supply			5	7(2)		*	*		*	*	mA
Negative Supply			8	10(2)		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		0		+70	*		*	*		*	°C
Operating Temperature	Derated Performance	–25		+85	*		*	*		*	°C
Storage		–40		+85	*		*	*		*	°C

*Same as DIV100HP.

NOTES: (1) FSO is the abbreviation for Full Scale Output. (2) This parameter is untested and is not guaranteed. This specifcation is established to a 90% confidence level.

PIN CONFIGURATION

Bottom View — DIP

$+V_{CC}$	14	1	Gain Error Adjust
Numerator (N) Input	13	2	Output
Output Offset Adjust	12	3	$-V_{CC}$
N Input Offset Adjust	11	4	D Input Offset Adjust
Common	10	5	Internally Connected to Pin 1
Denominator (D) Input	9	6	Internally Connected to Pin 14
Refererence Voltage	8	7	Internally Connected to Pin 8

ABSOLUTE MAXIMUM RATINGS

Supply .... ±20VDC
Internal Power Dissipation(1) 600mW
Input Voltage Range(2) .... ±20VDC
Storage Temperature Range .... –40°C to +85°C
Operating Temperature Range .... –25°C to 85°C
Lead Temperature (soldering, 10s) .... +300°C
Output Short-Circuit Duration(1, 3) .... Continuous
Junction Temperature .... +175°C

NOTES: (1) See General Information section for discussion. (2) For supply voltages less than ±20VDC, the absolute maximum input voltage is equal to the supply voltage. (3) Short-circuit may be to ground only. Rating applies to an ambient temperature of +38°C at rated supply voltage.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	TOTAL INITIAL ERROR (% FSO)
DIV100HP	0°C to +70°C	1.0
DIV100JP	0°C to +70°C	0.5
DIV100KP	0°C to +70°C	0.25

PACKAGE INFORMATION(1)

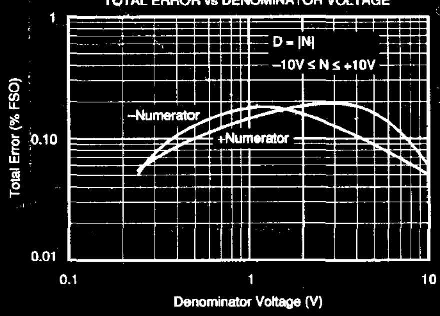
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DIV100HP	14-Pin DIP	105
DIV100JP	14-Pin DIP	105
DIV100KP	14-Pin DIP	105

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

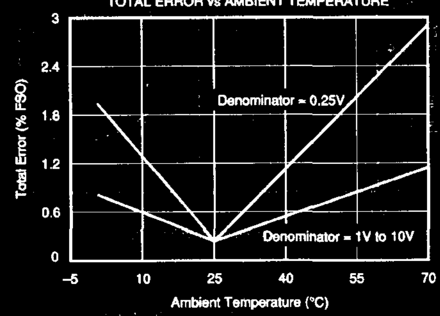
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC, unless otherwise specified.

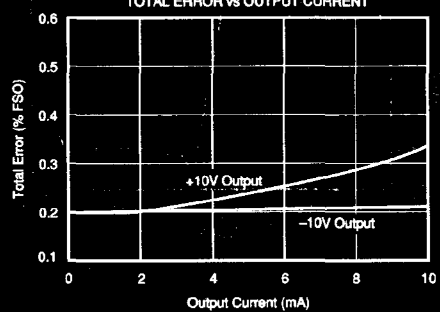
TOTAL ERROR vs DENOMINATOR VOLTAGE



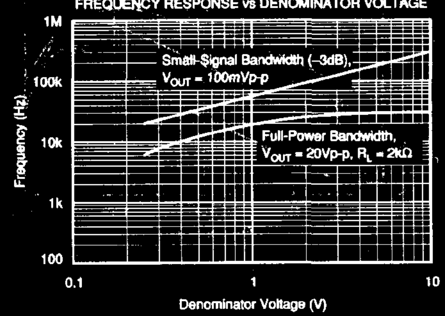
TOTAL ERROR vs AMBIENT TEMPERATURE



TOTAL ERROR vs OUTPUT CURRENT



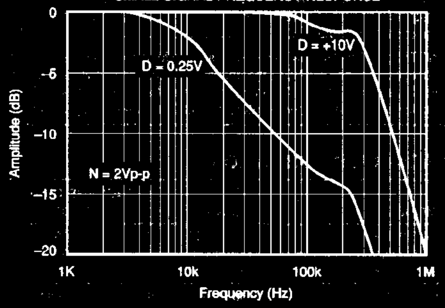
FREQUENCY RESPONSE vs DENOMINATOR VOLTAGE



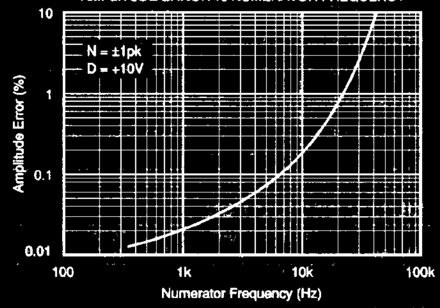
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC, unless otherwise specified.

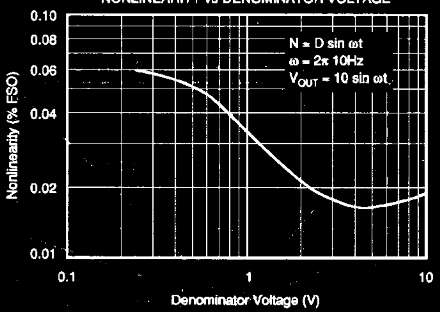
SMALL-SIGNAL FREQUENCY RESPONSE



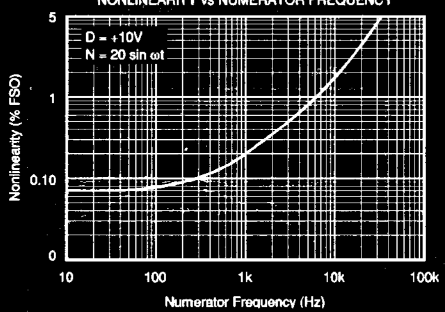
AMPLITUDE ERROR vs NUMERATOR FREQUENCY



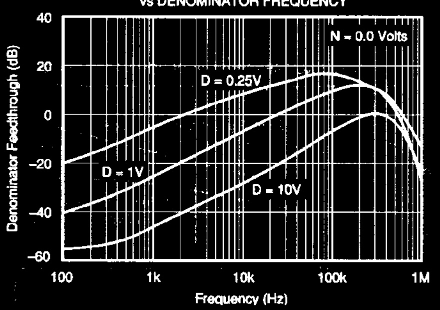
NONLINEARITY vs DENOMINATOR VOLTAGE



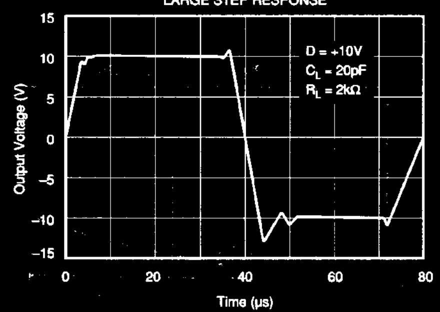
NONLINEARITY vs NUMERATOR FREQUENCY



DENOMINATOR FEEDTHROUGH vs DENOMINATOR FREQUENCY



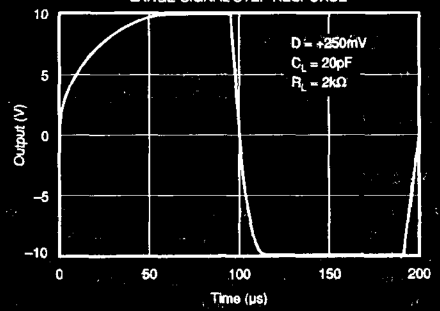
LARGE STEP RESPONSE



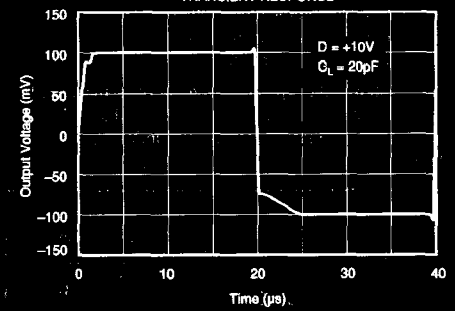
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15VDC, unless otherwise specified.

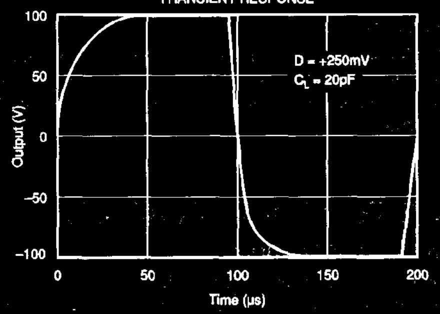
LARGE SIGNAL STEP RESPONSE



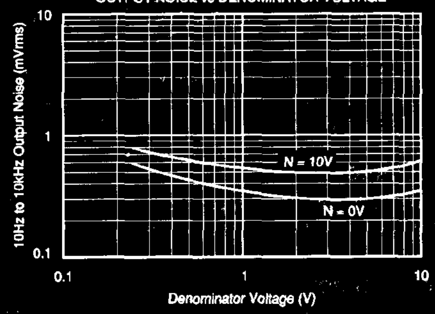
TRANSIENT RESPONSE



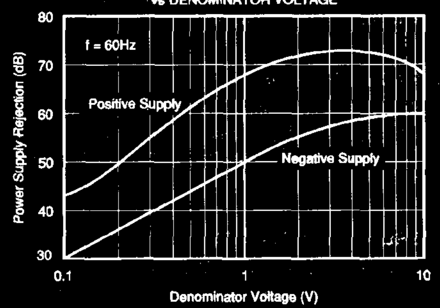
TRANSIENT RESPONSE



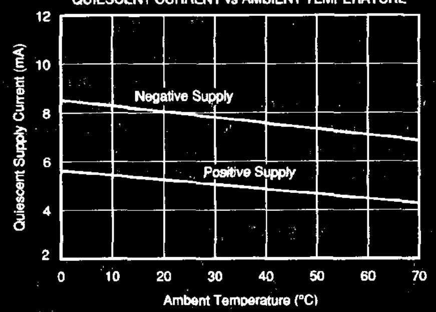
OUTPUT NOISE vs DENOMINATOR VOLTAGE



POWER SUPPLY REJECTION vs DENOMINATOR VOLTAGE



QUIESCENT CURRENT vs AMBIENT TEMPERATURE



DEFINITIONS

TRANSFER FUNCTION

The ideal transfer function for the DIV100 is:

$$V_{OUT} = 10N/D$$

where: N = Numerator input voltage
D = Denominator input voltage
10 = Internal scale factor

Figure 1 shows the operating region over the specified numerator and denominator ranges. Note that below the minimum denominator voltage (250mV) operation is undefined.

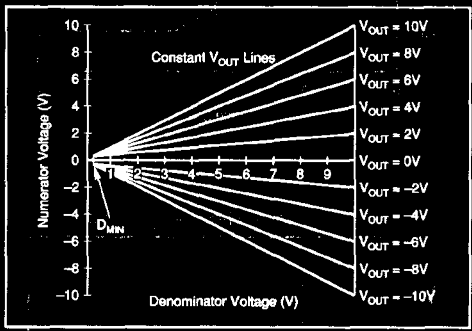


FIGURE 1. Operating Region.

ACCURACY

Accuracy is specified as a percentage of full-scale output (FSO). It is derived from the total error specification.

TOTAL ERROR

Total error is the deviation of the actual output from the ideal quotient 10N/D expressed in percent of FSO (10V); e.g., for the DIV100K:

$$V_{OUT\,(ACTUAL)} = V_{OUT\,(IDEAL)} \pm \text{total error},$$

where: Total error = 0.25%, FSO = 25mV.

It represents the sum of all error terms normally associated with a divider: numerator nonlinearity, denominator nonlinearity, scale-factor error, output-referred numerator and denominator offsets, and the offset due to the output amplifier. Individual errors are not specified because it is their sum that affects the user's application.

SMALL-SIGNAL BANDWIDTH

Small-signal bandwidth is the frequency the output drops to 70% (–3dB) of its DC value. The input signal must be low enough in amplitude to keep the divider's output from becoming slew-rate limited. A rule-of-thumb is to make the output voltage 100mVp-p, when testing this parameter. Small-signal bandwidth is directly proportional to denominator magnitude as described in the Typical Performance Curves.

0.5% AMPLITUDE ERROR

At high frequencies the input-to-output relationship is a complex function that produces both a magnitude and vector error. The 0.5% amplitude error is the frequency at which the magnitude of the output drops 0.5% from its DC value.

0.57° VECTOR ERROR

The 0.57° vector error is the frequency at which a phase error of 0.01 radians occurs. This is the most sensitive measure of dynamic error of a divider.

LINEARITY

Defining linearity for a nonlinear device may seem unnecessary; however, by keeping one input constant the output becomes a linear function of the remaining input. The denominator is the input that is held fixed with a divider. Nonlinearities in a divider add harmonic distortion to the output in the amount of:

$$\text{Percent Distortion} \approx \frac{\text{Percent Nonlinearity}}{\sqrt{2}}$$

FEEDTHROUGH

Feedthrough is the signal at the output for any value of denominator within its rated range, when the numerator input is zero. Ideally, the output should be zero under this condition.

GENERAL INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10µF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins to the power supply common. The connection of these capacitors should be as close to the DIV100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 1000pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the DIV100's output.

OVERLOAD PROTECTION

The DIV100 can be protected against accidental power supply reversal by putting a diode (1N4001 type) in series with each power supply line as shown in Figure 2. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off.

If this protection circuit is used, the accuracy of the DIV100 will be degraded by the power supply sensitivity specifica-

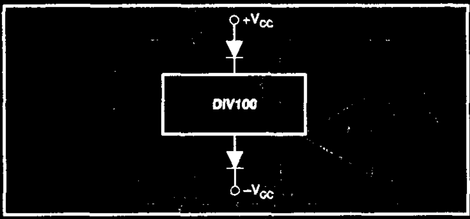


FIGURE 2. Overload Protection Circuit.

tion. No other overload protection circuit is necessary. Inputs are internally protected against overvoltages and they are current-limited by at least a 10kΩ series resistor. The output is protected against short circuits to power supply common only.

STATIC SENSITIVITY

No special handling is required. The DIV100 does not use MOS-type transistors. Furthermore, all external leads are protected by resistors against low energy electrostatic discharge (ESD).

INTERNAL POWER DISSIPATION

Figure 3 is the thermal model for the DIV100 where:

P_{DQ} = Quiescent power dissipation
 $= |+V_{CC}|\ I_{+QUIESCENT} + |-V_{CC}|\ I_{-QUIESCENT}$

P_{DX} = Worst case power dissipation in the output transistor
 $= V_{CC}^2/4R_{LOAD}$ (for normal operation)
 $= V_{CC}\ I_{OUTPUT\ LIMIT}$ (for short-circuit)

T_J = Junction temperature (output loaded)
T_J^* = Junction temperature (no load)
T_C = Case temperature
T_A = Ambient temperature
θ = Thermal resistance

This model is a multiple power source model to provide a more accurate simulation.

The model in Figure 3 must be used in conjunction with the DIV100's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

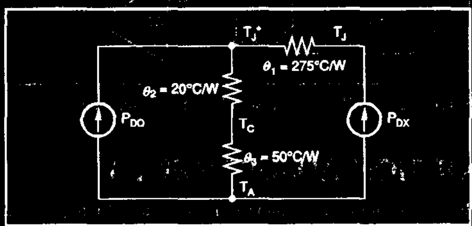


FIGURE 3. DIV100 Thermal Model.

As an example of how to use this model, consider this problem:

Determine the highest ambient temperature at which the DIV100 may be operated with a continuous short circuit to ground. V_{CC} = ±15VDC.

$P_{D(MAX)}$ = 600mW. $T_{J(MAX)}$ = +175°C.

$T_A = T_{J(MAX)} - P_{DQ}\ (\theta_2 + \theta_3) - P_{DX(SHORT-CIRCUIT)}\ (\theta_1 + \theta_2 + \theta_3)$
 = 175°C – 18°C – 119°C = 38°C

$P_{D(ACTUAL)} = P_{DQ} + P_{DX(SHORT-CIRCUIT)} \leq P_{D(MAX)}$
 = 255mW + 345mW = 600mW

The conclusion is that the device will withstand a short-circuit up to T_A = +38°C without exceeding either the 175°C or 600mW absolute maximum limits.

LIMITING OUTPUT VOLTAGE SWING

The negative output voltage swing should be limited to ±11V, maximum, to prevent polarity inversion and possible system instability. This should be done by limiting the input voltage range.

THEORY OF OPERATION

The DIV100 is a log-antilog divider consisting of four operational amplifiers and four logging transistors integrated into a single monolithic circuit. Its basic principal of operation can be seen by an analysis of the circuit in Figure 4.

The logarithmic equation for a bipolar transistor is:

$$V_{BE} = V_T\ \ell n\ (I_C/I_S), \quad (1)$$

where: $V_T = kT/q$
 k = Boltzmann's constant = 1.381×10^{-23}
 T = Absolute temperature in degrees Kelvin
 q = Electron charge = 1.602×10^{-19}
 I_C = Collector current
 I_S = Reverse saturation current

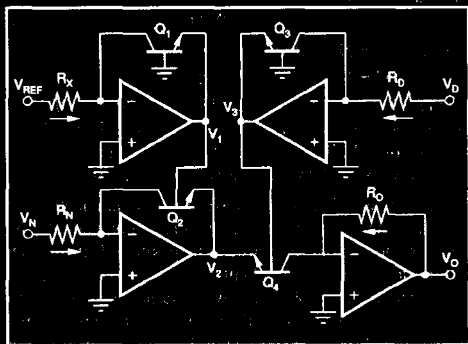


FIGURE. 4 One-Quadrant Log-Antilog Divider.

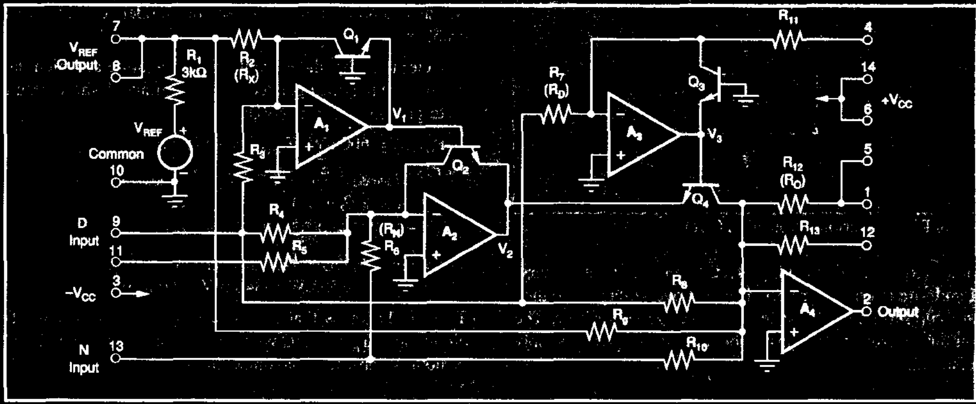


FIGURE 5. DIV100 Two-Quadrant Log-Antilog Circuit.

Applying equation (1) to the four logging transistors gives:

For Q_1:

$$V_{BE} = V_B - V_E = V_T[\ell n(V_{REF}/R_X - \ell n\, I_S]$$

This leads to:

$$V_1 = -V_T[\ell n(V_{REF}/R_X - \ell n\, I_S]$$

For Q_2:

$$V_1 - V_2 = V_T[\ell n(V_N/R_N) - \ell n\, I_S]$$

For Q_3:

$$V_3 = -V_T[\ell n\,(V_D/R_D) - \ell n\, I_S].$$

We have now taken the logarithms of the input voltage V_{REF}, V_N, and V_D. Applying equation (1) to Q_4 gives:

$$V_3 - V_2 = V_T\,[\ell n\,(V_O/R_O) - \ell n\, I_S].$$

Assume V_T and I_S are the same for all four transistors (a reasonable assumption with a monolithic IC). Solving this last equation in terms of the previously defined variables and taking the antilogarithm of the result yields:

$$V_O = \frac{V_{REF}\, V_N\, R_O\, R_D}{V_D\, R_X\, R_N} \qquad (2)$$

In the DIV100 V_{REF} = 6.6V, $R_O = R_N = R_D$, and R_X is such that the transfer function is:

$$V_O = 10N/D \qquad (3)$$

where: N = Numerator Voltage
D = Denominator Voltage

Figure 5 is a more detailed circuit diagram for the DIV100. In addition to the circuitry included in Figure 3, it also shows the resistors (R_3, R_4, R_8, R_9, and R_{10}) used for level-shifting. This converts the DIV100 to a two-quadrant divider.

The implementation of the transfer function in equation (3) is done using devices with real limitations. For example, the value of the D input must always be positive. If it isn't, Q_3 will no longer conduct, A_3 will become open loop, and its output and the DIV100 output will saturate. This limitation is further restricted in that if the D input is less than +250mV the errors will become substantial. It will still function, but its accuracy will be less.

Still another limitation is that the value of the N input must always be equal to or less than the absolute value of the D input. From equation (3) it can be seen that if this limitation is not met, V_O will try to be greater than the 10V output voltage limit of A_4.

A limitation that may not be obvious is the effect of source resistance. If the numerator or denominator inputs are driven from a source with more than 10Ω of output resistance, the resultant voltage divider will cause a significant output error. This voltage divider is formed by the source resistance and the DIV100 input resistance. With R_{SOURCE} = 10Ω and $R_{INPUT\,(DIV100)}$ = 25kΩ an error of 0.04% results. This means that the best performance of the DIV100 is obtained by driving its inputs from operational amplifiers.

Note that the reference voltage is brought out to pins 7 and 8. This gives the user a precision, temperature-compensated reference for external use. Its open-circuit voltage is +6.8VDC, typically. Its Thevenin equivalent resistance is 3kΩ. Since the output resistance is a relatively high value, an operational amplifier is necessary to buffer this source as shown in Figure 6. The external amplifier is necessary because current drawn through the 3kΩ resistor will effect the DIV100 scale factor.

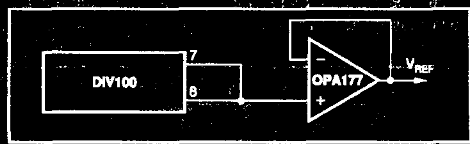


FIGURE 6. Buffered Precision Voltage Reference.

OPTION ADJUSTMENTS

Figure 7 shows the connections to make to adjust the DIV100 for significantly better accuracy over its 40-to-1 denominator range.

The adjustment procedure is:

1. Begin with R_1, R_2 and R_3 set to their mid-position.
2. With |N| = D = 10.000V, ±1mV, adjust R_1 for V_O = +10.000V, ±1mV. This sets the scale factor.
3. Set D to the minimum expected denominator voltage. With N = –D, adjust R_2 for V_O = –10.000V. This adjusts the output referred denominator offset errors.
4. With D still at its minimum expected value, make N = D. Adjust R_3 for V_O = 10.000V. This adjusts the output referred offset errors.
5. Repeat steps 2-4 until the best accuracy is obtained.

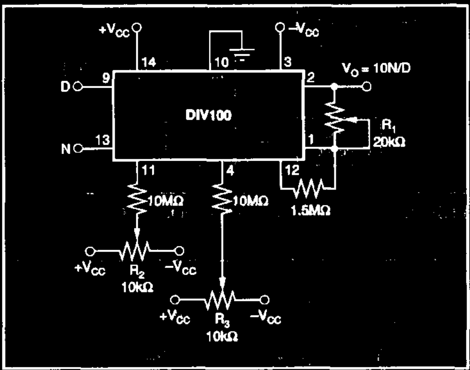


FIGURE 7. Connection Diagram for Optional Adjustments.

TYPICAL APPLICATIONS

CONNECTION DIAGRAM

Figure 8 is applicable to each application discussed in this section, except the square root mode.

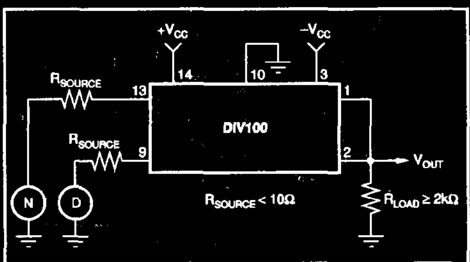


FIGURE 8. Connection Diagram—Divide Mode.

RATIOMETRIC MEASUREMENT

The DIV100 is useful for ratiometric measurements such as efficiency, elasticity, stress, strain, percent distortion, impedance magnitude, and fractional loss or gain. These ratios may be made for instantaneous, average, RMS, or peak values.

The advantage of using the DIV100 can be illustrated from the example shown in Figure 9.

The LVDT (Linear Variable Differential Transformer) weigh cell measures the force exerted on it by the weight of the material in the container. Its output is a voltage proportional to:

$$W = \frac{Fg}{a}$$

where: W = Weight of material
F = Force
g = Acceleration due to gravity
a = Acceleration (acting on body of weight W)

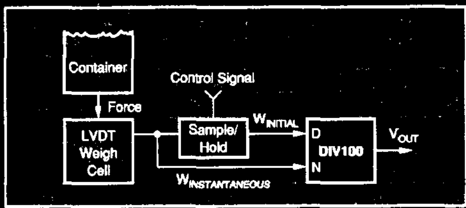


FIGURE 9. Weighing System - Fractional Loss.

In a fractional loss weighting system, the initial value of the material can be determined by the volume of the container and the density of the material. If this value is then held on the D-input to the DIV100 for some time interval, the DIV100 output will be a measure of the instantaneous fractional loss:

Loss (L) = $W_{INSTANTANEOUS}/W_{INITIAL}$

Note that by using the DIV100 in this application the common physical parameters of g and a have been eliminated from the measurement, thus eliminating the need for precise system calibration.

The output from a ratiometric measuring system may also be used as a feedback signal in an adaptive process control system. A common application in the chemical industry is in the ratio control of a gas and liquid flow as illustrated in Figure 10.

PERCENTAGE COMPUTATION

A variation of the direct ratiometric measurements previously discussed is the need for percentage computation. In Figure 11, the DIV100 output varies as the percent deviation of the measured variable to the standard.

TIME AVERAGING

The circuit in Figure 12 overcomes the fixed averaging interval and crude approximation of more conventional time averaging schemes.

BRIDGE LINEARIZATION

The bridge circuit in Figure 13 is fundamental to pressure, force, strain and electrical measurements. It can have one or

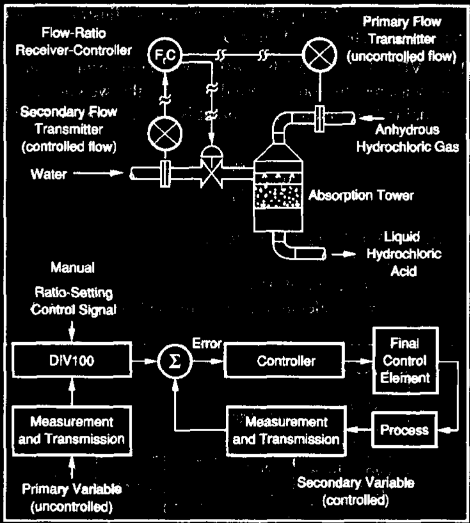


FIGURE 10. Ratio Control of Water to Hydrochloric Gas.

more active arms whose resistance is a function of the physical quantity, property, or condition that is being measured; e.g., force of compression. For the sake of explanation, the bridge in Figure 13 has only one active arm.

The differential output voltage V_{BA} is:

$$V_{BA} = V_B - V_A \frac{-V_{EX}\delta}{2(2+\delta)}$$

a nonlinear function of the resistance change in the active arm. This nonlinearity limits the useful span of the bridge to perhaps ±10% variation in the measured parameter.

Bridge linearization is accomplished using the circuit in Figure 14. The instrumentation amplifier converts the differential output to a single-ended voltage needed to drive the divider. The voltage-divider string makes the numerator and denominator voltages:

$$N = \frac{-V_{EX}\delta R_{IN}}{(2R_1 + 3R_{IN})(2+\delta)}\text{; and,}$$

$$D = \frac{2V_{EX}R_{ID}}{(2R_1 + 3R_{ID})(2+\delta)}\text{, respectively,}$$

where: R_{IN} = DIV100 numerator input resistance
R_{ID} = DIV100 denominator input resistance

Applying these voltages to the DIV100 transfer function gives:

$$V_O = 10N/D = \frac{(2R_1 + 3R_{ID})(R_{IN}\delta)\,10}{(2R_1 + 3R_{IN})(2R_{ID})},$$

which reduces to:

$$V_O = -5\delta$$

if the divider's input resistances are equal.

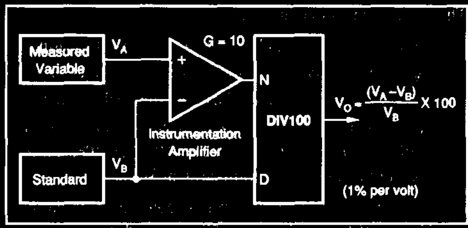


FIGURE 11. Percentage Computation.

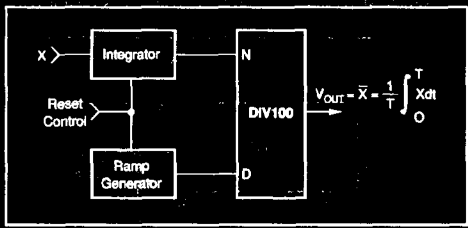


FIGURE 12. Time Averaging Computation Circuit.

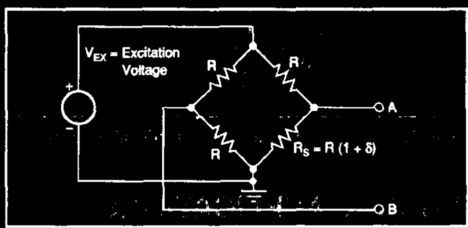


FIGURE 13. Bridge Circuit.

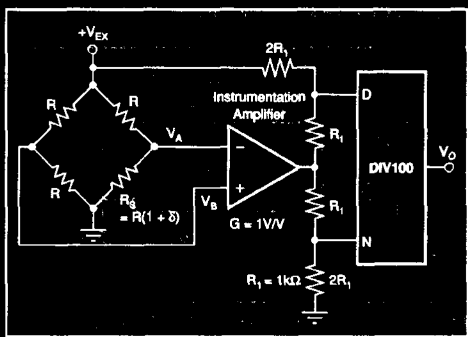


FIGURE 14. Bridge Linearization Circuit.

The nonlinearity of the bridge has been eliminated and the circuit output is independent of variations in the excitation voltage.

AUTOMATIC GAIN CONTROL

A simple AGC circuit using the DIV100 is shown in Figure 15. The numerator voltage may vary both positive and negative. The divider's output is half-wave rectified and filtered by D_1, R_3, and C_2. It is then compared to the DC reference voltage. If a difference exists, the integrator sends a control signal to the denominator input to maintain a constant output, thus compensating for input voltage changes.

VOLTAGE-CONTROLLED FILTER

Figure 16 shows how to use the DIV100 in the feedback loop of an integrator to form a voltage-controlled filter. The transfer function is:

$$\frac{V_{OUT}(S)}{V_{IN}(S)} = \frac{K}{\tau S + 1}$$

where: $K = -R_2/R_1$

$$\tau = \frac{10\,R_2\,C}{V_{CONTROL}}$$

This circuit may be used as a single-pole low-pass active filter whose cutoff frequency is linearily proportional to the circuit's control voltage.

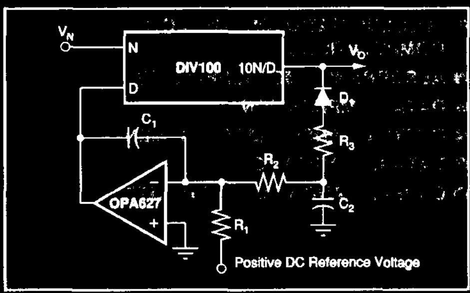


FIGURE 15. Automatic Gain Control Circuit.

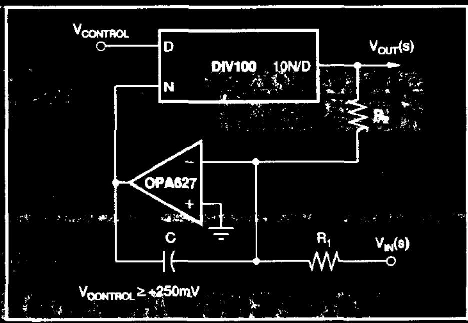


FIGURE 16. Voltage-Controlled Filter.

SQUARE ROOT

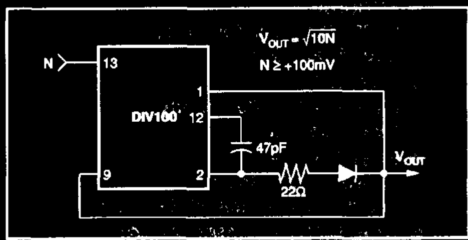


FIGURE 17. Connection Diagram for Square Root Mode.