DM2502,DM2503,DM2504

DM2502 DM2503 DM2504 Successive Approximation Registers

TEXAS INSTRUMENTS

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DM2502, DM2503, DM2504 Successive Approximation Registers

General Description

The DM2502, DM2503 and DM2504 are 8-bit and 12-bit TTL registers designed for use in successive approximation A/D converters. These devices contain all the logic and control circuits necessary in combination with a D/A converter to perform successive approximation analog-to-digital conversions.

The DM2502 has 8 bits with serial capability and is not expandable. The DM2503 has 8 bits and is expandable without serial capability. The DM2504 has 12 bits with serial capability and expandability.
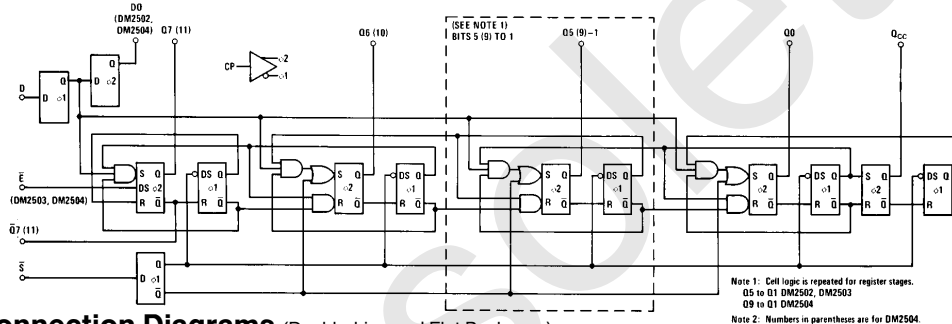
All three devices are available in ceramic DIP, ceramic flat-pak, and molded Epoxy-B DIPs. The DM2502, DM2503 and

DM2504 operate over −55°C to +125°C; the DM2502C, DM2503C and DM2504C operate over 0°C to +70°C.
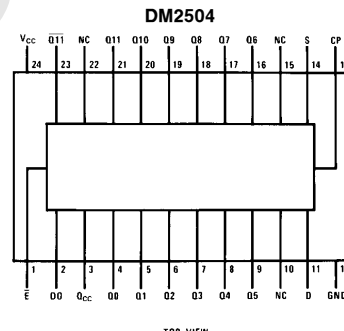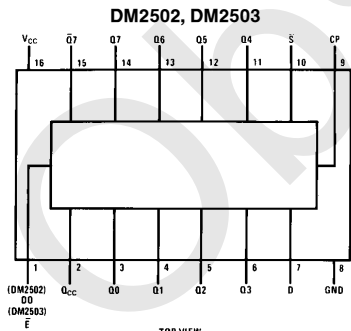
Features

- Complete logic for successive approximation A/D converters
- 8-bit and 12-bit registers
- Capable of short cycle or expanded operation
- Continuous or start-stop operation
- Compatible with D/A converters using any logic code
- Active low or active high logic outputs
- Use as general purpose serial-to-parallel converter or ring counter

Logic Diagram

Note 1: Cell logic is repeated for register stages.
Q5 to Q1 DM2502, DM2503
Q9 to Q1 DM2504

Note 2: Numbers in parentheses are for DM2504.

Connection Diagrams (Dual-In-Line and Flat Packages)

DM2502, DM2503

TOP VIEW

Order Number DM2502J, DM2502CJ, DM2503J or DM2503CJ
See NS Package J16A
Order Number DM2502CN or DM2503CN
See NS Package N16A
Order Number DM2502W, DM2502CW, DM2503W, or DM2503CW
See NS Package W16A

DM2504

TOP VIEW

Order Number DM2504F or DM2504CJ
See NS Package F24D
Order Number DM2504J or DM2504CJ
See NS Package J24A
Order Number DM2504CN
See NS Package N24A

TL/F/5702–1

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DM2502C, DM2503C, DM2504C	4.75	5.25	V
DM2502, DM2503, DM2504	4.5	5.5	V
Temperature, T_A			
DM2502C, DM2503C, DM2504C	0	+70	°C
DM2502, DM2503 DM2504	−55	+125	°C

Electrical Characteristics (Notes 2 and 3) $V_{CC} = 5.0V$, $T_A = 25°C$, $C_L = 15$ pF, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Logical "1" Input Voltage (V_{IH})	$V_{CC} = $ Min	2.0			V
Logical "1" Input Current (I_{IH}) CP Input D, $\overline{E}$, $\overline{S}$ Inputs All Inputs	$V_{CC} = $ Max $V_{IH} = 2.4V$ $V_{IH} = 2.4V$ $V_{IH} = 5.5V$		6 6	40 80 1.0	µA µA mA
Logical "0" Input Voltage (V_{IL})	$V_{CC} = $ Min			0.8	V
Logical "0" Input Current (I_{IL}) CP, $\overline{S}$ Inputs D, E Inputs	$V_{CC} = $ Max $V_{IL} = 0.4V$ $V_{IL} = 0.4V$		−1.0 −1.0	−1.6 −3.2	mA mA
Logical "1" Output Voltage (V_{OH})	$V_{CC} = $ Min, $I_{OH} = 0.48$ mA	2.4	3.6		V
Output Short Circuit Current (Note 4) (I_{OS})	$V_{CC} = $ Max; $V_{OUT} = 0.0V$; Output High; CP, D, $\overline{S}$, High; $\overline{E}$ Low	−10	−20	−45	mA
Logical "0" Output Voltage (V_{OL})	$V_{CC} = $ Min, $I_{OL} = 9.6$ mA		0.2	0.4	V
Supply Current (I_{CC}) DM2502C DM2502 DM2503C DM2503 DM2504C DM2504	$V_{CC} = $ Max, All Outputs Low		65 65 60 60 90 90	95 85 90 80 124 110	mA mA mA mA mA mA
Propagation Delay to a Logical "0" From CP to Any Output (t_{pd0})		10	18	28	ns
Propagation Delay to a Logical "0" From $\overline{E}$ to Q7 (Q11) Output (t_{pd0})	CP High, $\overline{S}$ Low DM2503, DM2503C, DM2504, DM2504C Only		16	24	ns
Propagation Delay to a Logical "1" From CP to Any Output (t_{pd1})		10	26	38	ns
Propagation Delay to a Logical "1" From $\overline{E}$ to Q7 (Q11) Output (t_{pd1})	CP High, $\overline{S}$ Low DM2503, DM2503C, DM2504, DM2504C Only		13	19	ns
Set-Up Time Data Input ($t_{s(D)}$)		−10	4	8	ns
Set-Up Time Start Input ($t_{s(\overline{S})}$)		0	9	16	ns
Minimum Low CP Width (t_{PWL})			30	42	ns
Minimum High CP Width (t_{PWH})			17	24	ns
Maximum Clock Frequency (f_{MAX})		15	21		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM2502, DM2503 and DM2504, and across the 0°C to +70°C range for the DM2502C, DM2503C and DM2504C. All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25°C$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Application Information

OPERATION

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the DM2502 and DM2504 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7 (11) low, and all the remaining register outputs high. The Q_{CC} (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ signal must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7 (11) register bit and the Q6 (10) register bit is set to a low ready for the next clock cycle. On the next clock low-to-high transition data enters the Q6 (10) register bit and Q5 (9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the Q_{CC} signal goes low, and the register is inhibited from further change until reset by a Start signal.

The DM2502, DM2503 and DM2504 have a specially tailored two-phase clock generator to provide nonoverlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates they drive). Thus, even at very slow dV/dt rates at the clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

LOGIC CODES

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator ½ full range + ½ LSB and using the complement of the MSB ($\overline{Q7}$ or $\overline{Q11}$) with a binary D/A converter. Offset binary is used in the same manner but with the MSB ($\overline{Q7}$ or $\overline{Q11}$). BCD D/A converters can be used with the addition of illegal code suppression logic.

### ACTIVE HIGH OR ACTIVE LOW LOGIC

The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

EXPANDED OPERATION

An active low enable input, $\overline{E}$, on the DM2503 and DM2504 allows registers to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs in parallel and connecting the Q_{CC} output of one register to the $\overline{E}$ input of the next less significant register. When the start resets the register, the $\overline{E}$ signal goes high, forcing the Q7 (11) bit high and inhibiting the register from accepting data until the previous register is full and its Q_{CC} goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

Timing Diagram

DM2502, DM2503

TL/F/5702–2

3
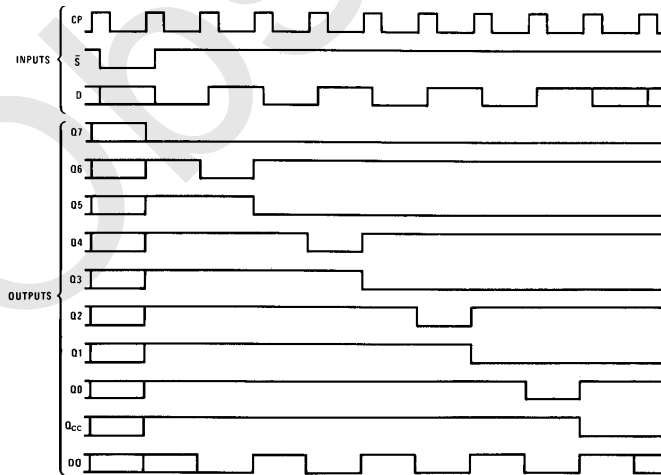
Application Information (Continued)

SHORT CYCLE

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather then the Q_{CC} signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of Q_{CC} and the appropriate register output.

COMPARATOR BIAS

To minimize the digital error below $\pm \frac{1}{2}$ LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased $+\frac{1}{2}$ LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased $-\frac{1}{2}$ LSB.

Definition of Terms

CP: The clock input of the register.

D: The serial data input of the register.

DO: The serial data out. (The D input delayed one bit).

$\overline{E}$: The register enable. This input is used to expand the length of the register and when high forces the Q7 (11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).

Q_i i = 7 (11) to 0: The outputs of the register.

Q_{CC}: The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.

Q7 (11): The true output of the MSB of the register.

$\overline{Q7}$ (11): The complement output of the MSB of the register.

$\overline{S}$: The start input. If the start input is held low for at least a clock period the register will be reset to Q7 (11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

Truth Table

DM2502, DM2503

Time	Inputs			Outputs[1]									
t_n	D	$\overline{S}$	$\overline{E}$[2]	DO[3]	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q_{CC}
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	L	X	L	H	H	H	H	H	H	H	H
2	D6	H	L	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	L	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	L	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	L	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	L	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	L	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	L	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	L	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	L	X	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

Note 1: Truth table for DM2504 is extended to include 12 outputs.

Note 2: Truth table for DM2502 does not include $\overline{E}$ column or last line in truth table shown.

Note 3: Truth table for DM2503 does not include D0 column.
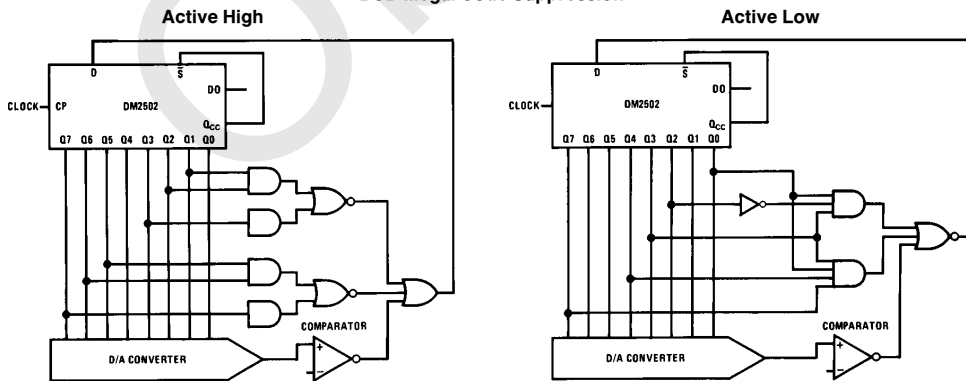
H = High Voltage Level
L = Low Voltage Level
X = Don't Care
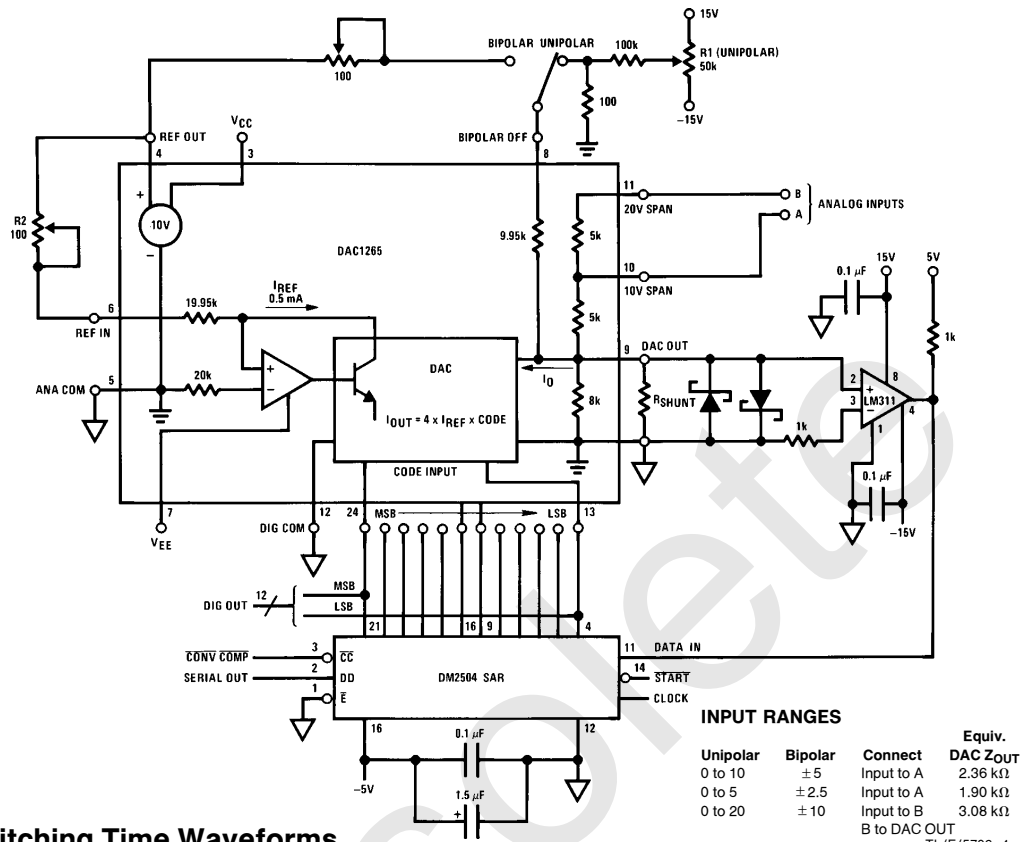NC = No Change

Typical Applications
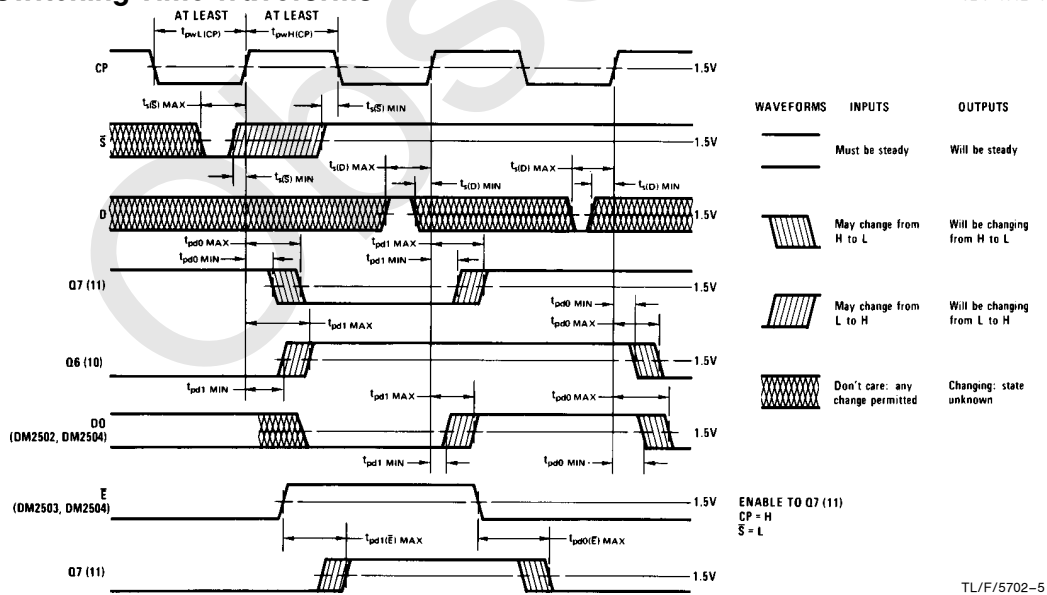
BCD Illegal Code Suppression

Active High

Active Low

TL/F/5702–3

4

Typical Applications (Continued)

Fast Precision Analog-to-Digital Converter

BIPOLAR UNIPOLAR

R1 (UNIPOLAR) 50k

15V
−15V

100

100k

100

REF OUT 4 V_{CC} 3

BIPOLAR OFF 8

11   B   ANALOG INPUTS
20V SPAN

R2 100

10V

DAC1265

9.95k   5k   10   A
10V SPAN

5k

6   REF IN   19.95k I_{REF} 0.5 mA

0.1 µF   15V   5V

ANA COM 5   20k

DAC

$I_{OUT} = 4 \times I_{REF} \times CODE$

I_0 9 DAC OUT

8k R_{SHUNT}

2   LM311   8
3   4
1

1k

1k

0.1 µF
−15V

CODE INPUT

7   12   24 MSB   LSB 13
V_{EE} DIG COM

DIG OUT   12   MSB
LSB

21   16 9   4

CONV COMP   3   CC
SERIAL OUT 2   DD   DM2504 SAR   11 DATA IN
1   E   14 START
CLOCK

16   0.1 µF   12

−5V

1.5 µF

INPUT RANGES

Unipolar	Bipolar	Connect	Equiv. DAC Z_{OUT}
0 to 10	±5	Input to A	2.36 kΩ
0 to 5	±2.5	Input to A	1.90 kΩ
0 to 20	±10	Input to B	3.08 kΩ
		B to DAC OUT	

TL/F/5702–4

Switching Time Waveforms

AT LEAST $t_{pwL(CP)}$ AT LEAST $t_{pwH(CP)}$

CP   1.5V

$t_{s(S)}$ MAX $t_{s(S)}$ MIN

$\overline{S}$ 1.5V

$t_{s(S)}$ MIN $t_{s(D)}$ MAX $t_{s(D)}$ MAX $t_{s(D)}$ MIN $t_{s(D)}$ MIN

D   1.5V

t_{pd0} MAX t_{pd1} MAX
t_{pd0} MIN t_{pd1} MIN

Q7 (11)   1.5V

t_{pd0} MIN
t_{pd0} MAX

t_{pd1} MAX

Q6 (10)   1.5V

t_{pd1} MIN t_{pd1} MAX t_{pd0} MAX

D0 (DM2502, DM2504)   1.5V

t_{pd1} MIN t_{pd0} MIN

$\overline{E}$ (DM2503, DM2504)   1.5V

$t_{pd1(\overline{E})}$ MAX $t_{pd0(\overline{E})}$ MAX

Q7 (11)   1.5V

WAVEFORMS	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care: any change permitted	Changing: state unknown

ENABLE TO Q7 (11)
CP = H
$\overline{S}$ = L

TL/F/5702–5

5

Physical Dimensions inches (millimeters)

0.620
(15.75)
MAX

0.090
(2.286)
MAX

0.050 ± 0.005
(1.270 ± 0.127)

0.010 − 0.040
(0.254 − 1.016)

0.045
(1.143)
MAX

0.030
(0.762)
MIN

0.250 − 0.350
(6.350 − 8.890)

0.180
(4.572)
MIN

PIN NO. 1
IDENT

24 23 22 21 20 19 18 17 16 15 14 13

0.360 − 0.420
(9.144 − 10.67)

1 2 3 4 5 6 7 8 9 10 11 12

0.030
(0.762)
MIN

0.250 − 0.350
(6.350 − 8.890)

0.003 − 0.006
(0.076 − 0.152)

0.005
(0.127)
MIN
ALL ENDS

0.015 − 0.019
(0.381 − 0.483)

F24D (REV D)

Order Number DM2504F or DM2504CF
NS Package Number F24D

0.785
[19.94] MAX

16   9

0.220−0.310
[5.59−7.87]

R 0.025
[0.64]

1   8

R 0.005−0.020
[0.13−0.51] TYP

0.037 ± 0.005
[0.94 ± 0.13] TYP

0.005
[0.13]
MIN TYP

0.055 ± 0.005
[1.40 ± 0.13] TYP

0.290−0.320
[7.37−8.13]

GLASS SEALANT

0.020−0.060
[0.51−1.52] TYP

0.200
[5.08]
MAX TYP

0.180
[4.57] MAX

0.010 ± 0.002
[0.25 ± 0.05] TYP

0.125−0.200
[3.18−5.08] TYP

0.150 MIN TYP
[3.81]

90° ± 4°
TYP

95° ± 5°
TYP

0.080
[2.03] MAX
BOTH ENDS

0.018 ± 0.003
[0.46 ± 0.08] TYP

0.310−0.410
[7.87−10.41]

0.100 ± 0.010
[2.54 ± 0.25] TYP
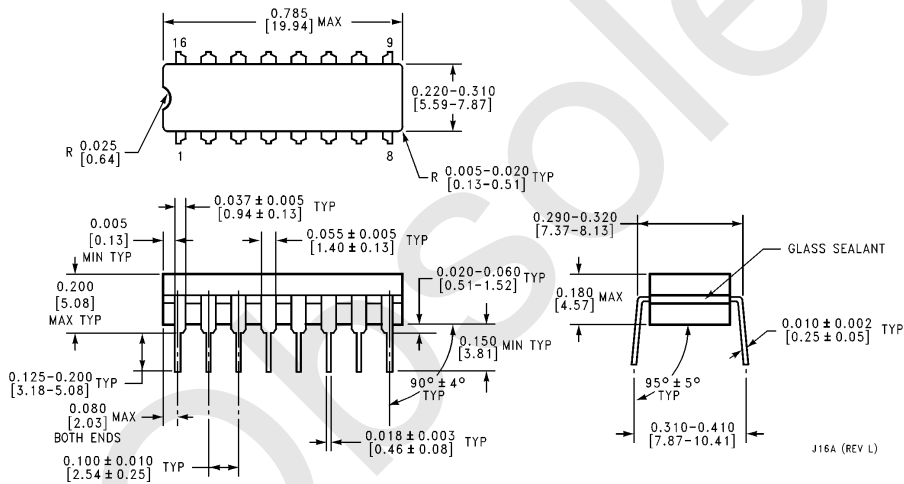
J16A (REV L)

Order Number DM2502J, DM2502CJ, DM2503J or DM2503CJ
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)
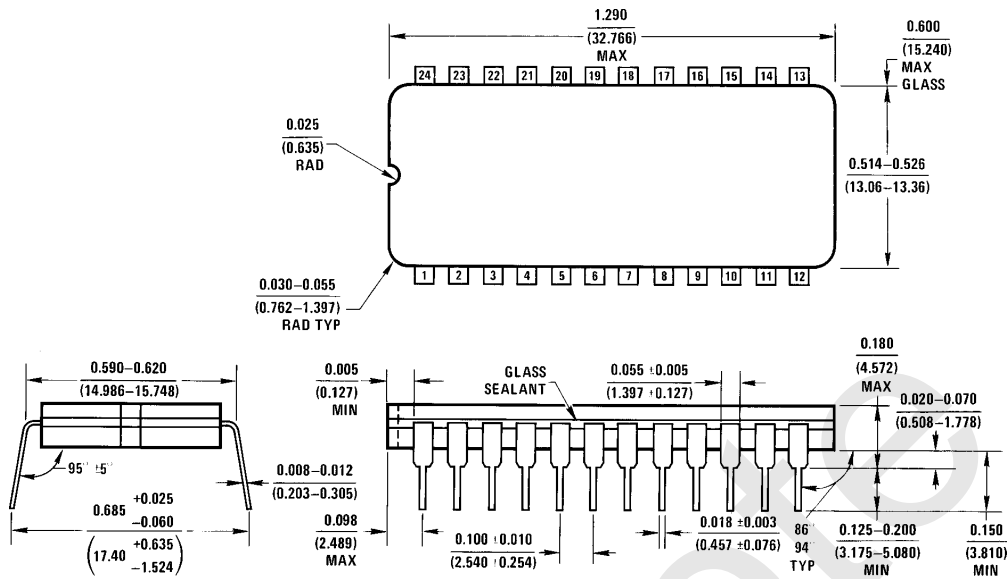
Order Number DM2504J or DM2504CJ
NS Package Number J24A
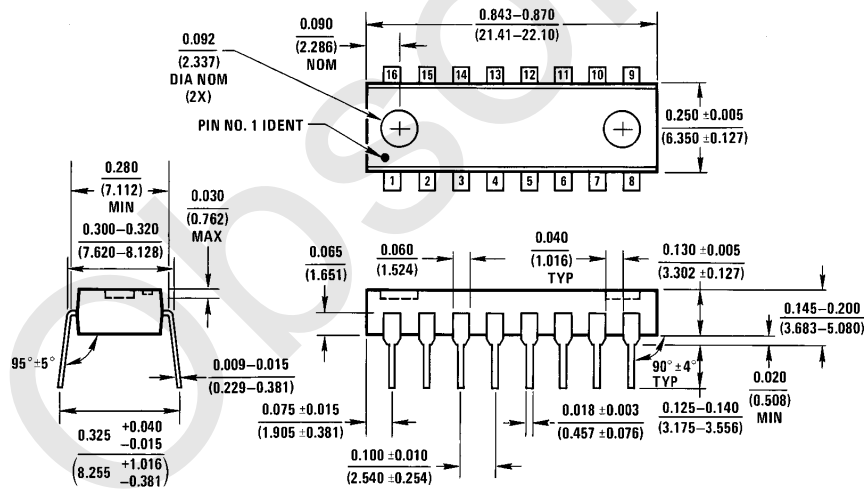
Order Number DM2502CM or DM2503CN
NS Package Number N16A

Physical Dimensions inches (millimeters) (Continued)
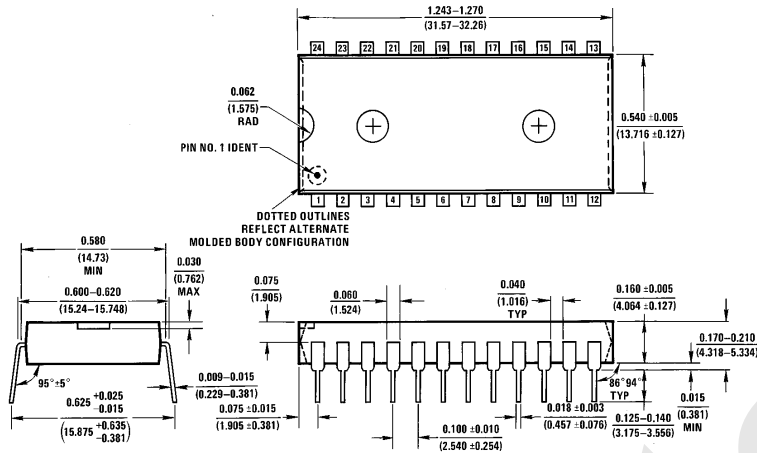
Order Number DM2504CN
NS Package Number N24A

N24A (REV E)
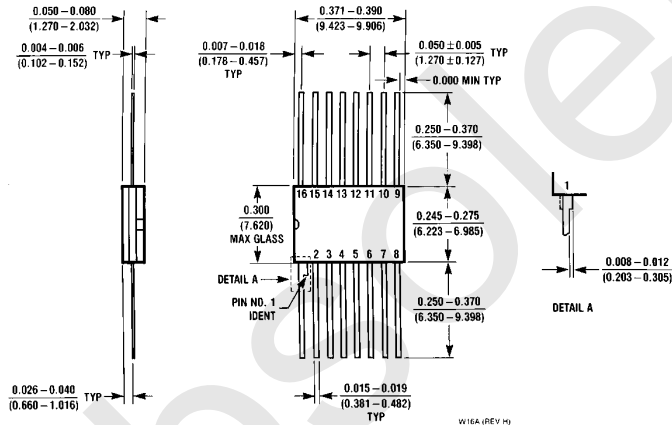
Order Number DM2502W, DM2502CW, DM2503W, or DM2503CW
NS Package Number W16A

W16A (REV H)

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