TTL MSI

DM5483 / DM7483 (SN5483/SN7483)
four-bit binary full adder and
dual single-bit binary full adder

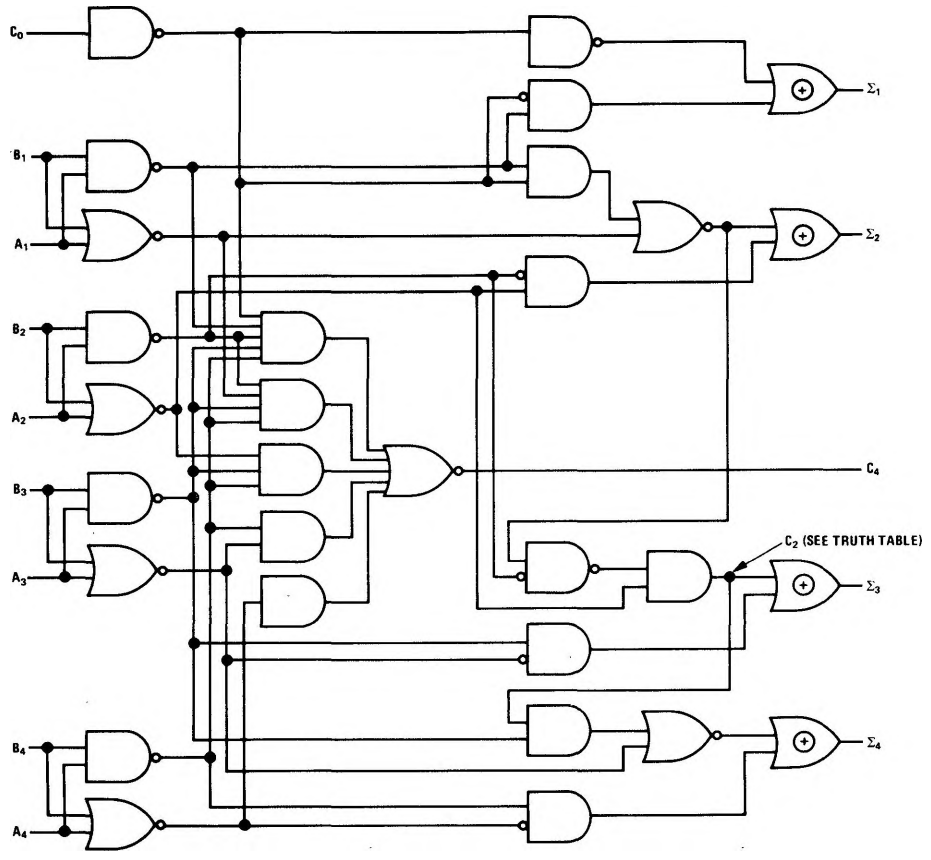
general description

The DM5483/DM7483 binary full adder adds two four-bit binary numbers. A carry input is included and four Σ outputs are provided along with the resultant carry. Since the carry-ripple-time is the limiting delay in the addition of a long word length, carry look-ahead circuitry has been included in the design to minimize this delay. Typical propagation delay from Carry-input to Carry output is 12 ns.

The device can also be used as a dual single-bit binary full adder. (See application.) In this application the Σ_2 output is used as the CARRY output for BIT 1; and the A_3B_3 inputs are used as the CARRY input for Bit 2.

It is completely compatible with other Series 54/74 devices.

logic diagram



absolute maximum ratings

V_{CC}		7V
Input Voltage		5.5V
Operating Temperature Range	DM7483	0°C to 70°C
	DM5483	−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITION		MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V
Logical "1" Input Voltage	DM5483	V_{CC} = 4.5V		2.0			V
	DM7483	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5483	V_{CC} = 4.5V				0.8	V
	DM7483	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM5483	V_{CC} = 4.5V	V_{IN} = 0.8V, I_{OUT} = −400 μA (Note 3)	2.4			V
	DM7483	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM5483	V_{CC} = 4.5V	V_{IN} = 2.0V, I_{OUT} = 16 mA (Note 3)			0.4	V
	DM7483	V_{CC} = 4.75V					
Logical "1" Input Current (all inputs)	DM5483	V_{CC} = 5.5V	V_{IN} = 2.4V			80	μA
	DM7483	V_{CC} = 5.25V					
Logical "1" Input Current	DM5483	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM7483	V_{CC} = 5.25V					
Logical "0" Input Current (all inputs)	DM5483	V_{CC} = 5.5V	V_{IN} = 0.4V			−3.2	mA
	DM7483	V_{CC} = 5.25V					
Output Short Circuit Current (Note 2) (except C_4)	DM5483	V_{CC} = 5.5V		−20		−55	mA
	DM7483	V_{CC} = 5.25V		−18			
Output Short Circuit Current (for C_4)	DM5483	V_{CC} = 5.5V		−27		−70	mA
	DM7483	V_{CC} = 5.25V					
Supply Current	DM5483	V_{CC} = 5.5V			58	79	mA
	DM7483	V_{CC} = 5.25V					

switching characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITION	MIN	TYP	MAX	UNITS
t_{pd1}	C_{IN}	Σ_1	N = 10, C = 50 pF		23	34	ns
t_{pd0}			N = 10, C = 50 pF		20	34	ns
t_{pd1}	C_{IN}	Σ_2	N = 10, C = 50 pF		24	35	ns
t_{pd0}			N = 10, C = 50 pF		22	35	ns
t_{pd1}	C_{IN}	Σ_3	N = 10, C = 50 pF		30	50	ns
t_{pd0}			N = 10, C = 50 pF		24	40	ns
t_{pd1}	C_{IN}	Σ_4	N = 10, C = 50 pF		30	50	ns
t_{pd0}			N = 10, C = 50 pF		28	50	ns
t_{pd1}	C_{IN}	C_4	N = 5, C = 50 pF		12	20	ns
t_{pd0}			N = 5, C = 50 pF		12	20	ns
t_{pd1}	A_2 or B_2	Σ_2	N = 10, C = 50 pF			40	ns
t_{pd0}			N = 10, C = 50 pF			35	ns
t_{pd1}	A_4 or B_4	Σ_4	N = 10, C = 50 pF			40	ns
t_{pd0}			N = 10, C = 50 pF			35	ns

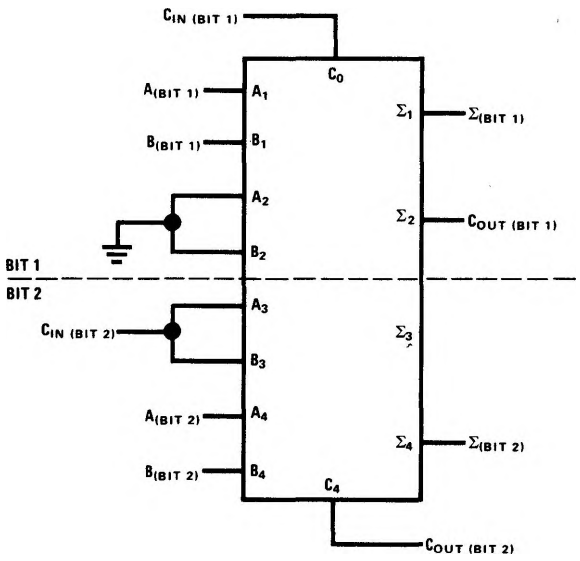
Note 1: Min/Max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7483 and −55°C to +125°C for the DM5483 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C

Note 2: Only one output at a time should be short circuited.

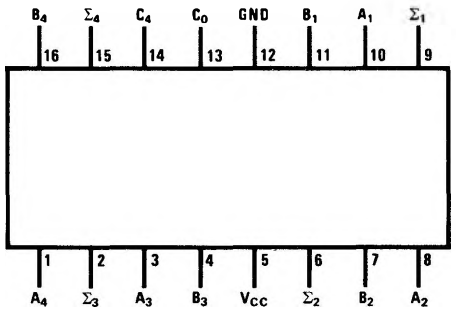
Note 3: For C_4 output, $I_{OUT(1)}$ = −200 μA, $I_{OUT(0)}$ = 8 mA.

typical application

Connect the DM5483/DM7483 in the following manner to implement a dual single-bit full adder.



connection diagram



truth table (See Note 1)

INPUT						OUTPUT					
				WHEN C_{in} = 0			WHEN C_{in} = 1		
				WHEN C_2 = 0			WHEN C_2 = 1		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Note 1: Input conditions at A_1, A_2, B_1, B_2, and C_{in} are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.