DM54L72

DM54L72 AND-Gated Master-Slave J-K Flip-Flop with Preset, Clear and Complementary Outputs

Literature Number: SNOS268A

National Semiconductor

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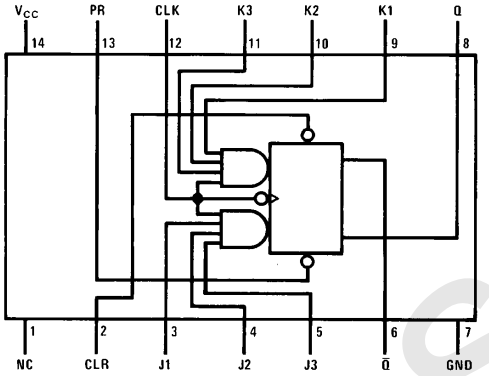
DM54L72 AND-Gated Master-Slave J-K Flip-Flop with Preset, Clear and Complementary Outputs

General Description

This device contains a positive pulse triggered master-slave J-K flip-flop with complementary outputs. Multiple J and K inputs are ANDed together to produce the internal J and K function for the flip-flop. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the AND gates is transferred to the master. While the clock is high the AND gate inputs are disabled. On the negative transition of the clock the data from the master is transferred to the slave. The logic state of the J and K inputs must not be allowed to change while the clock is in the high state. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs sets or resets the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6629–1

Order Number DM54L72J or DM54L72W
See NS Package Number J14A or W14B

Function Table

Inputs					Outputs	
PR	CLR	CLK	J (Note 1)	K (Note 1)	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q_o	$\overline{Q}_o$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	Toggle	

Note 1: J = (J1)(J2)(J3), K = (K1)(K2)(K3)

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

⊓ = Positive pulse. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_o = The output logic level before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

Toggle = Each output changes to the complement of its previous level on each complete high level clock pulse.

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guarateed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L72			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage	Clock			0.6	V
		Others			0.7	
I_{OH}	High Level Output Current				−0.2	mA
I_{OL}	Low Level Output Current				2	mA
f_{CLK}	Clock Frequency (Note 2)		0		6	MHz
t_W	Pulse Width (Note 2)	Clock High	100			ns
		Clock Low	100			
		Preset Low	100			
		Clear Low	100			
t_{SU}	Input Setup Time (Notes 1 & 2)		0 ↑			ns
t_H	Input Hold Time (Notes 1 & 2)		0 ↓			ns
T_A	Free Air Operating Temperature		−55		125	°C

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Note 2: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.15	0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	J, K			100	μA
			Clear			200	
			Preset			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			10	μA
			Clear			20	
			Preset			20	
			Clock			−200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	J, K			−0.18	mA
			Clear			−0.36	
			Preset			−0.36	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max		−3		−15	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			0.76	1.44	mA

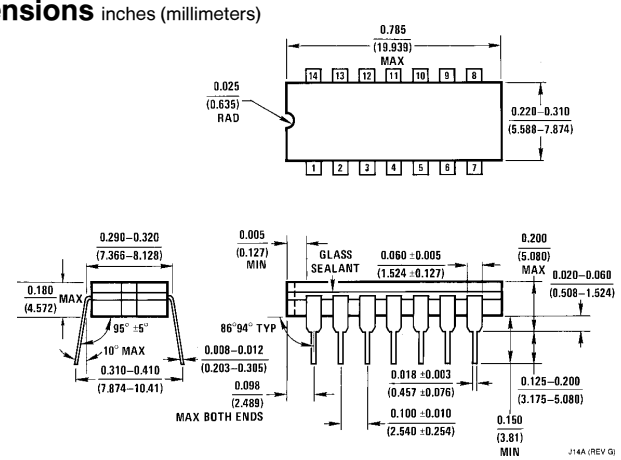
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

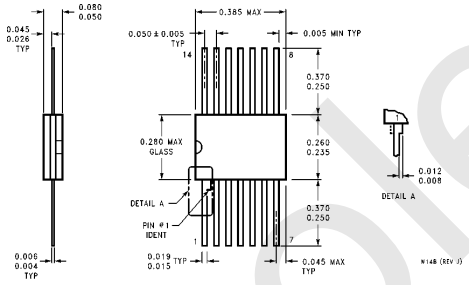
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		75	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		150	ns
t_{PLH}	Propagation Delay Level Output Low to High Level Output	Clear to $\overline{Q}$		75	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		150	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	75	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	150	ns

Physical Dimensions inches (millimeters)



14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54L72J
NS Package Number J14A



14-Lead Ceramic Flat Package (W)
Order Number DM54L72W
NS Package Number W14B

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