# TTL MSI

## DM7520/DM8520 modulo-n divider

### general description

The DM7520/DM8520 combines TTL technology and MSI (Medium Scale Integration) design to provide a circuit equal in complexity to more than 50 gates.

Although extremely versatile in a number of digital applications, its primary usage will be realized in two areas:

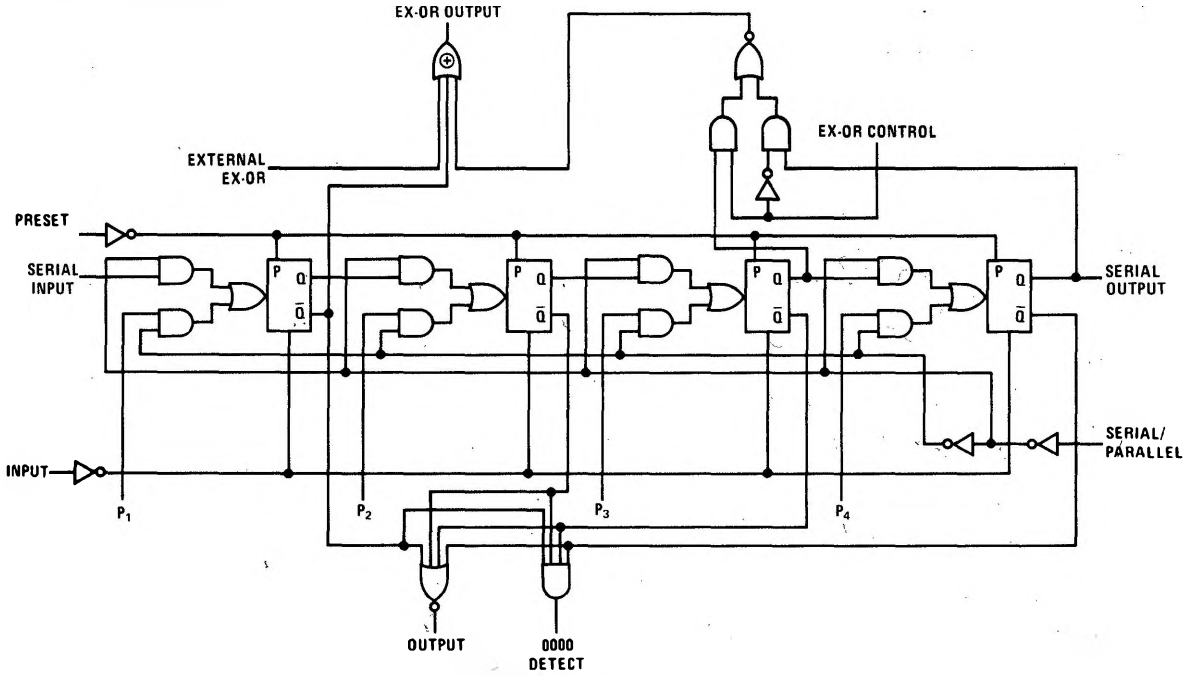
1. **MODULO-N DIVIDER**

   A single DM7520/DM8520 can be programmed without external components to divide by any number from 2 to 15. Cascading of these dividers will provide division by any number from 2 to very large numbers.

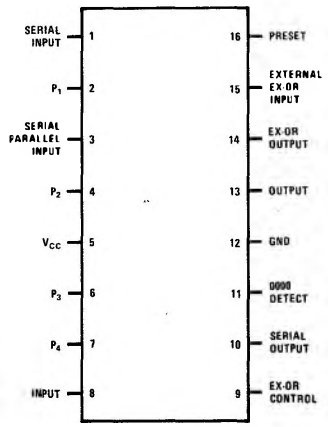
2. **SHIFT REGISTER**

   Since the basic organization of the logic is that of a serial shift register, the device may be used where four-bit parallel-in-serial out shifting is required.

### logic diagram




### connection diagram




### table for division by n

| SETTING $P_1$ | $P_2$ | $P_3$ | $P_4$ | ÷BY |
|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 2 |
| 1 | 1 | 0 | 0 | 3 |
| 1 | 0 | 0 | 0 | 4 |
| 0 | 0 | 0 | 1 | 5 |
| 0 | 0 | 1 | 0 | 6 |
| 0 | 1 | 0 | 0 | 7 |
| 1 | 0 | 0 | 1 | 8 |
| 0 | 0 | 1 | 1 | 9 |
| 0 | 1 | 1 | 0 | 10 |
| 1 | 1 | 0 | 1 | 11 |
| 1 | 0 | 1 | 0 | 12 |
| 0 | 1 | 0 | 1 | 13 |
| 1 | 0 | 1 | 1 | 14 |
| 0 | 1 | 1 | 1 | 15 |

## absolute maximum ratings

| | | |
|---|---|---|
| Supply Voltage | | 7V |
| Input Voltage | | 5.5V |
| Operating Temperature Range | DM7520 | −55°C to +125°C |
| | DM8520 | 0°C to +70°C |
| Storage Temperature Range | | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | | 300°C |

## electrical characteristics (Note 1)

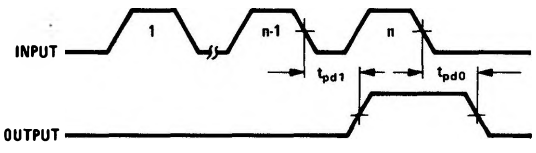
| PARAMETER | | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Logical "1" Input Voltage | DM7520 | $V_{CC}$ = 4.5V | | 2.0 | | | V |
| | DM8520 | $V_{CC}$ = 4.75V | | | | | |
| Logical "0" Input Voltage | DM7520 | $V_{CC}$ = 4.5V | | | | 0.8 | V |
| | DM8520 | $V_{CC}$ = 4.75V | | | | | |
| Logical "1" Output Voltage | DM7520 | $V_{CC}$ = 4.5V | $I_{OUT}$ = −400 μA | 2.4 | | | V |
| | DM8520 | $V_{CC}$ = 4.75V | | | | | |
| Logical "0" Output Voltage | DM7520 | $V_{CC}$ = 4.5V | $I_{OUT}$ = 16 mA | | | 0.4 | V |
| | DM8520 | $V_{CC}$ = 4.75V | | | | | |
| Logical "0" Input Current (All inputs except pin 9) | DM7520 | $V_{CC}$ = 5.5V | $V_{IN}$ = 0.4V | | | 1.6 | mA |
| | DM8520 | $V_{CC}$ = 5.25V | | | | | |
| Logical "0" Input Current (Pin 9) | DM7520 | $V_{CC}$ = 5.5V | $V_{IN}$ = 0.4V | | | 3.2 | μA |
| | DM8520 | $V_{CC}$ = 5.25V | | | | | |
| Logical "1" Input Current | DM7520 | $V_{CC}$ = 5.5V | $V_{IN}$ = 2.4V | | | 40 | μA |
| | DM8520 | $V_{CC}$ = 5.25V | | | | | |
| Logical "1" Input Current (Pin 9) | DM7520 | $V_{CC}$ = 5.5V | $V_{IN}$ = 2.4V | | | 80 | μA |
| | DM8520 | $V_{CC}$ = 5.25V | | | | | |
| Logical "1" Input Current (All inputs except pin 9) | DM7520 | $V_{CC}$ = 5.5V | $V_{IN}$ = 5.5V | | | 1 | mA |
| | DM8520 | $V_{CC}$ = 5.25V | | | | | |
| Output Short Circuit Current (Note 3) | DM7520 | $V_{CC}$ = 5.5V | $V_{OUT}$ = 0V (Note 2) | −20 | | 55 | mA |
| | DM8520 | $V_{CC}$ = 5.25V | | −18 | | | |
| Power Supply Current | | $V_{CC}$ = 5.0V | $T_A$ = 25°C | | 50 | | mA |
| Counting Frequency | | $V_{CC}$ = 5.0V | $T_A$ = 25°C | | 20 | | MHz |

**Note 1:** Unless otherwise specified, limits shown apply across the −55°C to +125°C temperature range for the DM7520 and the 0°C to +70°C temperature range for the DM8520. Typical values apply to supply voltages of 5.0V.

**Note 2:** Only one output should be shorted at a time.

**Note 3:** Serial and exclusive OR outputs.

## switching time waveforms



## theory of operation

The basic operation of the DM7520/DM8520 is derived from the fact that when several outputs of a shift register are EXCLUSIVE OR'ed and the result fed back to the register's input, a unique progression of stable states results on the outputs of the flip-flops. Depending upon which outputs are EXCLUSIVE OR'ed the number of different states can be varied. Even if optimum gating is provided the most states which can be obtained is $2^n$-1, where n is equal to the number of flip-flops in the register. The all-zero state is precluded; and, therefore, the maximum number of states is always one less than the theoretical maximum number. Since the DM7520/DM8520 contains four flip-flops, its maximum number of states is 15. Because the 1111 state occurs only once during a 15-state sequence, this state is detected; and its output becomes the output of the divider.

To obtain frequency division by numbers other than the maximum, it is necessary to cause the register to "jump" immediately from its initial 1111 to the state which it would normally reach in 16-m (m = desired frequency division) pulses. For example, to divide by eleven it would be necessary to jump to the fifth state and then simply allow the register to normally progress forward to its original state. The output of the divider is also used as a control pulse. Since the 1111 state is detected and since the "jump-state" information is of interest only at the time that this state is reached, the OUTPUT is used to gate the parallel inputs, through the SERIAL/PARALLEL input, so that it recognizes this "jump-state" information only at this time. Subsequently as the states change, the parallel input information is locked from the divider.

Should the divider ever be accidently set in the forbidden 0000 state, an output is provided to detect this state. If this output is in turn fed into the EXTERNAL EX-OR input, a 1 will be forced into the register at the next clock pulse, thus clearing the unallowed state.

A PRESET input is provided which when taken to a logical "1" level overrides all other inputs and sets the register to the 1111 state.

To divide by numbers greater than 15, it is necessary to cascade DM7520/DM8520's. Both the OUTPUT and the 0000 DETECT output are capable of being connected directly to other like outputs thus providing the "WIRED-OR" configuration. These outputs should be connected to the similar outputs on other dividers for proper operation. All SERIAL/PARALLEL inputs should be connected to the common OUTPUT.

Other connections are shown. (Figure 1 indicates connections for 2 dividers or a maximum frequency division of 255. For division by higher numbers, a more complete discussion of the interconnection techniques will be given in the final data sheet.)

To divide by numbers between 16 and 255, the table in Figure 2 will apply.

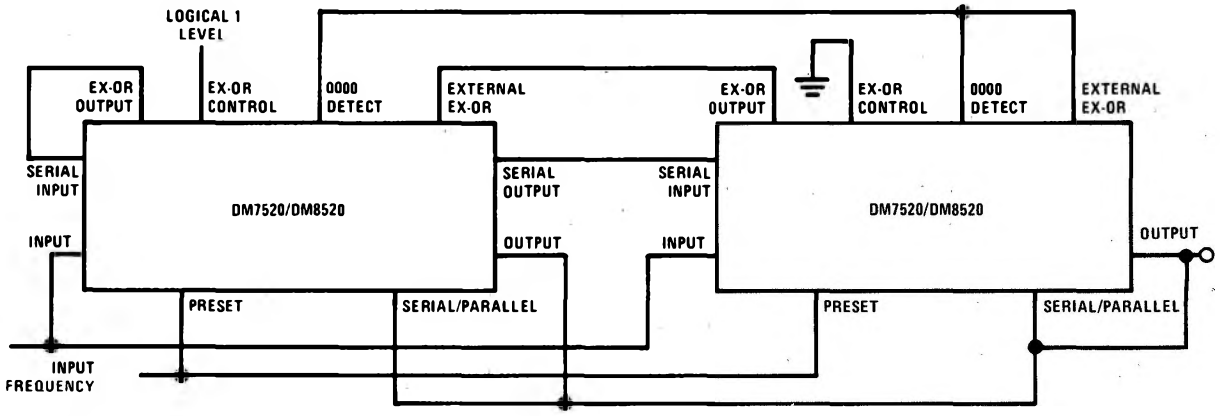



**FIGURE 1. Connection for 2 Divider or Maximum Frequency Division of 255**

| SETTING | | | | | | | | ÷ BY |
|---|---|---|---|---|---|---|---|---|
| DIVIDER 1 | | | | DIVIDER 2 | | | | |
| $P_1$ | $P_2$ | $P_3$ | $P_4$ | $P_1$ | $P_2$ | $P_3$ | $P_4$ | |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 255 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 254 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 253 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 252 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 251 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 250 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 249 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 248 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 247 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 246 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 245 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 244 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 243 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 242 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 241 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 240 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 239 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 238 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 237 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 236 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 235 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 234 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 233 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 232 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 231 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 230 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 229 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 228 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 227 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 226 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 225 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 224 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 223 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 222 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 221 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 220 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 219 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 218 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 217 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 216 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 215 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 214 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 213 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 212 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 211 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 210 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 209 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 208 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 207 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 206 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 205 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 204 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 203 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 202 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 201 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 200 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 199 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 198 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 197 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 196 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 195 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 194 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 193 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 192 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 191 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 190 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 189 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 188 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 187 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 186 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 185 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 184 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 183 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 182 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 181 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 180 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 179 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 178 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 177 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 176 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 175 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 174 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 173 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 172 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 171 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 170 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 169 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 168 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 167 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 166 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 165 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 164 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 163 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 162 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 161 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 160 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 159 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 158 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 157 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 156 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 155 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 154 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 153 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 152 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 151 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 150 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 149 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 148 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 147 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 146 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 145 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 144 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 143 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 142 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 141 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 140 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 139 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 138 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 137 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 136 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 135 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 134 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 133 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 132 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 131 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 130 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 129 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 128 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 127 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 126 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 125 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 124 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 123 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 122 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 121 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 120 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 119 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 118 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 117 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 116 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 115 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 114 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 113 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 112 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 111 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 110 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 109 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 108 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 107 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 106 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 105 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 104 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 103 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 102 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 101 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 100 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 99 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 98 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 97 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 96 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 95 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 94 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 93 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 92 |

**FIGURE 2. DM7520/8520 Shift Register Divider Input Coding Table (2 Package Combinations)**