Interface Gates

DM7800/DM8800 dual voltage translator

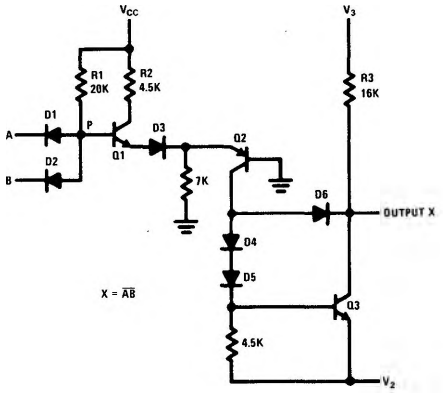
general description

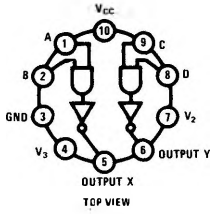
The DM7800/DM8800 are dual voltage translators designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with high impedance junction or MOS FET-type devices. The design allows the user a wide latitude in his selection of power supply voltages, thus providing custom control of the output swing. The translator is especially useful in analog switching; and since low power dissipation occurs in the "off" state, minimum system power is required.

Additional features include:

- 31 volt (max) output swing
- 1 mW power dissipation in normal state
- Standard 5V power supply
- Temperature range:
  DM7800 −55°C to +125°C
  DM8800 0°C to +70°C
- Compatible with all MOS devices

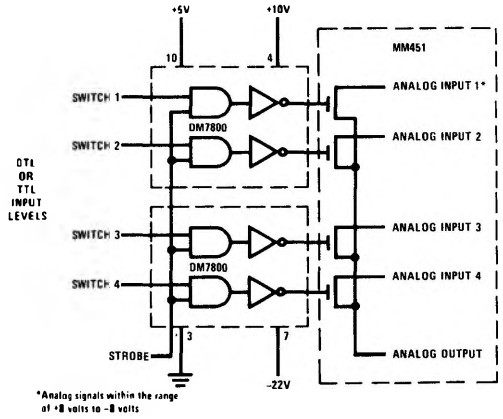
schematic and connection diagram



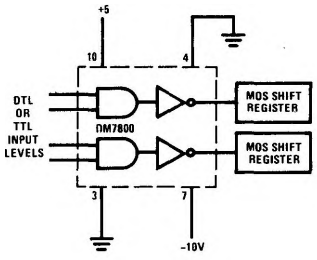


typical applications

4 channel analog switch



bipolar to MOS interfacing



absolute maximum ratings

V_{CC} Supply Voltage	7.0V
V_2 Supply Voltage	−30V
V_3 Supply Voltage	+30V
V_3-V_2 Voltage Differential	40V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM7800	−55°C to +125°C
DM8800	0°C to 70°C
Lead Temperature (Soldering, 10 sec)	300°C

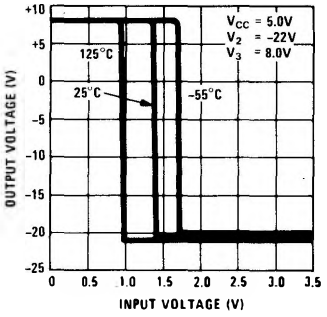
electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Logical "1" Input Voltage	DM7800 / DM8800	V_{CC} = 4.5V / V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM7800 / DM8800	V_{CC} = 4.5V / V_{CC} = 4.75V			0.8	V
Logical "1" Input Current	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 2.4V			5	μA
Logical "1" Input Current	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 0.4V		0.2	0.4	mA
Output Leakage Current (Note 2)	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 0.8V (Note 5)			10	μA
Output Collector Resistor		T_A = 25°C	11.5	16.0	20.0	kΩ
Logical "0" Output Voltage	DM7800 / DM8800	V_{CC} = 4.5V / V_{CC} = 4.75V V_{IN} = 2.0V (Note 5)			V_2 + 2.0	V
Power Supply Current Logical "0" (Note 3) (Each Gate)	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "1" (Note 3) (Each Gate)	DM7800 / DM8800	V_{CC} = 5.5V / V_{CC} = 5.25V V_{IN} = 0V		0.22	0.41	mA
Transition Time to Logical "0" Output		T_A = 25°C C = 15 pF	25	70	125	ns
Transition Time to Logical "1" Output		T_A = 25°C C = 15 pF	25	62	125	ns

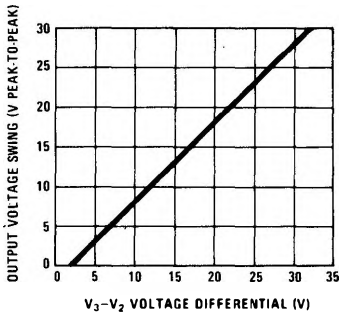
Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for the DM7800 and 0°C to +70°C for the DM8800 unless otherwise specified.
Note 2: Current measured is drawn from V_3 supply.
Note 3: Current measured is drawn from V_{CC} supply.
Note 4: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V, V_2 = −22V, V_3 = +8V.
Note 5: Specification applies for all allowable values of V_2 and V_3.

typical performance characteristics (Note 6)

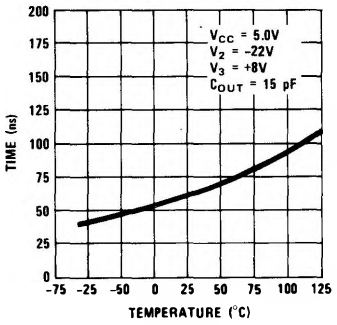
V_{IN}-V_{OUT}



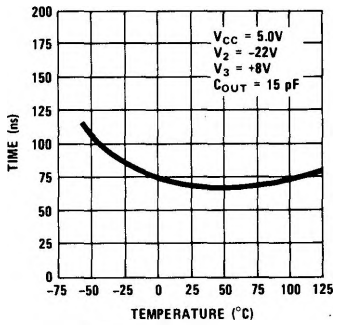
Output Voltage Swing



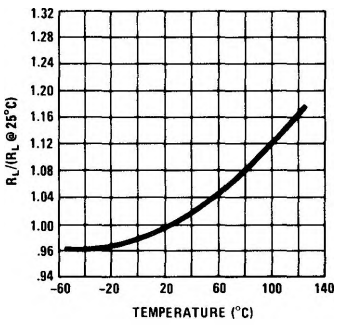
$T_{pd\ 1}$ vs Temperature



$T_{pd\ 0}$ vs Temperature



Logical "1" Output Resistance



Note 6: Curves also describe performance of DM8800 over 0°C to +70°C temperature range.

theory of operation

The two input diodes perform the AND function on TTL or DTL input voltage levels. When at least one input voltage is a logical "0", current from V_{CC} (nominally 5.0V) passes through R_1 and out the input(s) which is at the low voltage. Other than small leakage currents, this current drawn from V_{CC} through the 20 kΩ resistor is the only source of power dissipation in the logical "1" output state.

When both inputs are at logical "1" levels, current passes through R_1 and diverts to transistor Q_1, turning it on and thus pulling current through R_2. Current is then supplied to the PNP transistor, Q_2. The voltage losses caused by current through Q_1, D_3, and Q_2 necessitate that node P reach a voltage sufficient to overcome these losses before current begins to flow. To achieve this voltage at node P, the inputs must be raised to a voltage level which is one diode potential lower than node P. Since these levels are exactly the same as those experienced with conventional TTL and DTL, the interfacing with these types of circuits is achieved.

Transistor Q_2 provides "constant current switching" to the output due to the common base connection of Q_2. When at least one input is at the logical "0" level, no current is delivered to Q_2; so that its collector supplies essentially zero current to the output stage. But when both inputs are raised to a logical "1" level current is supplied to Q_2. Since this current is relatively constant, the collector of Q_2 acts as a constant current source for the output stage. Logic inversion is performed since logical "1" input voltages cause current to be supplied to Q_2 and to Q_3. And when Q_3 turns on the output voltage drops to the logical "0" level.

The reason for the PNP current source, Q_2, is so that the output stage can be driven from a high impedance. This allows voltage V_2 to be adjusted in accordance with the application. Negative voltages to -25V can be applied to V_2. Since the output will neither source nor sink large amounts of current, the output voltage range is almost exclusively dependent upon the values selected for V_2 and V_3.

Maximum leakage current through the output transistor Q_3 is specified at 10 μA under worst-case voltage between V_2 and V_3. This will result in a logical "1" output voltage which is 0.2V below V_3. Likewise the clamping action of diodes D_4, D_5, and D_6, prevents the logical "0" output voltage from falling lower than 2V above V_2, thus establishing the output voltage swing at typically 2 volts less than the voltage separation between V_2 and V_3.