National Semiconductor

DP802514-1 TROPIC REEF+™, DP802515-1 TROPIC PELÉ+™, TROPIC™ Microcode ROM

General Description

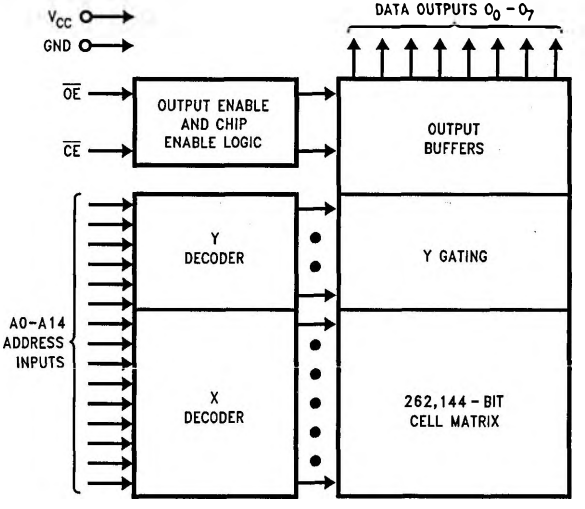
The DP802514-1 and DP802515-1 are the microcode ROMs for the TROPIC token ring network controllers. The DP802514-1 is a TROPIC REEF+ device and the DP802515-1 is a TROPIC PELÉ+ device. The devices feature an interface that is compatible to DP8025 interface controller to allow direct interfacing without the use of glue logic.

The DP802514-1 and DP802515-1 are implemented in National's double poly, single metal CMOS process. They operate from a single 5V ±10% power supply. They are available in 28-pin, DIP or 32-pin PLCC.

Features

- TROPIC compatible
  - Glueless interface
- High reliability CMOS processing
  - ESD protection exceeds 2000V
  - Latch up immunity to 200 mA
- Surface mount and DIP package
  - 28-pin molded plastic DIP
  - 32-pin PLCC

Block Diagram



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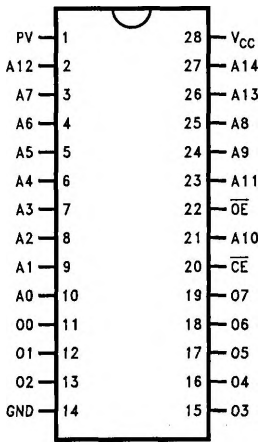
Connection Diagrams

DIP



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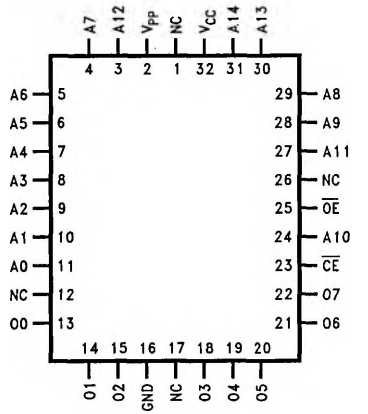
Order Number DP802514-1N or DP802515-1N
See NS Package Number N28B

PLCC



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Order Number DP802514-1V or DP802515-1V
See NS Package Number VA32A

Commercial Temperature Range
(0°C to +70°C) V_{CC} = 5V ±10%

Order Number	Microcode Section	Check Sum
DP802514-1N, V	Even/Lower	7940
DP802515-1N, V	Odd/Upper	D739

Pin Names

Symbol	Description
A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
PV*	Connect to V_{CC}

*This function is used during test/manufacture.
Should be connected to V_{CC} in application.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages with Respect to Ground	−0.6V to +7V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground	V_{CC} +1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +60°C	5V ±10%
Industrial	−40°C to +85°C	5V ±10%

Read Operation

DC Electrical Characteristics Over Operating Range

Symbol	Parameter	Test Condtions	Min	Max	Units
V_{IL}	Input Low Level		−0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA	3.5		V
I_{CCSB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3V		100	μA
I_{CCSB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}		1	mA
I_{CC}	V_{CC} Standby Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 5 MHz I/O = 0 mA		35	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}		10	μA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	−10	10	μA

AC Electrical Characteristics Over Operating Range

Symbol	Parameter	Min	Max
t_{ACC}	Address to Output Delay		95
$t_{\overline{CE}}$	$\overline{CE}$ to Output Delay		95
$t_{\overline{OE}}$	$\overline{OE}$ to Output Delay		40
t_{DF} (Note 2)	Output Disable to Output Float		25
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurred First	7	

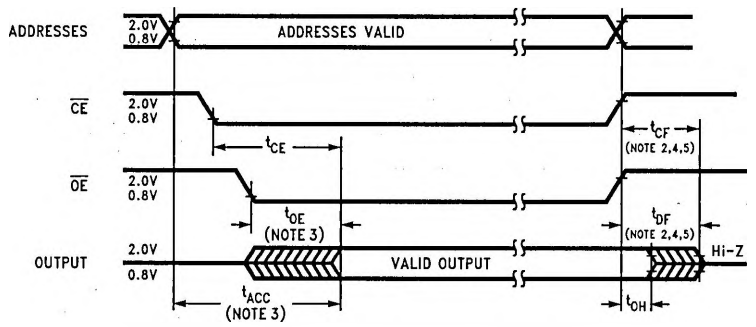
Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note ≤ 5 ns)
Input Pulse Levels	0.45V to 2.4V
Input Pulse Level	0.45V to 2.4V
Timing Measurement Level	(Note 8)
Inputs	0.8V to 2V
Outputs	0.8V to 2V

AC Waveforms (Notes 6, 7 and 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{\overline{CE}}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measure V_{CH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics require careful device decoupling. It is recommended that at least a 0.2 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA, C_L: 100 pF includes fixture capacitance.

Functional Description

DEVICE OPERATION

The three modes of operation of the DP802514-1 and DP802515-1 are listed in Table I. It should be noted that all inputs for the three modes are at TTL levels. The power supply required is V_{CC}.

READ MODE

THE DP802514-1 and DP802515-1 have two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs $t_{\overline{OE}}$ after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{\overline{OE}}$.

STANDBY MODE

The DP802514-1 and DP802515-1 have a standby mode which reduces the active power dissipation by over 99%, from 75 mW to 0.55 mW. They are placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT DISABLE

The DP802514-1 and DP802515-1 are placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

APPLICATION

In application, the DP802514-1 and DP802515-1 should be connected to the DP8025 TROPIC controller as shown in *Figure 1*. The DP802514-1 is the lower microcode ROM, and O_0 thru O_7 are to be connected to SD_0 thru SD_7. The DP802515-1 is the upper microcode ROM and O_0 thru O_7 are to be connected to SD_8 thru SD_{15} of the DP8025.

SYSTEM CONSIDERATION

The power switching characteristics of DP802514-1 and DP802515-1 require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.2 μF ceramic capacitor be used on every device between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the subsystem. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the DP802514-1 and DP802515-1 are listed in Table I. A single 5V power supply is required. All inputs are TTL levels except for PV = V_{CC}.

Mode Selection (Continued)

TABLE I. Modes Selection

Mode \ Pins	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	PV	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	5.0V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	V_{CC}	5.0V	High Z

Note 1: X can be V_{IL} or V_{IH}.

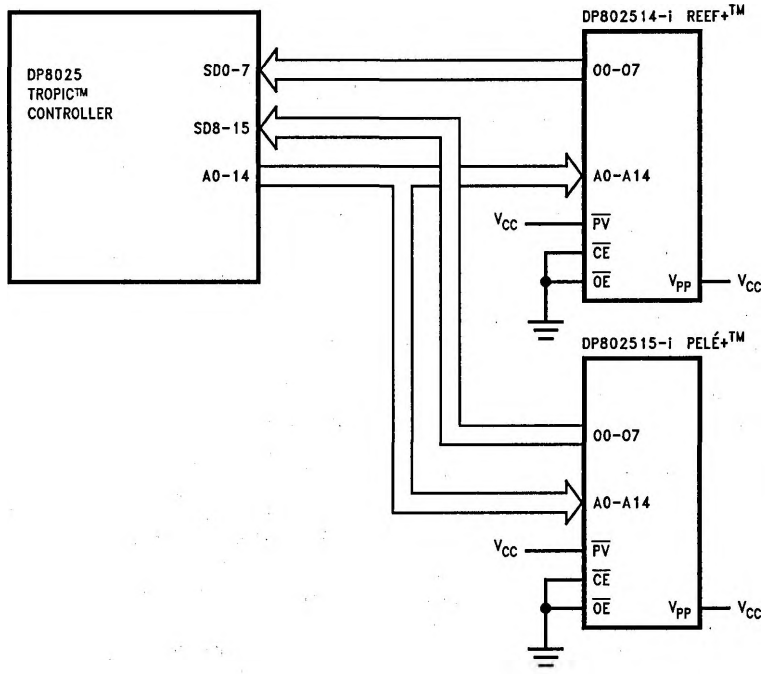

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FIGURE 1. Typical TROPIC Connection