![National Semiconductor logo] **National Semiconductor**

DP83256/DP83257
PLAYER + ™ Device (FDDI Physical Layer Controller)

General Description

The DP83256/DP83257 Enhanced Physical Layer Controller (PLAYER+ device) implements one complete Physical Layer (PHY) entity as defined by the Fiber Distributed Data Interface (FDDI) ANSI X3T9.5 standard.

The PLAYER+ device integrates state of the art digital clock recovery and improved clock generation functions to enhance performance, eliminate external components and remove critical layout requirements.

FDDI Station Management (SMT) is aided by Link Error Monitoring support, Noise Event Timer (TNE) support, Optional Auto Scrubbing support, an integrated configuration switch and built-in functionality designed to remove all stringent response time requirements such as PC_React and CF_React.

Features

- Single chip FDDI Physical Layer (PHY) solution
- Integrated Digital Clock Recovery Module provides enhanced tracking and greater lock acquisition range
- Integrated Clock Generation Module provides all necessary clock signals for an FDDI system from an external 12.5 MHz reference

- Alternate PMD Interface (DP83257) supports UTP twisted pair FDDI PMDs with no external clock recovery or clock generation functions required
- No External Filter Components
- Connection Management (CMT) Support (LEM, TNE, PC_React, CF_React, Auto Scrubbing)
- Full on-chip configuration switch
- Low Power CMOS-BIPOLAR design using a single 5V supply
- Full duplex operation with through parity
- Separate management interface (Control Bus)
- Selectable Parity on PHY-MAC Interface and Control Bus Interface
- Two levels of on-chip loopback
- 4B/5B encoder/decoder
- Framing logic
- Elasticity Buffer, Repeat Filter, and Smoother
- Line state detector/generator
- Supports single attach stations, dual attach stations and concentrators with no external logic
- DP83256 for SAS/DAS single path stations
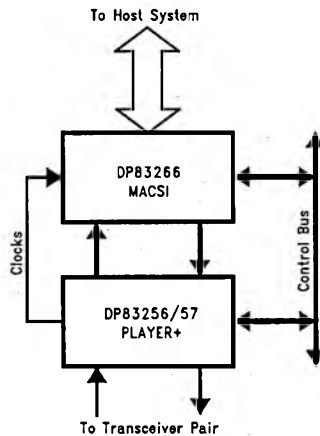- DP83257 for SAS/DAS single/dual path stations

FIGURE 1-1. FDDI Chip Set Overview

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