DP84240,DP84244

DP84240 DP84244 Octal TRI-STATE(RM) MOS Drivers

![Texas Instruments logo]

Literature Number: SNOSBD9A

National **S**emiconductor

March 1986

DP84240/DP84244 Octal TRI-STATE® MOS Drivers

General Description

The DP84240 and DP84244 are octal TRI-STATE drivers which are designed for heavy capacitive load applications such as fast data buffers or as memory address drivers. The DP84240 is an inverting driver which is pin-compatible with both the 74S240 and AM2965. The DP84244 is a non-inverting driver which is pin-compatible with the 74S244 and AM2966. These parts are fabricated using an oxide isolation process, for much faster speeds, and are specified for 250 pF and 500 pF load capacitances.

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Features

■ t_{pd} specified with 250 pF and 500 pF loads
■ Output specified from 0.8V to 2.7V
■ Designed for symmetric rise and fall times at 500 pF
■ Outputs glitch free at power up and power down
■ PNP inputs reduce DC loading on bus lines
■ Low static and dynamic input capacitance
■ Low skew times between edges and pins
■ AC parameters specified with all outputs switching simultaneously

Connection Diagram
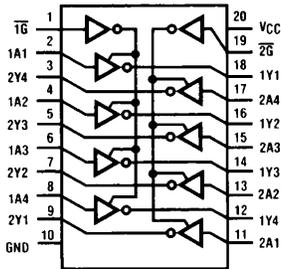
DP84240

TL/F/5219–1

Top View

**Order Number DP84240J or DP84240N
See NS Package Numbers J20A or N20A**

DP84244

TL/F/5219–2

Top View

**Order Number DP84244J or DP84244N
See NS Package Numbers J20A or N20A**

Truth Table

DP84240

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	L	H
L	H	L

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance

DP84244

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	
Cavity Package	1150 mW
Molded Package	1300 mW
Lead Temperature (soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.5	5.5	V
T_A Ambient Temperature	0	+70	°C

Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $0 \leq T_A \leq 70°C$. (Notes 2 and 3.)

| Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 2.7V$		0.1	20	μA
		$V_{IN} = 7.0V$			100	μA
$I_{IN(0)}$	Logical "0" Input Current	$0 \leq V_{IN} \leq 0.4V$		−50	−200	μA
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -18$ mA		−1	−1.2	V
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -100$ μA $I_{OH} = -1$ mA	$V_{CC}-1.15$ $V_{CC}-1.5$	4.3 3.9		V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 10$ μA $I_{OL} = 12$ mA		0.2 0.3	0.4 0.5	V
I_{1D}	Logical "1" Drive Current	$V_{OUT} = 1.5V$	−75	−250		mA
I_{0D}	Logical "0" Drive Current	$V_{OUT} = 1.5V$	+100	+150		mA
Hi-Z	TRI-STATE Output Current	$0.4V \leq V_{OUT} \leq 2.7V$	−100		+100	μA

I_{CC}	Supply Current
	DP84240
		All Outputs Open
		  All Outputs High
		  All Outputs Low
		  All Outputs Hi-Z
				16
				74
				80
					50
					125
					125
						mA

	DP84244	All Outputs High All Outputs Low All Outputs Hi-Z		40 100 115	75 130 150	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

Note 3: Typical characteristics are taken at $V_{CC} = 5.0V$ and $T_A = 25°C$.

Note 4: The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See *Figures 5* and *6* for the switching time variations.
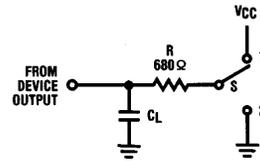
Switching Characteristics

V_{CC} = 5V $\pm$10%, 0 $\leq$ T$_A$ $\leq$ 70°C, all outputs loaded with specified load capacitance and all eight outputs switching simultaneously. (Note 3.)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay from LOW-to-HIGH Output	*Figures 1 & 3*	CL = 250 pF	9	16	27	ns
			C_L = 500 pF	10	20	33	
t_{PHL}	Propagation Delay from HIGH-to-LOW Output		C_L = 250 pF	9	16	25	ns
			C_L = 500 pF	12	20	31	
t_{PLZ}	Output Disable Time from LOW	*Figures 2 & 4,* S = 1, C_L = 50 pF			11	24	ns
t_{PHZ}	Output Disable Time from HIGH	*Figures 2 & 4,* S = 2, C_L = 50 pF			12	24	ns
t_{PZL}	Output Enable Time to LOW	*Figures 2 & 4,* S = 1, C_L = 500 pF			30	45	ns
t_{PZH}	Output Enable Time to HIGH	*Figures 2 & 4,* S = 2, C_L = 500 pF			23	35	ns
t_{SKEW}	Output-to-Output Skew (Note 4)	*Figures 1 & 3,* C_L = 500 pF			3		ns

Capacitance

T$_A$ = 25°C, f = 1 MHz, V_{CC} = 5V $\pm$10%. (Note 3.)

Parameter	Conditions	Typ	Units
C_{IN}	All Other Inputs Tied Low	6	pF
C_{OUT}	Output in TRI-STATE Mode	20	pF

Note 1: ''Absolute Maximum Ratings'' are those values beyond which the safety of the device cannot be guaranteed. Except for ''Operating Temperature Range'' they are not meant to imply that the devices should be operated at these limits. The table of ''Electrical Characteristics'' provides conditions for actual device operation.

Note 2: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

Note 3: Typical characteristics are taken at V_{CC} = 5.0V and T$_A$ = 25°C.

Note 4: The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See *Figures 5* and *6* for the switching time variations.

Switching Test Circuits
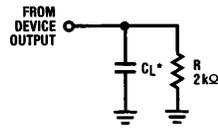
TL/F/5219–3

*C_L INCLUDES PROBE AND JIG CAPACITANCES

FIGURE 1. Capacitive Load Switching
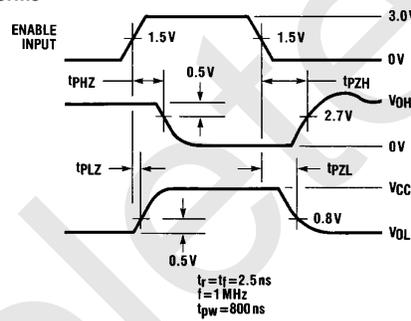

TL/F/5219–4

FIGURE 2. TRI-STATE Enable/Disable
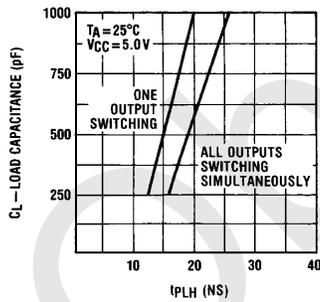
Typical Switching Characteristics

Voltage Waveforms
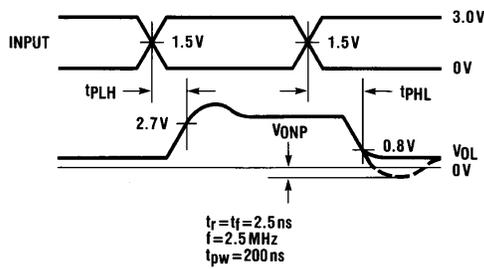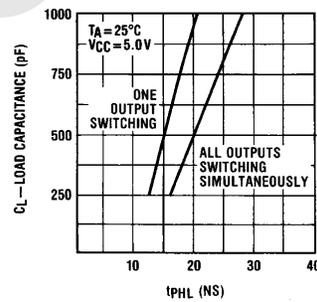

TL/F/5219–5

FIGURE 3. Output Drive Levels

TL/F/5219–6

FIGURE 4. TRI-STATE Control Levels

TL/F/5219–7

FIGURE 5. t_{PLH} Measured to 2.7V on Output vs. C_L

TL/F/5219–8

FIGURE 6. t_{PHL} Measured to 0.8V on Output vs. C_L

4

Typical Switching Characteristics (Continued)

TL/F/5219-9
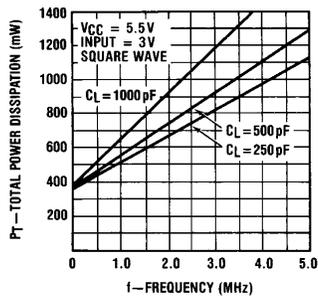
FIGURE 7. Typical Power Dissipation for DP84240 at $V_{CC} = 5.5V$ (All 8 drivers switching simultaneously)
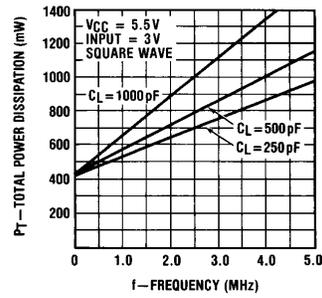
TL/F/5219-10

FIGURE 8. Typical Power Dissipation for DP84244 at $V_{CC} = 5.5V$ (All 8 drivers switching simultaneously)

Typical Application

DP84244 used as a buffer in a large memory array (greater than 88 dynamic RAMs)

TL/F/5219-11

5
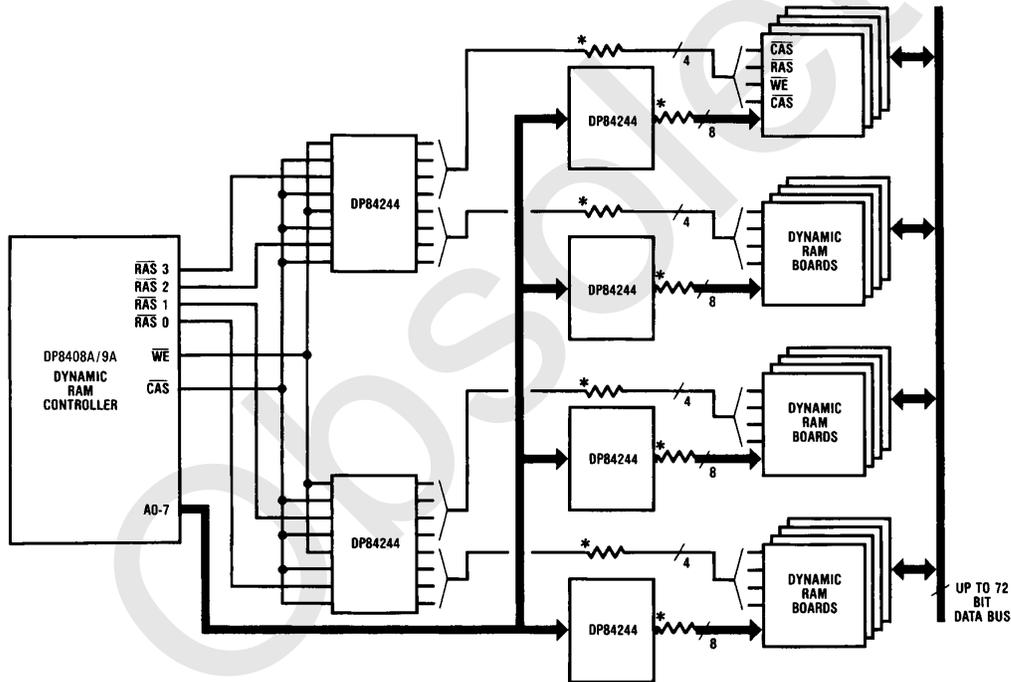
Physical Dimensions inches (millimeters)

0.985
(25.019)
MAX

0.025
(0.635)
RAD

0.220 – 0.310
(5.588 – 7.874)

0.005 – 0.020
(0.127 – 0.508)
RAD TYP

0.037 ± 0.005
(0.940 ± 0.127)

0.005
(0.127)
MIN

GLASS SEALANT

0.055 ± 0.005
(1.397 ± 0.127)

0.020 – 0.060
(0.508 – 1.524)

0.200
(5.080)
MAX

0.150
(3.810)
MIN

0.125 – 0.200
(3.175 – 5.080)

0.180
(4.572)
MAX

0.290 – 0.320
(7.366 – 8.128)

95° ± 5°

0.008 – 0.012
(0.203 – 0.305)

86° 94°

0.310 – 0.410
(7.874 – 10.41)

0.060
(1.524)
MAX
BOTH ENDS

0.100 ± 0.010
(2.540 ± 0.254)

0.018 ± 0.003
(0.457 ± 0.076)

J20A (REV M)
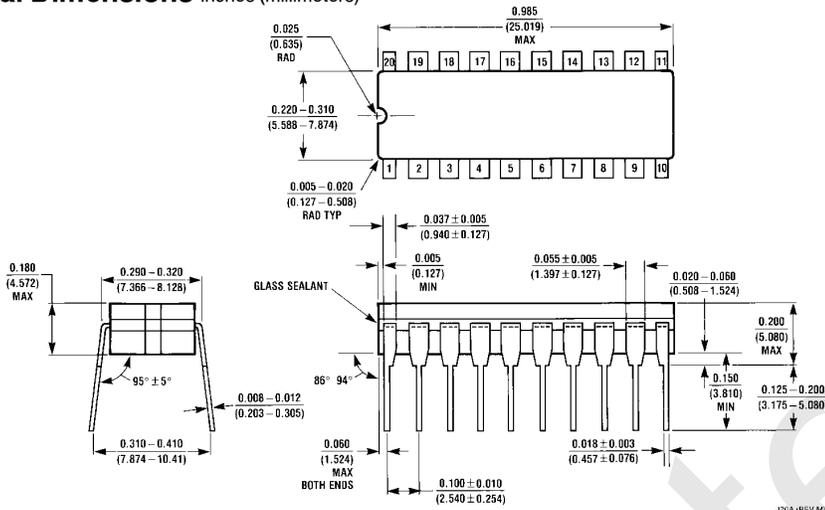
20-Lead Dual-In-Line Package (J)
Order Number DP84240J/DP84244J
NS Package Number J20A

1.013 – 1.040
(25.73 – 26.42)

0.092 × 0.030
(2.337 × 0.762)
MAX DP

PIN NO. 1 IDENT

OPTION 1

0.032 ± 0.005
(0.813 ± 0.127)
RAD

PIN NO. 1 IDENT

OPTION 2

0.260 ± 0.005
(6.604 ± 0.127)

0.280
(7.112)
MIN

0.300 – 0.320
(7.620 – 8.128)

95° ± 5°

0.009 – 0.015
(0.229 – 0.381)
TYP

0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

0.090
(2.286)

0.060
(1.524)
TYP

0.065
(1.651)

0.040
(1.016)
TYP

OPTION 2
4° (4X)

0.130 ± 0.005
(3.302 ± 0.127)

0.145 – 0.200
(3.683 – 5.080)

90° ± 0.004°

0.020
(0.508)
MIN

0.125 – 0.140
(3.175 – 3.556)

0.100 ± 0.010
(2.540 ± 0.254)

0.060 ± 0.005
(1.524 ± 0.127)

0.018 ± 0.003
(0.457 ± 0.076)

N20A (REV G)

20-Lead Dual-In-Line Package (N)
Order Number DP84240N/DP84244N
NS Package Number N20A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

IMPORTANT NOTICE

Products		Applications	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		

TI E2E Community Home Page   e2e.ti.com