

DS14C241

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SNLS083B-MAY 2004-REVISED SEPTEMBER 2004

DS14C241 Single Supply TIA/EIA-232 4 x 5 Driver/Receiver

Check for Samples: DS14C241

FEATURES

- Conforms to TIA/EIA-232-E and CCITT V.28
- Internal DC-DC Converter
- Operates with Single +5V Supply
- Low Power Requirement—I_{CC} 10 mA Max
- Shutdown Mode—I_{CX} 10 μA Max
- Internal Driver Slew Rate Control
- Receiver Noise Filtering
- Operates Above 120 kbits/sec
- TRI-STATE Receiver Outputs
- Direct Replacement for MAX241

DESCRIPTION

The DS14C241 is four driver, five receiver device which conforms to the TIA/EIA-232-E standard and CCITT V.28 recommendations. This device eliminates ±12V supplies by employing an internal DC-DC converter to generate the necessary output levels from a single +5V supply. Driver slew rate control and receiver noise filtering have also been internalized to eliminate the need for external slew rate control and noise filtering capacitors. With the addition of TRI-STATE receiver outputs and a shutdown mode, device power consumption is kept to a minimum.

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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

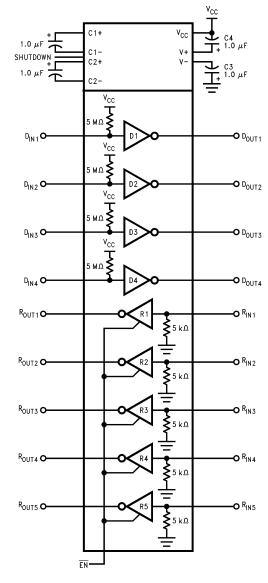


CONNECTION DIAGRAM

$\mathrm{D}_{\mathrm{OUT3}}$ · D_{OUT4} 28 D_{OUT 1} 27 - R_{IN3} D_{OUT2} 26 - R_{OUT3} - SHUTDOWN (SD) 25 R_{IN2} – EN 24 R_{OUT2} – R_{IN4} 23 D_{IN2} 22 - R_{OUT4} D_{IN 1} 21 – D_{IN4} R_{OUT 1} - D_{IN3} 20 $R_{\rm IN\,1}$ GND 19 - R_{OUT5} — R_{IN5} $\rm v_{\rm cc}$ C1+ **—** C2-**-** C2+

Figure 1. See Package Number DW

FUNCTIONAL DIAGRAM





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage (V _{CC})		-0.3V to +6V
V ⁺ Pin		(V _{CC} - 0.3V) to +15V
V [−] Pin		+0.3V to −15V
Driver Input Voltage		-0.3V to (V _{CC} + 0.3V)
Driver Output Voltage		$(V^+ + 0.3V)$ to $(V^ 0.3V)$
Receiver Input Voltage		±30V
Receiver Output Voltage		-0.3V to (V _{CC} + 0.3V)
Junction Temperature	+150°C	
Maximum Package Power Dissipation	@ +25°C ⁽³⁾	
	D Package	1520 mW
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C	
Short Circuit Duration (D _{OUT})	continuous	
ESD Rating (HBM, 1.5 kΩ, 100 pF)		≥ 2.0 kV

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Ratings apply to ambient temperature at +25°C. Above this temperature derate: D package 14.3 mW/°C.

RECOMMENDED OPERATING CONDITIONS

	Min	Max	Units
Supply Voltage (V _{CC})	4.5	5.5	V
Operating Free Air Temp. (T _A) DS14C241	0	+70	°C

ELECTRICAL CHARACTERISTICS(1)

Over recommended operating conditions, unless otherwise specified

Symbol	Parameter	Condit	ions	Min	Тур	Max	Units
DEVICE C	HARACTERISTICS					•	
V ⁺	Positive Power Supply	$R_L = 3 \text{ k}\Omega, \text{ C1-C4} = 1.0 \mu$	F, D _{IN} = 0.8V		9.0		V
V ⁻	Negative Power Supply	$R_L = 3 \text{ k}\Omega, \text{ C1-C4} = 1.0 \mu$	F, $D_{IN} = 2.0V$		-8.0		V
Icc	Supply Current (V _{CC})	No Load			8.5	10	mA
I _{CX}	Supply Current Shutdown	$R_L = 3 \text{ k}\Omega, \text{ SD} = V_{CC}$			1.0	10	μΑ
V _{IH}	High Level Enable Voltage		SD	2.4		V _{CC}	V
V _{IL}	Low Level Enable Voltage			GND		0.8	V
I _{IH}	High Level Enable Current			-10		+10	μΑ
I _{IL}	Low Level Enable Current			-10		+10	μΑ
DRIVER C	HARACTERISTICS					•	
V _{IH}	High Level Input Voltage		D _{IN}	2.0		V _{CC}	V
V _{IL}	Low Level Input Voltage			GND		0.8	V
I _{IH}	High Level Input Current	V _{IN} ≥ 2.0V		-10		+10	μΑ
I _{IL}	Low Level Input Current	V _{IN} ≤ 0.8V		-10		+10	μΑ
V _{OH}	High Level Output Voltage	$R_L = 3 \text{ k}\Omega$		5.0	7.5		V
V _{OL}	Low Level Output Voltage				-6.5	-5.0	V
los+	Output High Short Circuit Current	$V_{O} = 0V, V_{IN} = 0.8V$		-30	-15	-5.0	mA
I _{OS} -	Output Low Short Circuit Current	$V_{O} = 0V, V_{IN} = 2.0V$	V _O = 0V, V _{IN} = 2.0V		12	30	mA
R _O	Output Resistance	$-2V \le V_O \le +2V$, $V_{CC} = GI$	ND = 0V	300			Ω

Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

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ELECTRICAL CHARACTERISTICS(1) (continued)

Over recommended operating conditions, unless otherwise specified

Symbol	Parameter	Conditions	i	Min	Тур	Max	Units
RECEIVER	CHARACTERISTICS						
V_{TH}	Input High Threshold Voltage				1.9	2.4	V
V_{TL}	Input Low Threshold Voltage			0.8	1.5		V
V_{HY}	Hysteresis			0.2	0.4	1.0	V
R _{IN}	Input Resistance			3.0	4.5	7.0	kΩ
I _{IN}	Input Current	V _{IN} = +15V		2.14	3.8	5.0	mA
		V _{IN} = +3V		0.43	0.6	1.0	mA
		V _{IN} = −3V		-1.0	-0.6	-0.43	mA
		V _{IN} = −15V		-5.0	-3.8	-2.14	mA
V_{OH}	High Level Output Voltage	$V_{IN} = -3V$, $I_{O} = -3.2$ mA		3.5	4.6		V
		$V_{IN} = -3V$, $I_{O} = -20 \mu A$		4.0	4.9		V
V _{OL}	Low Level Output Voltage	$V_{IN} = +3V$, $I_{O} = +2.0$ mA			0.25	0.4	V
V _{IH}	High Level Input Voltage		EN	2.0		V _{CC}	V
V _{IL}	Low Level Input Voltage			GND		0.8	V
I _{IH}	High Level Input Current	V _{IN} ≥ 2.0V		-10		+10	μΑ
I _{IL}	Low Level Input Current	V _{IN} ≤ 0.8V		-10		+10	μA
l _{OZ}	Output Leakage Current	$\overline{EN} = V_{CC}, \ 0V \le R_{OUT} \le V_{CC}$		-10		+10	μΑ

SWITCHING CHARACTERISTICS(1)

Over recommended operating conditions, unless otherwise specified

Symbol	Parameter	Conditions	Min	Тур	Max	Units
DRIVER C	HARACTERISTICS					
t _{PLH}	Propagation Delay LOW to HIGH	$R_L = 3 \text{ k}\Omega$		0.7	4.0	μs
t _{PHL}	Propagation Delay HIGH to LOW	C _L = 50 pF		0.6	4.0	μs
t _{SK}	Skew t _{PLH} -t _{PHL}	(Figure 2, Figure 3)		0.1	1.0	μs
SR1	Output Slew Rate	$R_L = 3 \text{ k}\Omega \text{ to } 7 \text{ k}\Omega, C_L = 50 \text{ pF}$	4.0	15	30	V/µs
SR2	Output Slew Rate	$R_L = 3 \text{ k}\Omega, C_L = 2500 \text{ pF}$	3.0	5.0		V/µs
RECEIVER	CHARACTERISTICS					
t _{PLH}	Propagation Delay LOW to HIGH	Input Pulse Width > 10 µs C _L = 50 pF (Figure 4, Figure 5)		2.0	6.5	μs
t _{PHL}	Propagation Delay HIGH to LOW			2.8	6.5	μs
t _{SK}	Skew t _{PLH} -t _{PHL}	(Figure 4, Figure 3)		0.8	2.0	μs
t _{PLZ}		(Figure 6, Figure 8)		0.1	2.0	μs
t _{PZL}				0.6	2.0	μs
t _{PHZ}		(Figure 6, Figure 7)		0.2	2.0	μs
t _{PZH}				0.6	2.0	μs
t _{NW}	Noise Pulse Width Rejected	(Figure 4, Figure 5)		2.5	1.0	μs

⁽¹⁾ Receiver AC input waveform for test purposes: $t_r = t_f = 200$ ns, $V_{IH} = 3V$, $V_{IL} = -3V$, f = 64 kHz (128 kbits/sec). Driver AC input waveform for test purposes: $t_r = t_f \le 10$ ns, $V_{IH} = 3V$, $V_{IL} = 0V$, f = 64 kHz (128 kbits/sec).

PARAMETER MEASUREMENT INFORMATION

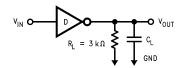


Figure 2. Driver Load Circuit



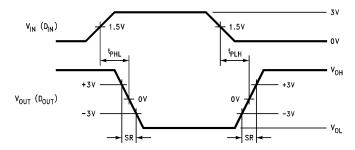


Figure 3. Driver Switching Waveform

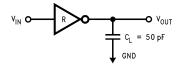


Figure 4. Receiver Load Circuit

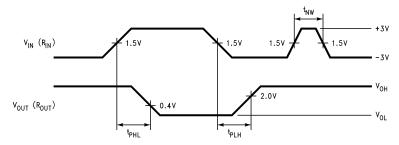


Figure 5. Receiver Propagation Delays and Noise Rejection

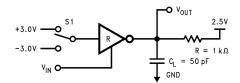


Figure 6. Receiver Disable Load Circuit

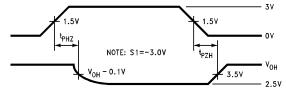


Figure 7. Receiver TRI-STATE Timing (t_{PHZ}, t_{PZH})

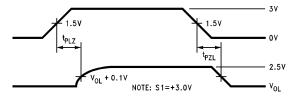


Figure 8. Receiver TRI-STATE Timing (t_{PLZ}, t_{PZL})



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PIN DESCRIPTIONS

V_{CC} (pin 11) —Power supply pin for the device,

+5V (±10%).

 V^+ (pin 13) —Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor: C4 = 1.0 μ F (6.3V). This supply is not intended to be loaded externally.

 V^- (pin 17) —Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor: C3 = 1.0 μ F (16V). This supply is not intended to be loaded externally.

C1⁺, C1⁻ (pins 12 and 14) —External capacitor connection pins. Recommended capacitor—1.0 μF (6.3V).

C2+, C2- (pins 15 and 16) - External capacitor connection pins. Recommended capacitor-1.0 µF (16V).

EN (pin 24) — Controls the Receiver output TRI-STATE Circuit. A HIGH level on this pin will disable the Receiver Output.

SHUTDOWN (SD) (pin 25) —A High on the SHUTDOWN pin will lower the total I_{CC} current to less than 10 μA. Providing a low power state.

 D_{IN} 1–4 (pins 7, 6, 20 and 21) —Driver input pins are TTL/CMOS compatible. Inputs of unused drivers may be left open, an internal pull-up resistor (500 k Ω minimum, typically 5 M Ω) pulls input to V_{CC} . Output will be LOW for open inputs.

Dout 1-4 (pins 2, 3, 1 and 28) — Driver output pins conform to TIA/EIA-232-E levels.

 R_{IN} 1–5 (pins 9, 4, 27, 23 and 18) —Receiver input pins accept TIA/EIA-232-E input voltages (±15V). Receivers feature a noise filter and ensured hysteresis of 200 mV. Unused receiver input pins may be left open. Internal input resistor (5 k Ω) pulls input LOW, providing a failsafe HIGH output.

Rout 1-5 (pins 8, 5, 26, 22 and 19) —Receiver output pins are TTL/CMOS compatible. Receiver output HIGH voltage is specified for both CMOS and TTL load conditions.

Product Folder Links: DS14C241

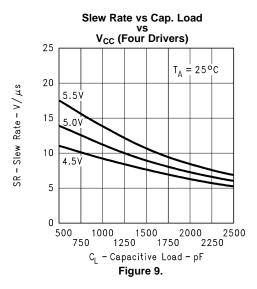
GND (pin 10) —Ground pin.

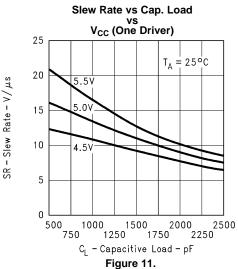
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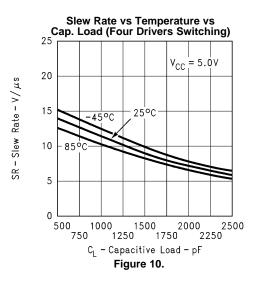
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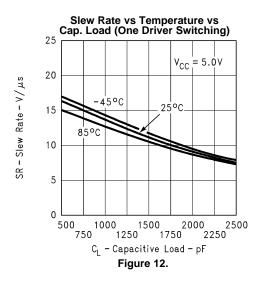


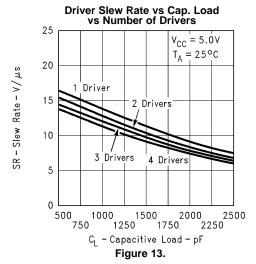
TYPICAL PERFORMANCE CHARACTERISTICS





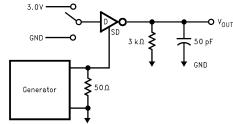






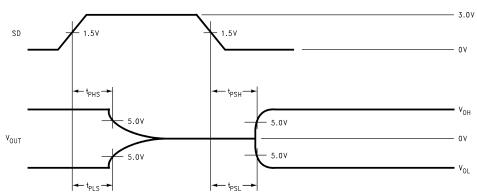


TYPICAL PERFORMANCE CHARACTERISTICS (continued)



Driver Shutdown (SD) Delay Test Circuit

Figure 14.



Driver Shutdown (SD) Delay Timing Waveforms

Figure 15.

Typical data only.

Symbol	Parameter	Conditions	Тур	Units
t _{PHS}	Propagation Delay High to SD	$V_{CC} = 5V^{(1)(2)}$	124	рs
t _{PLS}	Propagation Delay Low to SD	T _A = 25°C	110	μs
t _{PSH}	Propagation Delay SD to High		114	μs
t _{PSL}	Propagation Delay SD to Low		97	μs

(1) Sample size = 10 parts; 3 different datecodes.

(2) All drivers are loaded as shown in Figure 14.

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AE.



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