National Semiconductor

DS26F31C/DS26F31M
Quad High Speed Differential Line Driver

General Description

The DS26F31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26F31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The DS26F31 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F31 features lower power, extended temperature range, and improved specifications.

The circuit provides an enable and disable function common to all four drivers. The DS26F31C/DS26F31M features TRI-STATE® outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

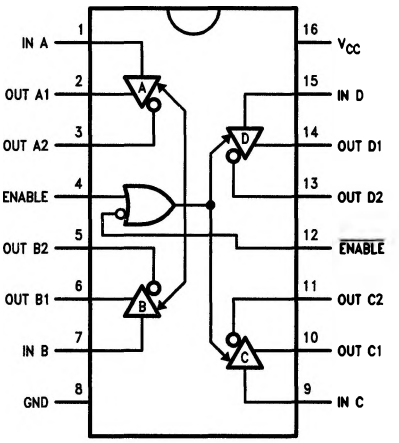
The DS26F31C/DS26F31M offers optimum performance when used with the DS26F32 Quad Differential Line Receiver.

Features

- Military temperature range
- Output skew—2.0 ns typical
- Input to output delay—10 ns
- Operation from single +5.0V supply
- 16-lead ceramic DIP Package
- Outputs won't load line when V_{CC} = 0V
- Output short circuit protection
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines

Connection and Logic Diagrams

16-Lead Dual-In-Line Package



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Top View

Order Number DS26F31CJ or DS26F31MJ
See NS Package Number J16A

For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS26F31ME/883, DS26F31MJ/883, or DS26F31MW/883
See NS Package Numbers E20A, J16A, or W16A

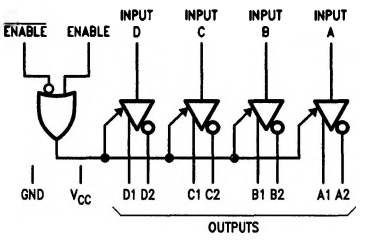

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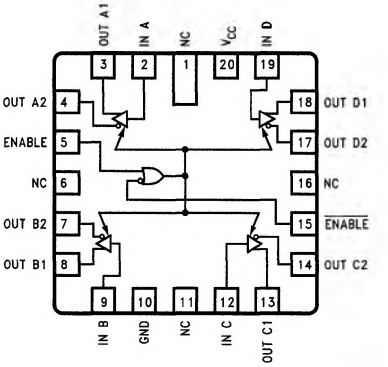
FIGURE 1. Logic Symbol

20-Lead Ceramic Leadless Chip Carrier (E)



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Supply Voltage	7.0V
Input Voltage	7.0V
Output Voltage	5.5V

*Derate cavity package 10 mW/°C above 25°C.

Operating Range

DS26F31C	
Temperature	0°C to +70°C
Supply Voltage	4.75V to 5.25V
DS26F31M	
Temperature	−55°C to +125°C
Supply Voltage	4.5V to 5.5V

Electrical Characteristics over operating range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output Voltage HIGH	V_{CC} = Min, I_{OH} = −20 mA		2.5	3.2		V
V_{OL}	Output Voltage LOW	V_{CC} = Min, I_{OL} = 20 mA			0.32	0.5	V
V_{IH}	Input Voltage HIGH	V_{CC} = Min		2.0			V
V_{IL}	Input Voltage LOW	V_{CC} = Max				0.8	V
I_{IL}	Input Current LOW	V_{CC} = Max, V_I = 0.4V			−0.10	−0.20	mA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_I = 2.7V			0.5	20	μA
I_{IR}	Input Reverse Current	V_{CC} = Max, V_I = 7.0V			0.001	0.1	mA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.5V		0.5	20	μA
			V_O = 0.5V		0.5	−20	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−0.8	−1.5	V
I_{OS}	Output Short Circuit	V_{CC} = Max (Note 4)		−30	−60	−150	mA
I_{CCX}	Supply Current	V_{CC} = Max, All Outputs Disabled				50	mA
I_{CC}		V_{CC} = Max, All Outputs Enabled				40	mA
t_{PLH}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5, Note 6			10	15	ns
t_{PHL}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5			10	15	ns
SKEW	Output to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5, Note 6			2.0	4.5	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10 pF			23	32	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10 pF			15	25	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5			20	30	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5			23	32	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS26F31M and across the 0°C to +70°C range for the DS26F31C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: C_L = 30 pF, V_I = 1.3V to V_O = 1.3V, V_{PULSE} = 0V to +3V (See AC Load Test Circuit for TRI-STATE Outputs).

Note 6: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Test Circuit and Timing Waveforms

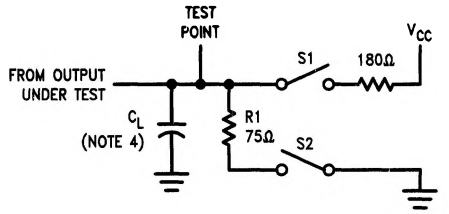

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FIGURE 2. AC Load Test Circuit for TRI-STATE Outputs

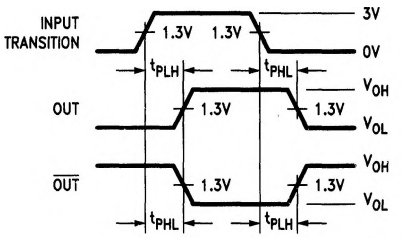

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FIGURE 3. Propagation Delay (Notes 1 and 3)

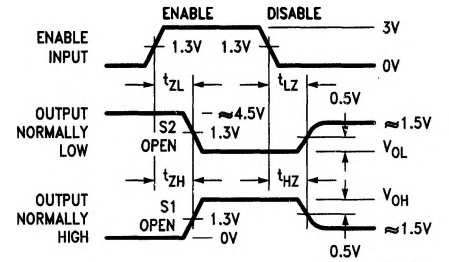

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FIGURE 4. Enable and Disable Times (Notes 2 and 3)

Note 1: Diagram shown for Enable Low. Switches S1 and S2 open.

Note 2: S1 and S2 of Load Circuit are closed except where shown.

Note 3: Pulse Generator for all Pulses: Rate ≤ 1.0 MHz, $Z_O = 50\Omega$, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns.

Note 4: C_L includes probe and jig capacitance.

Typical Application

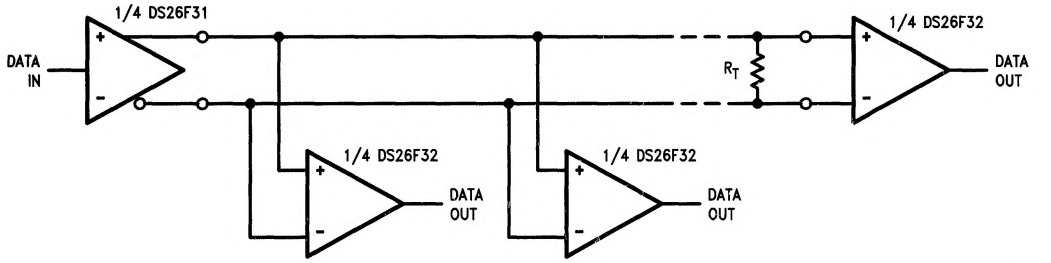

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FIGURE 5. Typical Application