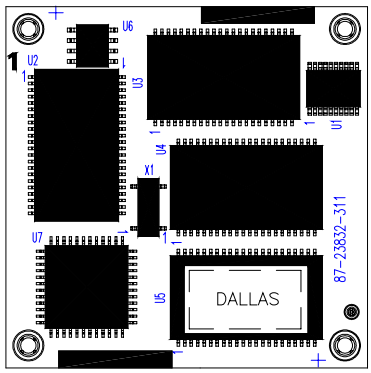
DS3832C-311
3.3V, 32Mb Advanced NV SRAM with Clock

www.maxim-ic.com

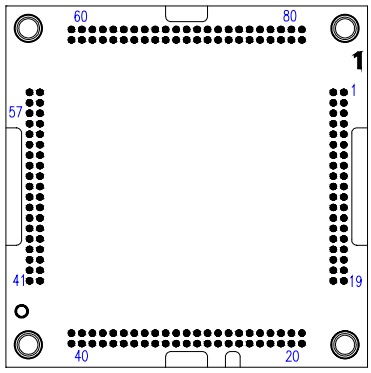
FEATURES

- 3.0V to 3.6V operation
- Surface-mount nonvolatile (NV) RAM ball-grid array (BGA) module construction
- 1024k x 32 NV SRAM memory space and separate 64 x 8 real-time clock (RTC) memory space
- RTC maintains hundredths of seconds, seconds, minutes, hours, day, date, month, and year with leap-year compensation valid up to 2100
- Removable backup power source provides more than eight years of timekeeping and data retention
- Read and write access times as fast as 100ns for NV SRAM memory and 200ns for RTC
- Automatic data protection during power loss
- Unlimited write-cycle endurance
- Low-power CMOS operation
- Battery monitor checks remaining capacity daily
- Industrial temperature range of -40°C to +85°C

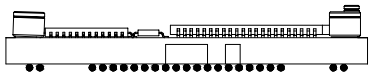
PACKAGE OUTLINE



Top View



Bottom View



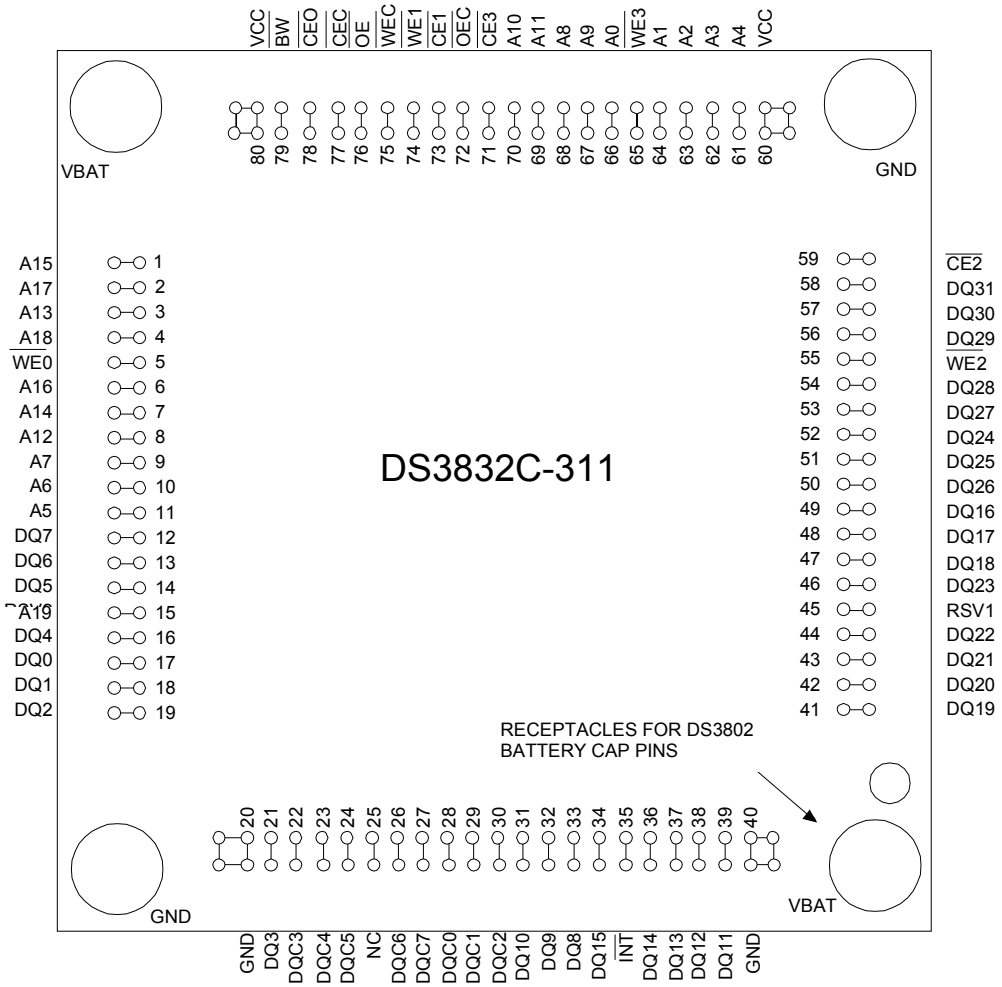
Side View

DESCRIPTION

The DS3832C-311 is a 1,048,576 x 32 advanced NV SRAM module with a 168-bump BGA pinout. The highly integrated DS3832C-311 contains a 64-byte RTC, four 8Mb SRAMs, and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the DS3832C-311 makes use of an attached DS3802 battery cap to maintain clock information and preserve stored data while protecting that data by disallowing all memory accesses. Additionally, the DS3832C-311 has dedicated circuitry for monitoring the status of V_{CC} and the status of an attached DS3802 battery cap.

PIN ASSIGNMENT (With Overlaid Package Outline) Figure 1

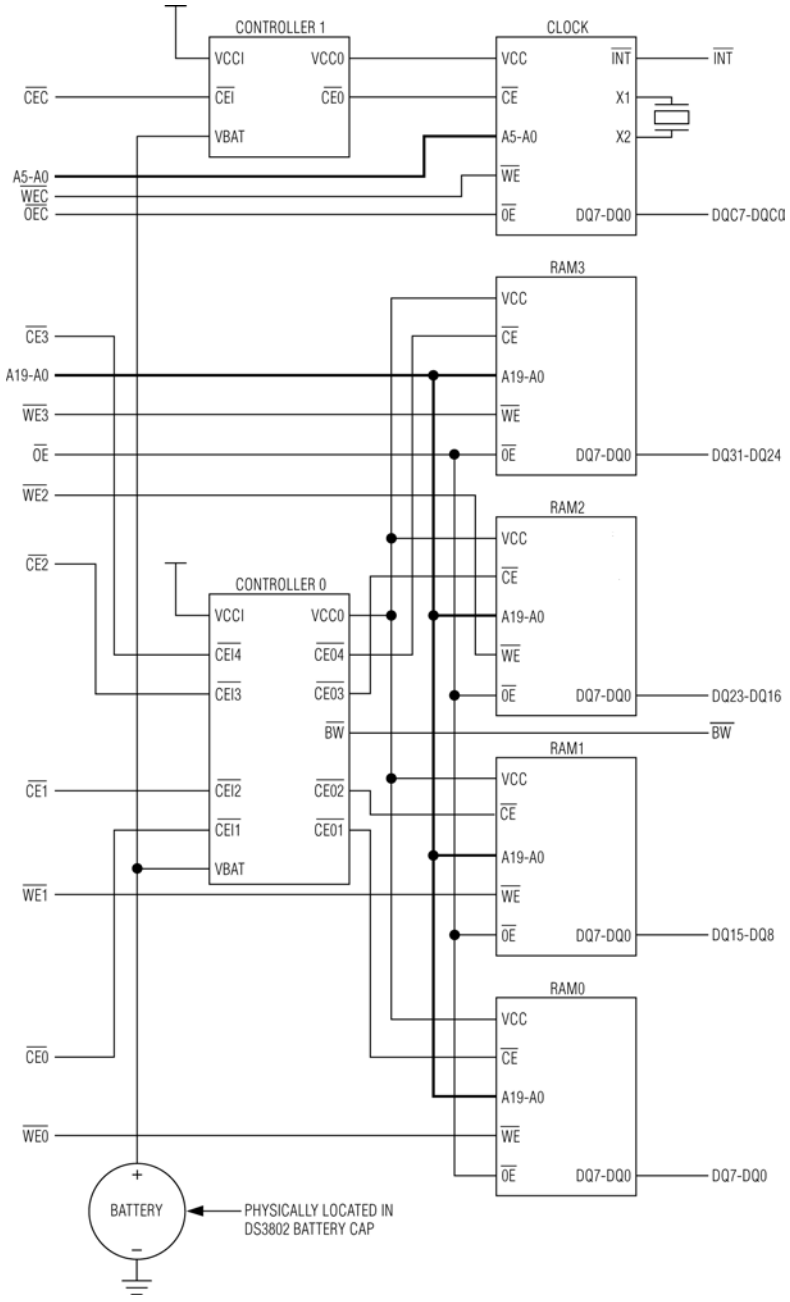
Because the DS3832C-311 has a total of 168 balls and only 76 active signals, balls are wired together into numbered groups, thus providing redundant connections for every signal.



PIN DESCRIPTION

A19 to A0 - Address Inputs
DQ31 to DQ0 - NV SRAM Data In/Data Out
DQC7 to DQC0 - Clock Data In/Data Out
$\overline{CE3}$ to $\overline{CE0}$ - NV SRAM Chip-Enable Inputs
$\overline{CEC}$ - Clock Chip-Enable Input
$\overline{WE3}$ to $\overline{WE0}$ - NV SRAM Write-Enable Inputs
$\overline{WEC}$ - Clock Write-Enable Input
$\overline{OE}$ - NV SRAM Output-Enable Input
$\overline{OEC}$ - Clock Output-Enable Input
$\overline{BW}$ - Battery Warning Output
$\overline{INT}$ - Interrupt Output
V_{CC} - Power (3.3V)
GND - Ground
RSV1 - No Connect
VBAT - DS3802 Battery Cap Connection

BLOCK DIAGRAM Figure 2



NV SRAM READ MODE

The DS3832C-311 executes an NV SRAM read cycle whenever $\overline{WE0}$ to $\overline{WE3}$ (write enables) are inactive (high), any or all of $\overline{CE0}$ to $\overline{CE3}$ (chip enables) are active (low) and $\overline{OE}$ (output enable) is active (low). The unique address specified by the 20 address inputs (A_0 to A_{19}) defines which of the 1,048,576 words of data is accessed. The four chip-enable signals ($\overline{CE0}$ to $\overline{CE3}$) determine which bytes in the addressed word are output on data lines DQ31 to DQ0. Valid data will be output within t_{ACC} (NV SRAM access time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{CE}$ and $\overline{OE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than t_{ACC}.

NV SRAM WRITE MODE

The DS3832C-311 executes an NV SRAM write cycle whenever any or all of the $\overline{WE}$ signals ($\overline{WE0}$ to $\overline{WE3}$) are active (low) and any of the corresponding $\overline{CE}$\ signals ($\overline{CE0}$ to $\overline{CE3}$) are active (low) after all address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ determines the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE0}$ to $\overline{WE3}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ disables the outputs in t_{ODW} from its falling edge.

CLOCK READ MODE

The DS3832C-311 executes a clock read cycle whenever $\overline{WEC}$ (clock write enable) is inactive (high), $\overline{CEC}$ (clock chip enable) is active (low), and $\overline{OEC}$ (output enable) is active (low). The unique clock address specified by address inputs A_0 to A_5 defines which of the 64 bytes of data is accessed. Valid data is output within t_{ACC} (clock access time) after the last address input signal is stable, providing that $\overline{CEC}$ and $\overline{OEC}$ (output enable) access times are also satisfied. If $\overline{CEC}$ and $\overline{OEC}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CEC}$ or $\overline{OEC}$) and the limiting parameter is either t_{CO} for $\overline{CEC}$ or t_{OE} for $\overline{OEC}$ rather than t_{ACC}. Only addresses 0 to 3Fh are implemented in the clock address space. Accesses to clock addresses higher than 3Fh are undefined.

CLOCK WRITE MODE

The DS3832C-311 executes a clock write cycle whenever $\overline{WEC}$ is active (low) and $\overline{CEC}$ is active (low) after all address inputs are stable. The later occurring falling edge of $\overline{CEC}$ or $\overline{WEC}$ determines the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CEC}$ or $\overline{WEC}$. All address inputs must be kept valid throughout the write cycle. $\overline{WEC}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OEC}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if output drivers are enabled ($\overline{CEC}$ and $\overline{OEC}$ active) then $\overline{WEC}$ disables the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

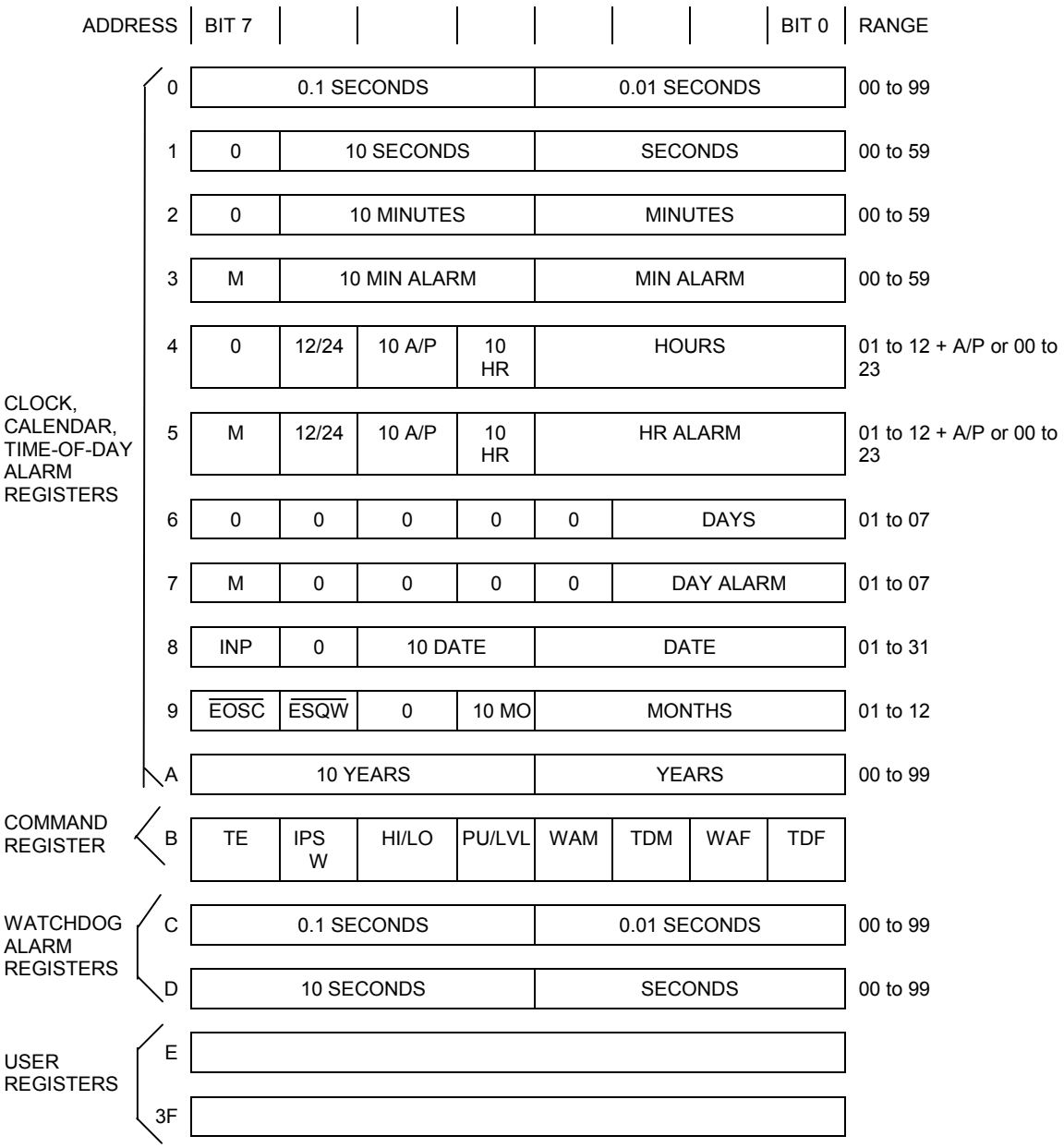
The DS3832C-311 provides full functional capability for V_{CC} greater than 3.0V and write protects by 2.8V. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS3832C-311 constantly monitors V_{CC}. Should the supply voltage decay to V_{TP}, the device automatically write protects itself, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 2.8V, a power-switching circuit electrically connects an attached DS3802 battery cap to the SRAM to retain data. During power-up, when V_{CC} rises above approximately 2.8V, the power-switching circuit connects external V_{CC} to the SRAM and disconnects the DS3802 normal RAM operation can resume after V_{CC} reaches the minimum power-supply voltage.

BATTERY MONITORING

The DS3832C-311 automatically monitors the battery in an attached DS3802 battery cap on a 24-hour time interval. Such monitoring begins within t_{REC} after V_{CC} rises above V_{TP} and is suspended when power failure occurs.

After each 24-hour period has elapsed, the battery is connected to an internal 1MΩ test resistor for one second. During this one second, if battery voltage falls below the battery voltage trip point (2.6V), the battery warning output $\overline{BW}$ is asserted. Once asserted, $\overline{BW}$ remains active until the battery cap or DS3802 is replaced. The battery is still retested after each V_{CC} power-up even if $\overline{BW}$ is active. If the battery voltage is found to be higher than 2.6V during such testing, $\overline{BW}$ is de-asserted and regular 24-hour testing resumes. $\overline{BW}$ has an open-drain output driver.

CLOCK REGISTERS Figure 3



TIME-OF-DAY ALARM MASK BITS (Figure 4)

REGISTER			ALARM
MINUTES	HOURS	DAYS	
1	1	1	ALARM ONCE PER MINUTE
0	1	1	ALARM WHEN MINUTES MATCH
0	0	1	ALARM WHEN MINUTES AND HOURS MATCH
0	0	0	ALARM WHEN MINUTES, HOURS, AND DAYS MATCH

NOTE:

Any other bit combinations produce illogical operation.

CLOCK REGISTERS

The DS3832C-311 clock has 14 8-bit internal registers that contain all timekeeping, alarm, watchdog, and control information. The clock, calendar, alarm, and watchdog registers are memory locations that contain both external (user-accessible) and internal copies of the data. The external copies are independent of internal functions except that they are updated periodically by simultaneous transfer from the incremented internal copies. The command register bits are affected by both internal and external functions. In addition to the 14 registers, the clock also contains 50 bytes of user RAM. Clock registers 0, 1, 2, 4, 6, 8, 9, and A (hex) contain day, date, and time information stored in binary-code decimal (BCD) format. Registers 3, 5, and 7 contain time-of-day alarm information also stored in BCD format. Register B is the command register containing eight 1-bit binary fields. Registers C and D contain watchdog alarm information stored in BCD format. Addresses E through 3F are general-purpose user RAM.

DAY, DATE AND TIME REGISTERS

Registers 0, 1, 2, 4, 6, 8, 9, and A (hex) contain day, date, and time information in BCD format. Eleven bits within these eight registers are not used and will always read zero regardless of how they are written. Bits 6 and 7 in the month register (register 9) are binary control bits.

When set to logic 0, $\overline{\text{EOSC}}$ (register 9, bit 7) enables the clock oscillator. This bit is normally turned on by the user during device initialization. The oscillator can be turned on and off as needed by enabling or disabling this bit.

Register 8 bit 7, INP, controls the logic state of the $\overline{\text{INTP}}$ output pin of the clock device. Because this logic feature is not supported in the DS3832C-311, INP should be set to a logic zero.

Register 9 bit 6, $\overline{\text{ESQW}}$, enables and disables the output of a 1024Hz square wave. Because this feature is not supported in the DS3832C-311, $\overline{\text{ESQW}}$ should be set to logic one.

Bit 6 of the hour register (register 4) is defined as the 12- or 24-hour select bit. When set to logic one, the 12-hour format is selected. In the 12-hour format, bit 5 is the AM/PM bit with logic 1 being PM. In the 24-hour mode, bit 5 is the upper-order 10-hour bit (set for hours 20 to 23).

The external day, date, and time registers are updated from their internal counterparts every 0.01 seconds except when the TE bit (bit 7 of register B) is set low or the clock oscillator is not running ($\overline{\text{EOSC}}$ high). Setting TE low freezes the external day, date, and time registers at their present values allowing all the registers to be read or written without any of them being updated from the internal registers. After the

registers have been read or written, setting TE high re-enables external register updates. While TE is set low and the external registers are frozen, the internal registers continue to be incremented.

TIME-OF-DAY ALARM REGISTERS

Registers 3, 5, and 7 contain the time-of-day alarm registers. Bits 3, 4, 5, and 6 of register 7 always read zero regardless of how they are written. Bit 7 of registers 3, 5, and 7 are mask bits (see Figure 4). When all of the mask bits are logic 0, a time-of-day alarm only occurs when registers 2, 4, and 6 match the values stored in registers 3, 5, and 7. An alarm is generated every day when bit 7 of register 7 is set to logic 1. Similarly, an alarm is generated every hour when registers 7 and 5 both have bit 7 set to logic 1. When registers 7, 5, and 3 all have bit 7 set to logic 1, an alarm occurs every minute at the point where register 1 (seconds) rolls over from 59 to 00. Whenever an alarm occurs, the time-of-day alarm flag TDF (register B, bit 0) and the internal time-of-day interrupt signal goes to the active state. If the interrupt-switch bit IPSW (register B, bit 6) is set to a logic 0 and the time-of-day alarm mask bit TDM (register B, bit 3) is logic 0, the interrupt-output pin $\overline{INT}$ also activates.

Time-of-day alarm registers are written and read in the same format as the day, date, and time registers. The time-of-day alarm flag, time-of-day interrupt, and $\overline{INT}$ output are always cleared when the time-of-day alarm registers are read or written.

WATCHDOG ALARM REGISTERS

Registers C and D contain the timeout period for the watchdog alarm. The two registers contain a count from 0.01 to 99.99 seconds in BCD format. The two watchdog alarm registers can be written or read in any order. After a new value is entered or either of the watchdog alarm registers is read, an internal watchdog timer starts counting down from the entered watchdog alarm register value toward zero. When zero is reached, the watchdog alarm flag (register B, bit 1) and the internal watchdog interrupt signal go to the active state. If the interrupt switch bit IPSW (register B bit 6) is set to logic 1 and the watchdog alarm mask bit WAM (register B, bit 3) is logic 0, the interrupt output $\overline{INT}$ also activates. The watchdog timer countdown is interrupted and the timer is re-initialized to the value in the watchdog alarm registers every time either watchdog alarm register is accessed. Controlled, periodic accesses to the watchdog alarm registers can prevent the activation of the watchdog alarm flag, the internal watchdog interrupt signal and the $\overline{INT}$ output. The watchdog alarm registers always read the value entered. The actual watchdog timer is internal and is not accessible. Writing 00h to registers C and D disables the watchdog alarm feature.

COMMAND REGISTER

Register B, the command register, contains control bits and flag bits. The operation of each bit is described below.

TE—Transfer Enable (Bit 7). When set to logic 0, this bit disables the transfer of data between internal and external clock registers. The contents of the external registers are frozen and reads and writes of day, date, and time information are not affected by updates. This bit must be set to logic 1 to enable updates.

IPSW—Interrupt Switch (Bit 6). This bit should be initialized to logic 1 to connect the internal watchdog interrupt signal to the $\overline{INT}$ output pin. Setting this bit to logic 0 connects the internal time-of-day interrupt signal to the $\overline{INT}$ output pin.

HI/LO—$\overline{INT}$ Sink or Source Current (Bit 5). When this bit is set to logic 1 and V_{CC} is applied, the $\overline{INT}$ output pin will source current when activated (see I_{OH} spec). When this bit is set to logic 0, $\overline{INT}$ sinks current (see I_{OL} spec).

PU/LVL—$\overline{INT}$ Pulse or Level (Bit 4). When this bit is set to logic 0, $\overline{INT}$ is in the level mode, going to the logic level defined by the HI/LO bit and staying there until the interrupt is cleared. When this bit is set to logic 1, $\overline{INT}$ is in pulse mode, sourcing or sinking current as defined by the HI/LO bit for a minimum of 3ms and then releasing.

WAM—Watchdog Alarm Mask (Bit 3). When this bit is set to logic 0, the internal watchdog interrupt signal is enabled. If IPSW is also set to logic 1, any watchdog alarm activates the $\overline{INT}$ output. When this bit is set to logic 1, watchdog alarms have no effect on the internal watchdog interrupt signal or on the $\overline{INT}$ pin.

TDM—Time-of-Day Alarm Mask (Bit 2). When this bit is set to logic 0, the internal time-of-day interrupt signal is enabled. If IPSW is set to logic 0, any time-of-day alarm activates the $\overline{INT}$ output. When this bit is set to logic 1, time-of-day alarms have no effect on the internal time-of-day interrupt signal or on the $\overline{INT}$ pin.

WAF—Watchdog Alarm Flag (Bit 1). This bit is set to logic 1 when a watchdog alarm occurs (regardless of the state of the watchdog alarm mask bit WAM). WAF is read-only. This bit is reset when either of the watchdog alarm registers is accessed. When the PU/LVL bit is in the pulse mode, this flag is only set to logic 1 for the 3ms duration of the $\overline{INT}$ output pulse.

TDF—Time-of-Day Alarm Flag (Bit 0). This bit is set to logic 1 when a time-of-day alarm occurs (regardless of the state of the time-of-day alarm mask bit TDM). TDF is read-only. The time the alarm occurred can be determined by reading the time-of-day alarm registers. This bit is reset to logic 0 when any of the time-of-day alarm registers is accessed. When the PU/LVL bit is in the pulse mode, this flag is only set to logic 1 for the 3ms duration of the $\overline{INT}$ output pulse.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3 to +4.6 V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +85°C
Soldering Temperature	See IPC/JEDEC J-STD-020A Specification

** This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

RECOMMENDED DC OPERATING CONDITIONS (T_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	1
Logic 1 Input Voltage	V_{IH}	2.2		V_{CC}	V	1
Logic 0 Input Voltage	V_{IL}	0		0.6	V	1

DC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C; V_{CC}= 3.3V ± 0.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-5		5	µA	
I/O Leakage Current	I_{IO}	-1		1	µA	
Output Current at 2.4V	I_{OH}	-1			mA	
Output Current at 0.4V	I_{OL}	2			mA	
Standby Current (All $\overline{CE}$ = V_{IH})	I_{CCS1}		5	7	mA	
Standby Current (All $\overline{CE}$ = V_{CC} - 0.3V)	I_{CCS2}		2	5	mA	
Operating Current (One $\overline{CE}$ = V_{IL})	I_{CCO1}			50	mA	4
Operating Current (All $\overline{CE}$ = V_{IL})	I_{CCO2}			200	mA	4
Write Protection Voltage	V_{TP}	2.8	2.9	3.0	V	

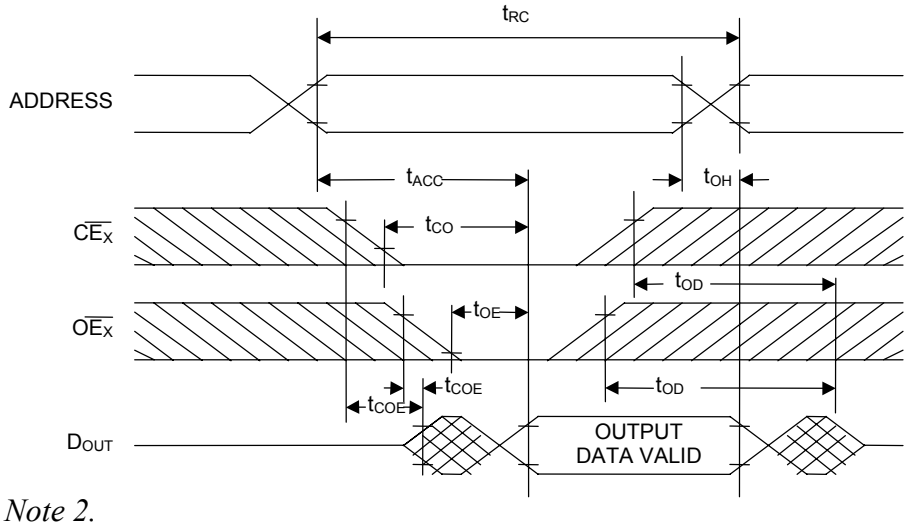
CAPACITANCE (T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance: A19 to A0, $\overline{OE}$	C_{IN}		25	50	pF	
Input Capacitance: $\overline{CE3}$ – $\overline{CE0}$, $\overline{WE3}$ – $\overline{WE0}$, $\overline{CEC}$, $\overline{WEC}$, $\overline{OEC}$	C_{IN}		5	10	pF	
I/O Capacitance: DQ31–DQ0, DQC7–DQC0	$C_{I/O}$		5	10	pF	
Output Capacitance: $\overline{BW}$, $\overline{INT}$	C_{OUT}		5	10	pF	

AC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C; V_{CC}= 3.3V ± 0.3V)

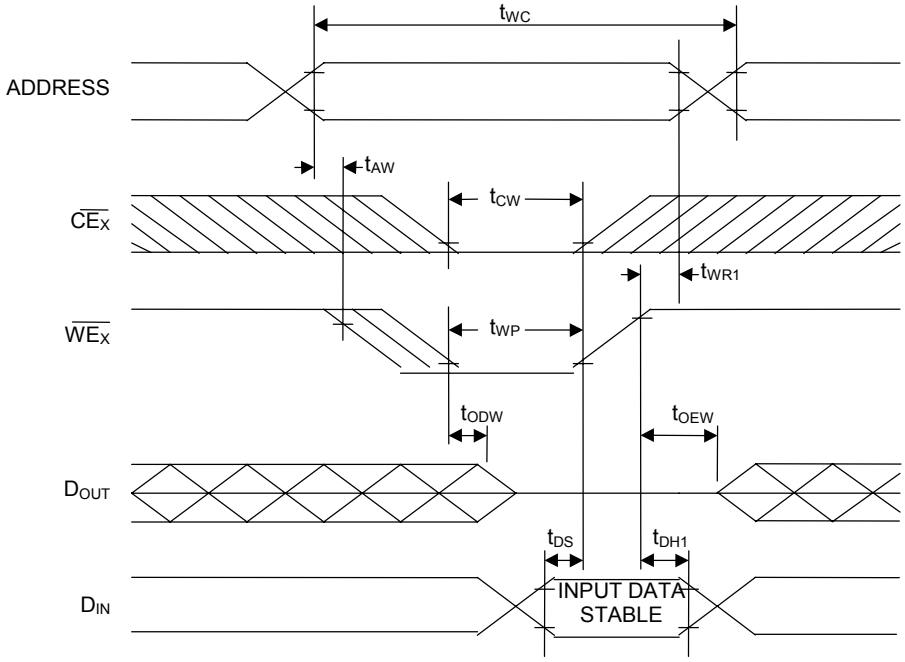
		NV SRAM		CLOCK			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	100		200		ns	
Access Time	t_{ACC}		100		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		50		70	ns	
$\overline{CE}$ to Output Valid	t_{CO}		100		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	6
Output High-Z from Deselection	t_{OD}		35		50	ns	6
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	100		200		ns	
$\overline{CE}$ Pulse Width	t_{CW}	100		200			
Write Pulse Width	t_{WP}	75		150		ns	
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 20		15 20		ns ns	12 13
Output High-Z from $\overline{WE}$	t_{ODW}		35		50	ns	6
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	6
Data Setup Time	t_{DS}	40		100		ns	5
Data Hold Time	t_{DH1} t_{DH2}	0 20		0 20		ns ns	12 13

TIMING DIAGRAM: READ CYCLE



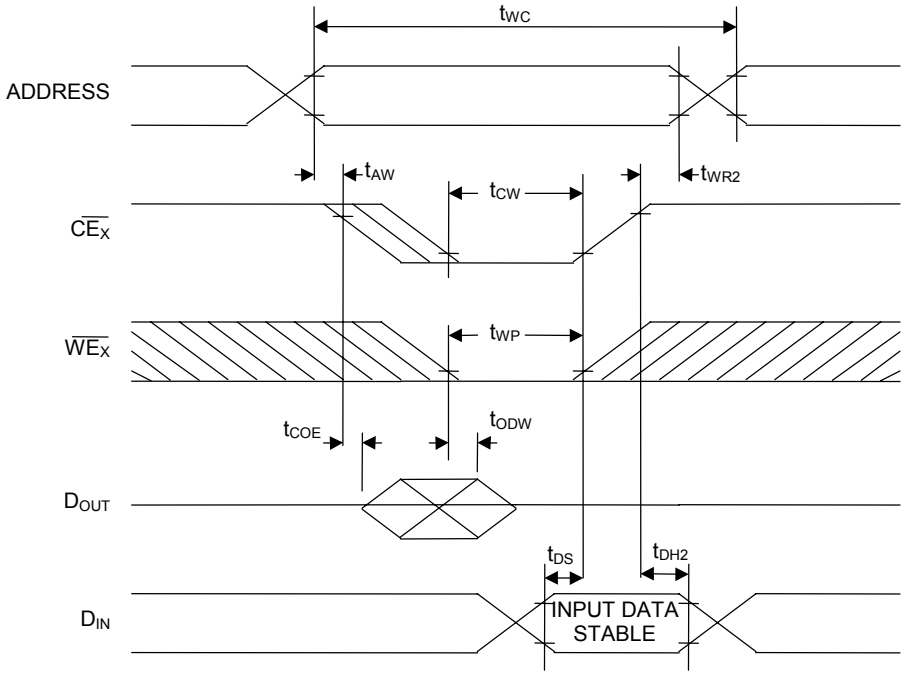
See Note 2.

TIMING DIAGRAM: WRITE CYCLE 1 ($\overline{WE}$)



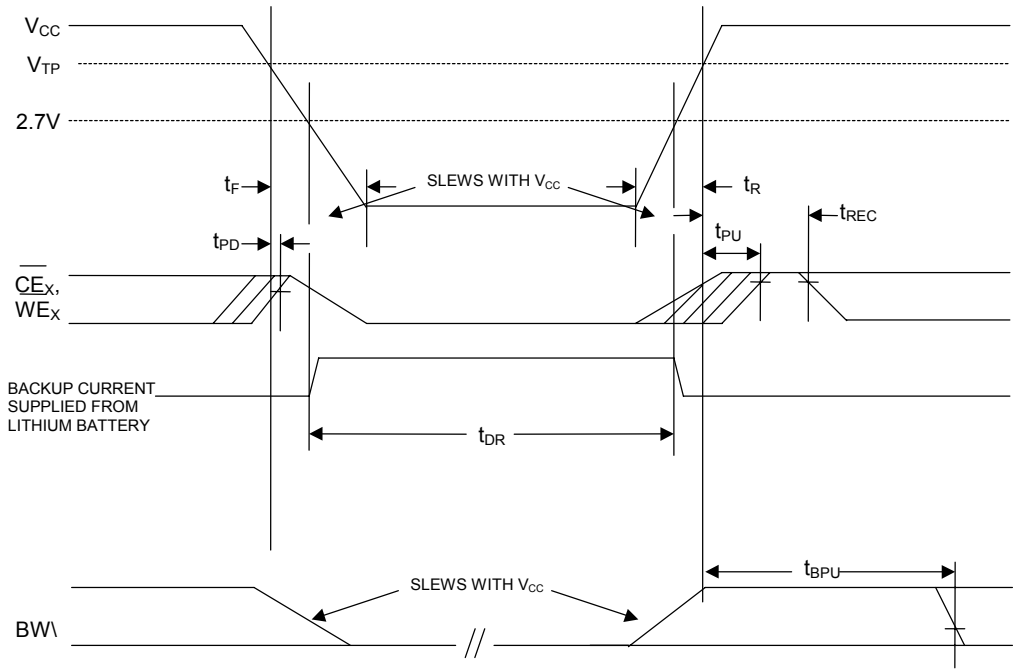
See Notes 3, 5, 7, 8, 9, and 12.

TIMING DIAGRAM: WRITE CYCLE 2 ($\overline{CE}$)



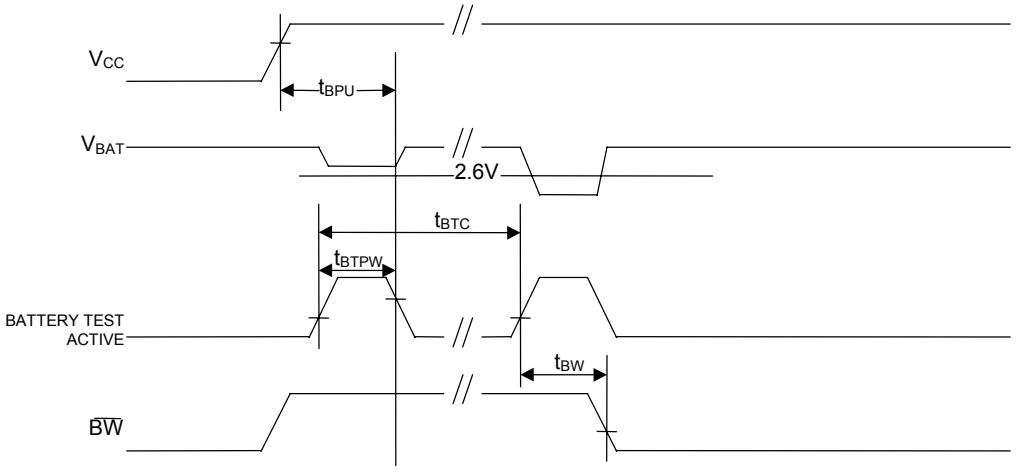
See Notes 3, 5, 7, 8, 9, and 13.

POWER-DOWN/POWER-UP CONDITION



See Note 11.

TIMING DIAGRAM: BATTERY WARNING DETECTION



See Note 14.

POWER-DOWN/POWER-UP TIMING

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to $\overline{CE}$ and WE\ Inactive	t_{PD}			0	µs	11
V_{CC} Slew from V_{TP} to 0V	t_F	300			µs	
V_{CC} Slew from 0V to V_{TP}	t_R	300			µs	
V_{CC} Valid to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PU}			2	ms	
V_{CC} Valid to End of Write Protection	t_{REC}			125	ms	
V_{CC} Valid to $\overline{BW}$ Valid	t_{BPU}			1	s	14
$\overline{INT}$ Pulse Width (PU/LVL Bit High)	t_{IPW}	3			ms	15

BATTERY WARNING TIMING

(T_A = -40°C to +85°C; V_{CC} = 3.3V ± 0.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Test Cycle	t_{BTC}		24		hr	
Battery Test Pulse Width	t_{BTPW}			1	s	
Battery Test to $\overline{BW}$ Active	t_{BW}			1	s	

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	8			years	10

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when this device is in battery backup mode.

NOTES:

1) All voltages referenced to ground.
2) $\overline{WE}$ is high throughout read cycle.
3) $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high-impedance state.
4) All outputs open-circuited.
5) t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
6) These parameters are sampled with a 5pF load and are not 100% tested.
7) If the $\overline{CE}$ low transition occurs simultaneously with, or later than, the $\overline{WE}$ low transition, the output buffers remain in a high-impedance state during this period.
8) If the $\overline{CE}$ high transition occurs prior to, or simultaneously with, the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.
9) If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to, or simultaneously with, the $\overline{CE}$ low transition, the output buffers remain in a high-impedance state during this period.
10) Expected data retention time can be extended indefinitely if the DS3802 battery cap is periodically replaced.
11) In a power-down condition, the voltage on any pin may not exceed the voltage on V_{CC}.
12) t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13) t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.
14) $\overline{BW}$ is an open-drain output and cannot source current. An external pullup resistor should be connected to this pin for proper operation. This pin sinks 10mA.
15) $\overline{INT}$ activates within 100ns after the alarm condition arises.

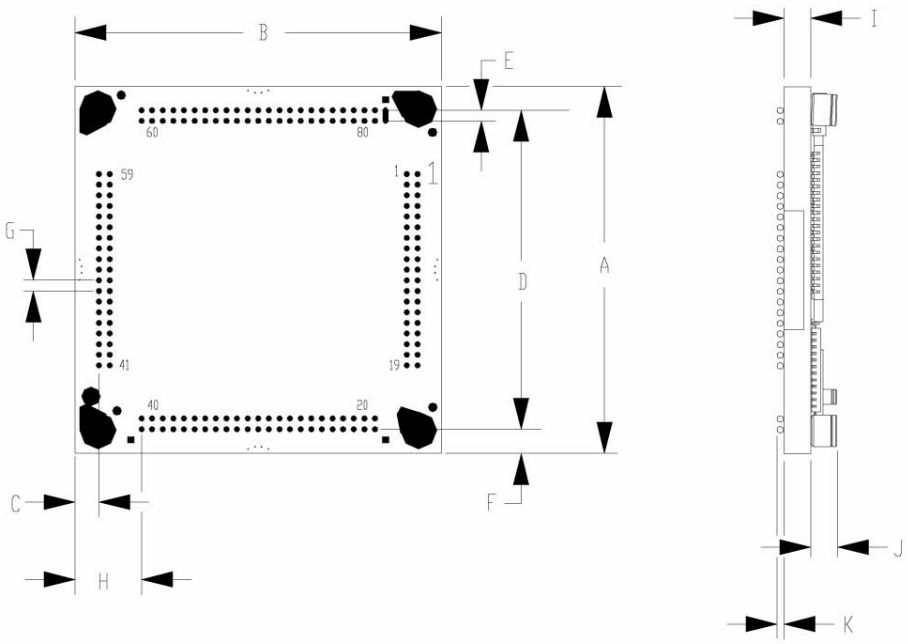
DC TEST CONDITIONS

Outputs Open
All voltages are referenced to ground

AC TEST CONDITIONS

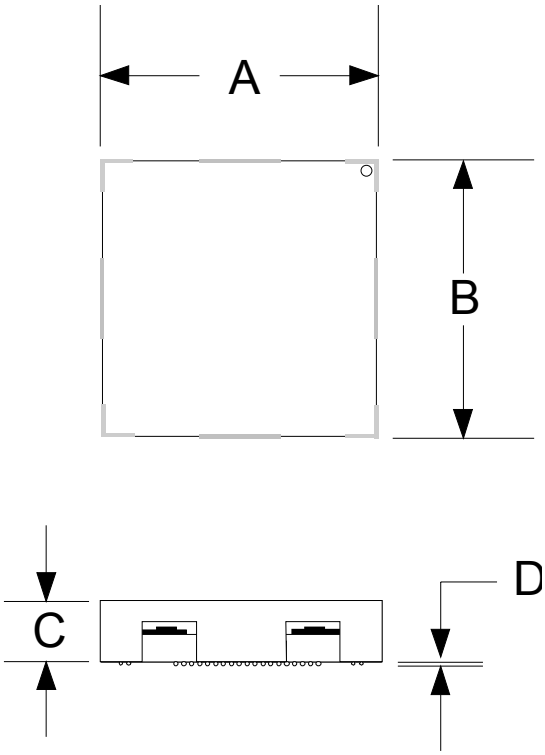
Output load: 100pF + 1 TTL gate
Input pulse levels: 0V to 2.7V
Timing measurement reference levels
Input: 1.5V
Output: 1.5V
Input pulse rise and fall times: 5ns

DS3832C-311 PACKAGE DIMENSIONS



DIM		MIN	MAX
A	**in**	1.720	1.730
	mm	43.69	43.94
B	**in**	1.720	1.730
	mm	43.69	43.94
C	**in**	0.108	0.118
	mm	2.74	3.00
D	**in**	1.497	1.503
	mm	38.02	38.18
E	**in**	0.047	0.053
	mm	1.19	1.35
F	**in**	0.108	0.118
	mm	2.74	3.00
G	**in**	0.047	0.053
	mm	1.19	1.35
H	**in**	0.305	0.320
	mm	7.74	8.13
I	**in**	0.125	0.135
	mm	3.10	3.43
J	**in**	-	.135
	mm	-	3.43
K	**in**	0.025	0.032
	mm	0.64	0.76

DS3832C-311 PACKAGE DIMENSIONS (With Attached DS3802 Battery Cap)



DIM		MIN	MAX
A	**in**	-	1.830
	mm	-	45.046
B	**in**	-	1.830
	mm	-	45.046
C	**in**	-	0.435
	mm	-	10.708
D	**in**	-	0.0390
	mm	-	0.9600

DS3832C-311 RECOMMENDED LAND PATTERN
(With Overlaid Package Outline)

The DS3832C-311 ball grid array is a subset of the industry-standard 40mm BGA format, with all balls on a 50mil grid. Corner balls have been removed to provide space for the electrical and mechanical interface features that facilitate attachment of the DS3802 battery cap